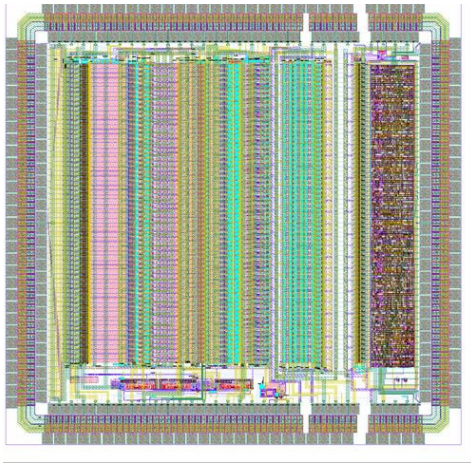
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

MAROC 1 Run : SiGe 0.35mm 13 June 2005

MAROC 2 Run : SiGe 0.35mm 6 mars 2006



ATLAS LUMINOMETRY
64-channel Front-End readout chip status
MAROC 2 (Multi Anode Readout Chip)
Version 2

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Table of content

I. GENERAL DESCRIPTION

The MAROC2 chip is a 64-channel input front end circuit to read out multi-anodes photomultiplier (MAPMT) outputs. It provides one shaped signal proportional to the input charge and 64 trigger outputs.

Figure 1 gives a simplified schematic diagram of the whole chip. The different blocks are described in the next section.

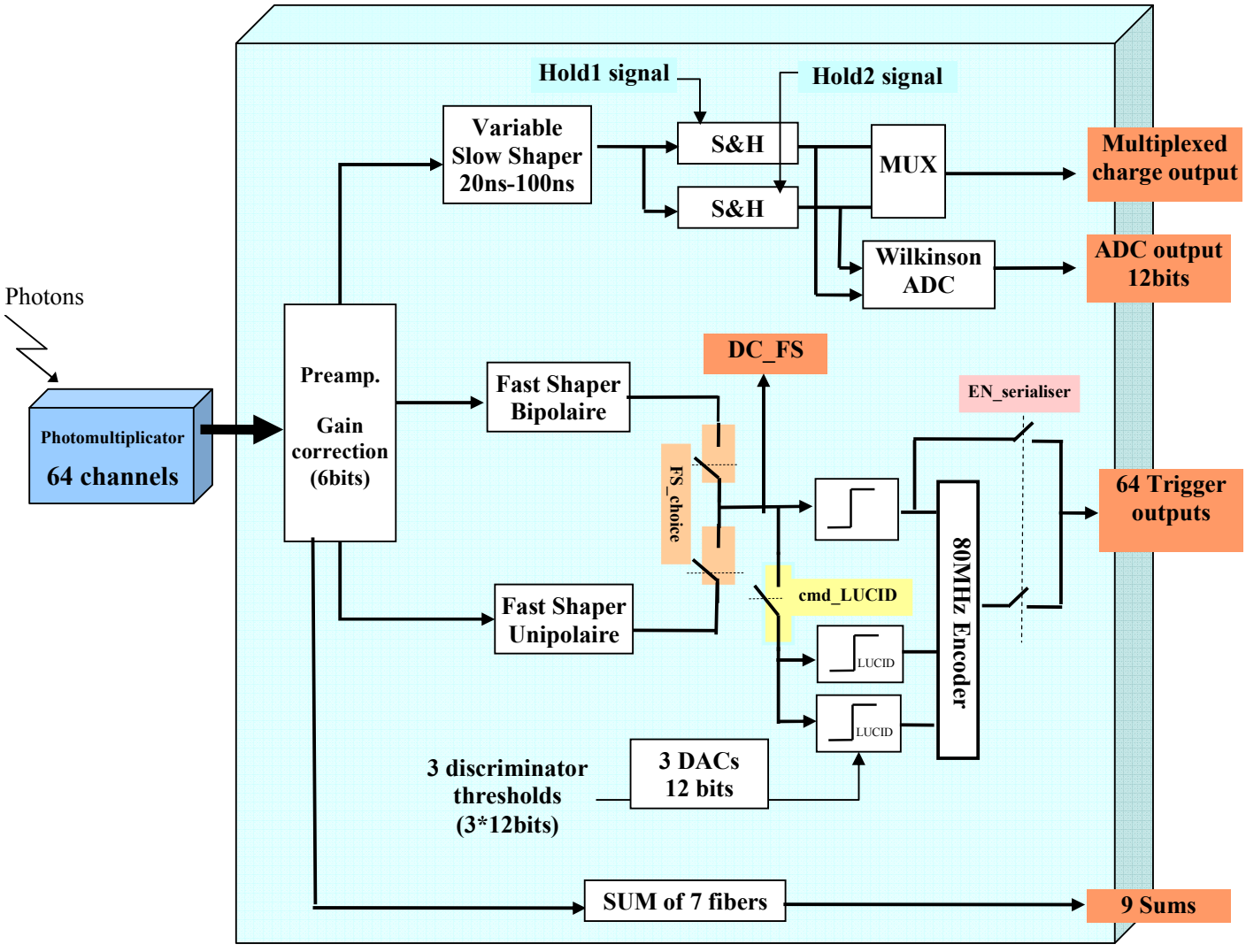


Figure 1: Block schematics of MAROC2chip architecture

The chip characteristics are the following:

- Technology : AMS SiGe 0.35µm
- Chip Area : 16 mm^2 (4mm *3.9mm)
- Package : CQFP240
- Power consumption : 350 mW
- Power supply : 0-3.5 V

The electronic requirements are the following:

- Dynamic range: 1 φe- to 30 φe- with a gain of 10^6, i.e 160 fC to 4800 fC (10 ns current pulse from 16 uA to 160 uA)
- **Counting rate:** > 10 MHz
- **Discriminator threshold:** 100 % sensitivity to 1 φe- => Threshold = 0.3 φe- 3 thresholds for LUCID application
- **64 digital outputs**

II. BLOCK FUNCTIONALITY DIAGRAM:

1. One channel description

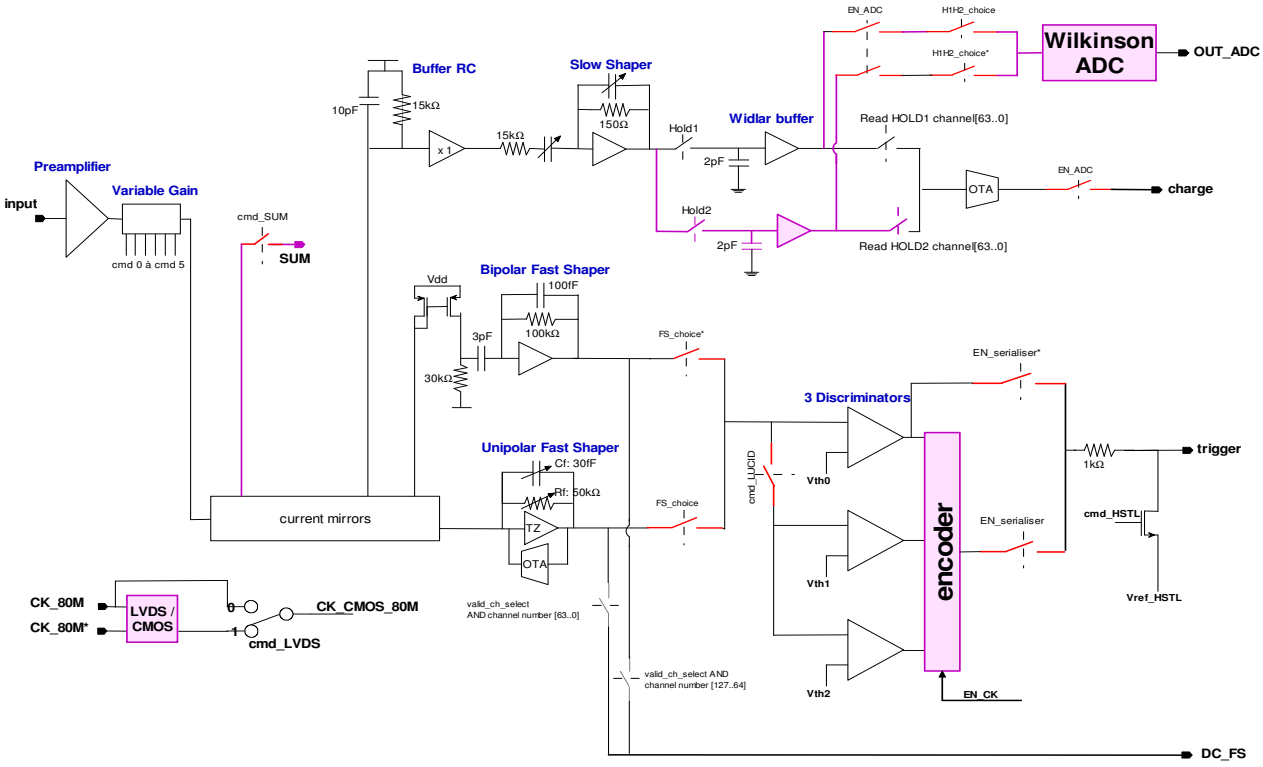


Figure 2: One channel schematic

Figure2 shows a simplified block scheme of one channel. Each channel is made of a variable gain preamplifier which has low offset and low input impedance to minimise crosstalk. It allows compensating for the PM gain dispersion up to a factor 4 with 6 bits.

The amplifier current feeds then 3 possible paths:

- Slow channel path: one slow shaper with three switchable feedback capacitances to allow tuning peaking time of signal followed by two Track and Hold buffers. The idea is to use the first one to measure the baseline and the second one to store the charge in 2pF. An OTA delivers the multiplexed charge.
- Fast channel path: two possible fast shapers (bipolar and unipolar) selected with FS_choice switch are followed by a one discriminator (low offset comparator) to deliver trigger outputs. Two other discriminators are implemented to trig for different thresholds (cmd_LUCID switch) so a 2 bits encoded trigger outputs has to be used (EN_serialiser=1).

Like MAROC1, the biases of each stage are common for every channel and have an internal default value.

In this new version of MAROC, a 12 bit Wilkinson ADC is added for future applications and a LVDS/CMOS translator to drive the input clock used by the ADC and the encoder.

2. Preamplifier

2.a. Schematic

The preamplifier is a super common base to minimise the input impedance following by scaled mirror to set the gain for each channel. The gain of 0 allows inhibiting the signal at input. Otherwise the gain can be tuned from 0 to about 4.

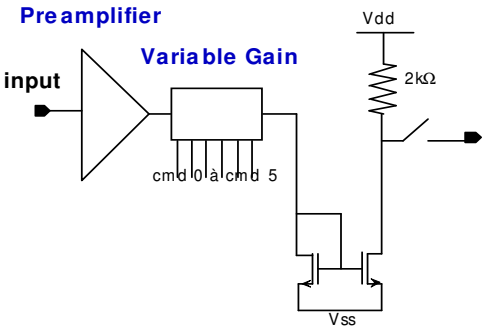


Figure 3: Block schematic

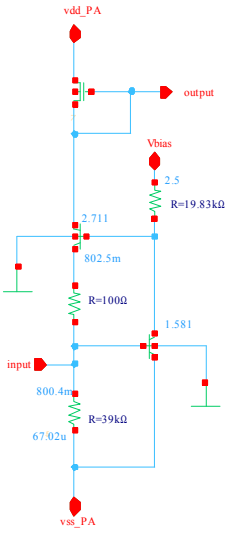


Figure 4: Super Base Commune schematic

The input impedance of the SBC is given by: Zin= $1/gm_1gm_2Rc$ which is a low value resulting in small currents in the mirrors and thereby reducing the crosstalk.

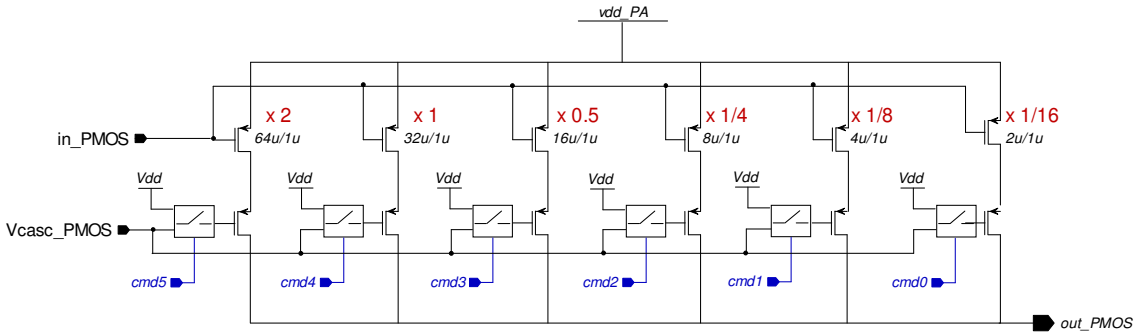


Figure 5: Variable Gain block

We have 6 bits to set the gain. The gain value 16 corresponds to the unity gain. The bias current can be up to 80µA.

3. SUM

3.a. Principe

We added the possibility to make a sum of 7 channel preamplifier signals.

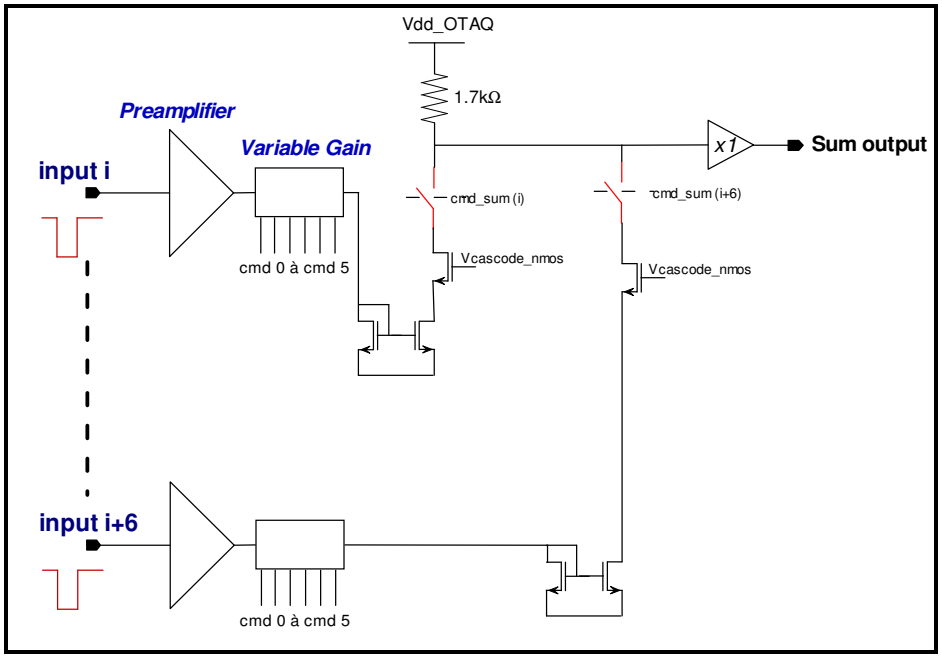


Figure 6: Sum schematic

3.b. Measurements

➢ DC measurements

Figure 7 represents the pedestal measured on the sum output for different number of fibers summed. Figure 8 shows that there is a nice linearity for this measurement.

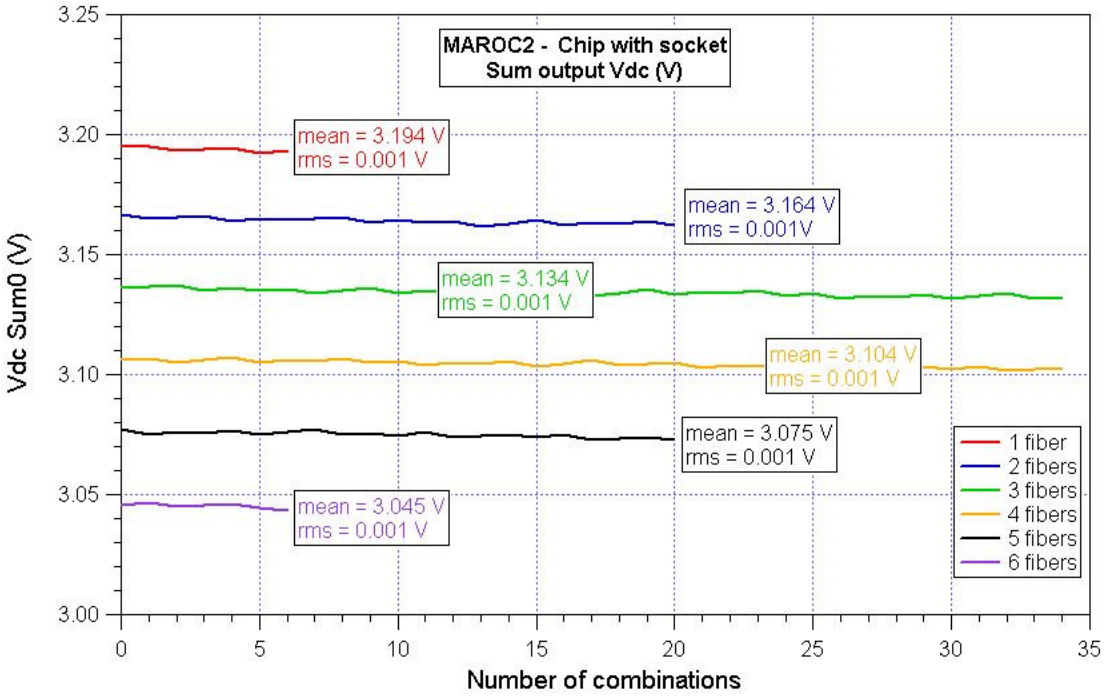


Figure 7: The DC voltage of one sum output versus the number of fiber.

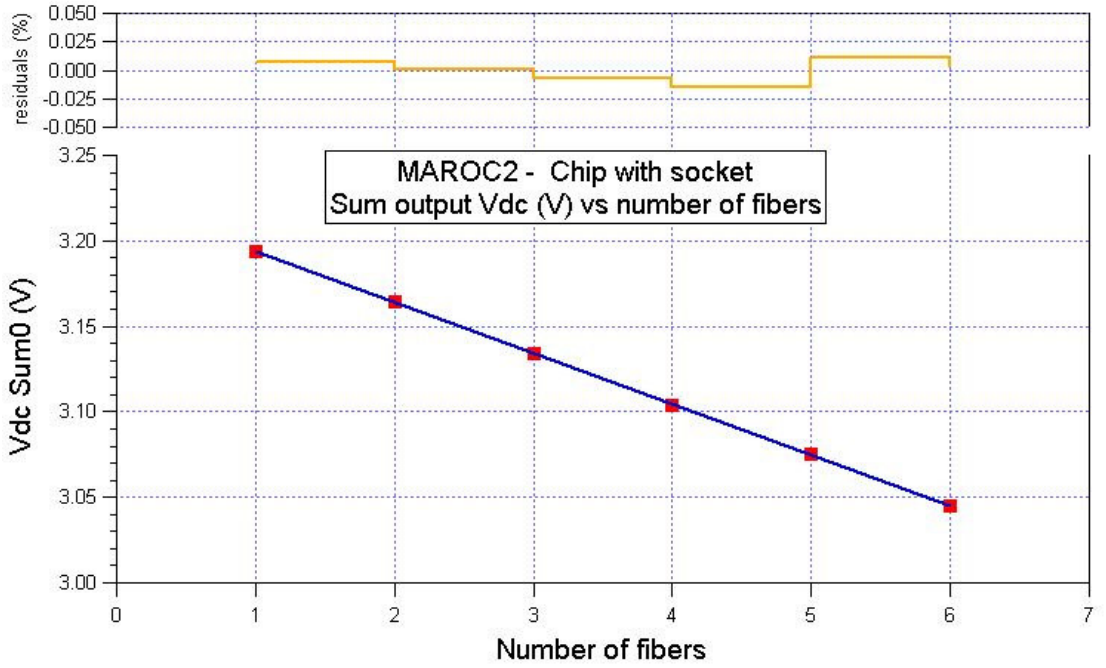


Figure 8: The DC voltage linearity versus the number of fiber

➢ Pulse measurements

Figure 9 shows sum output waveforms for different number of fibers summed. The input signal was the same for all 7 channels. From figure 10 we can see that there is a nice linearity of the maximal amplitude.

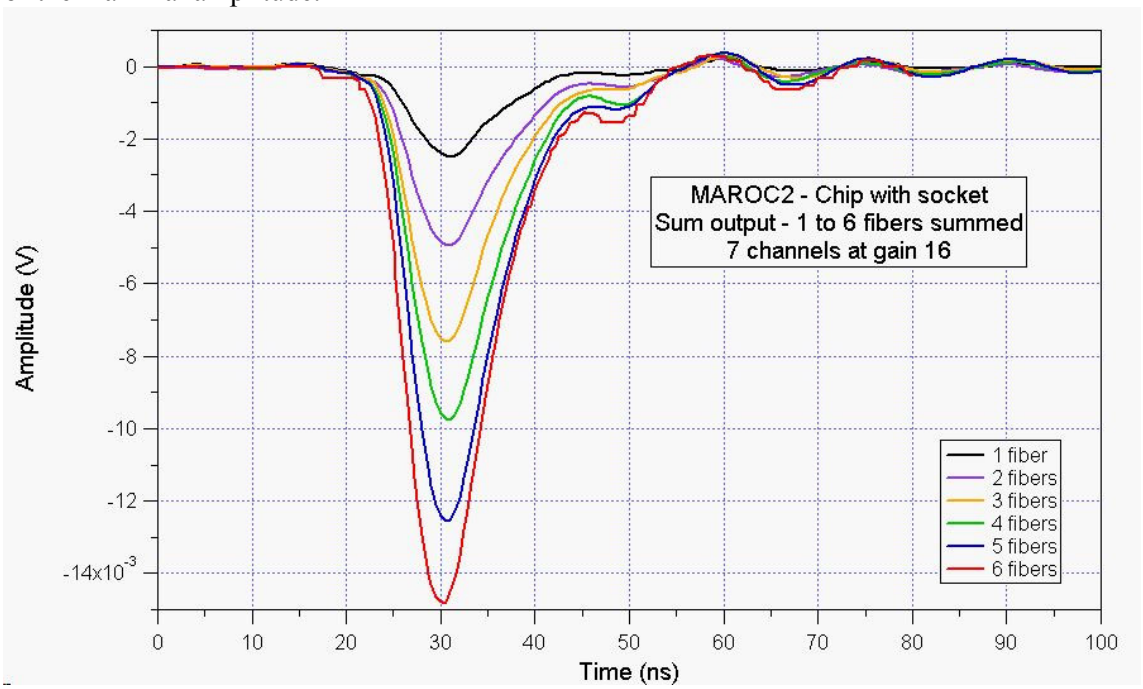


Figure 9: Sum waveforms versus the number of fiber

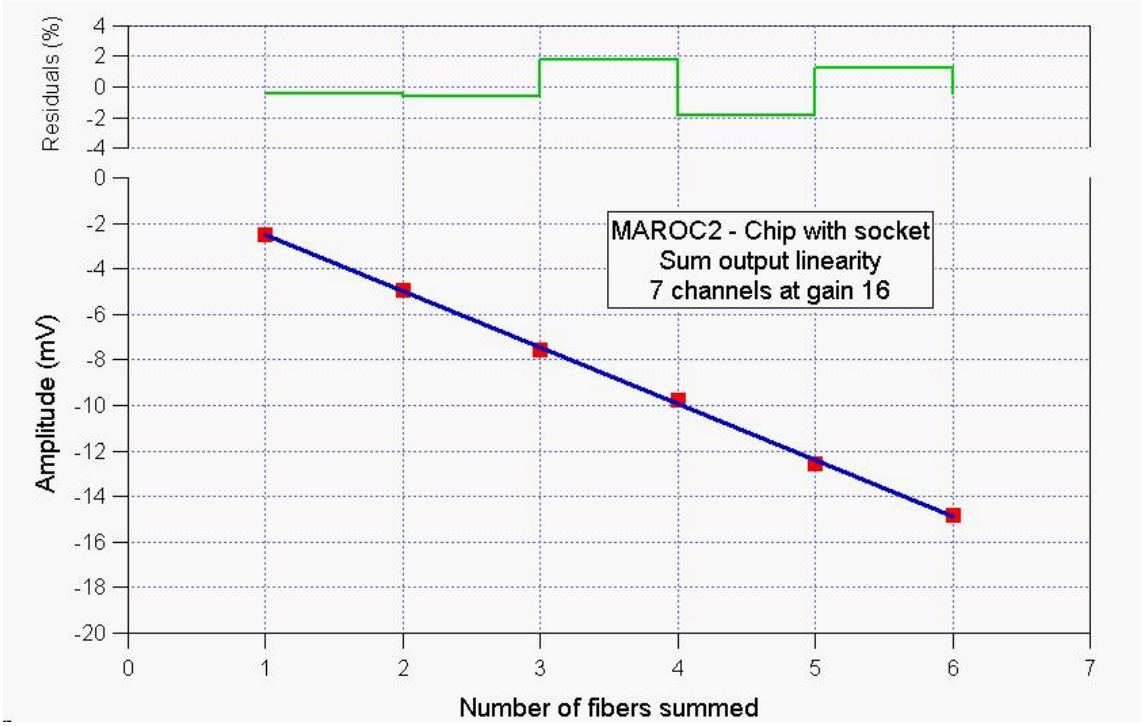


Figure 10: The sum linearity versus the number of fiber

4. Slow channel

4.a. Principe

The preamplifier signal goes to slow channel thank to a NMOS current mirror.

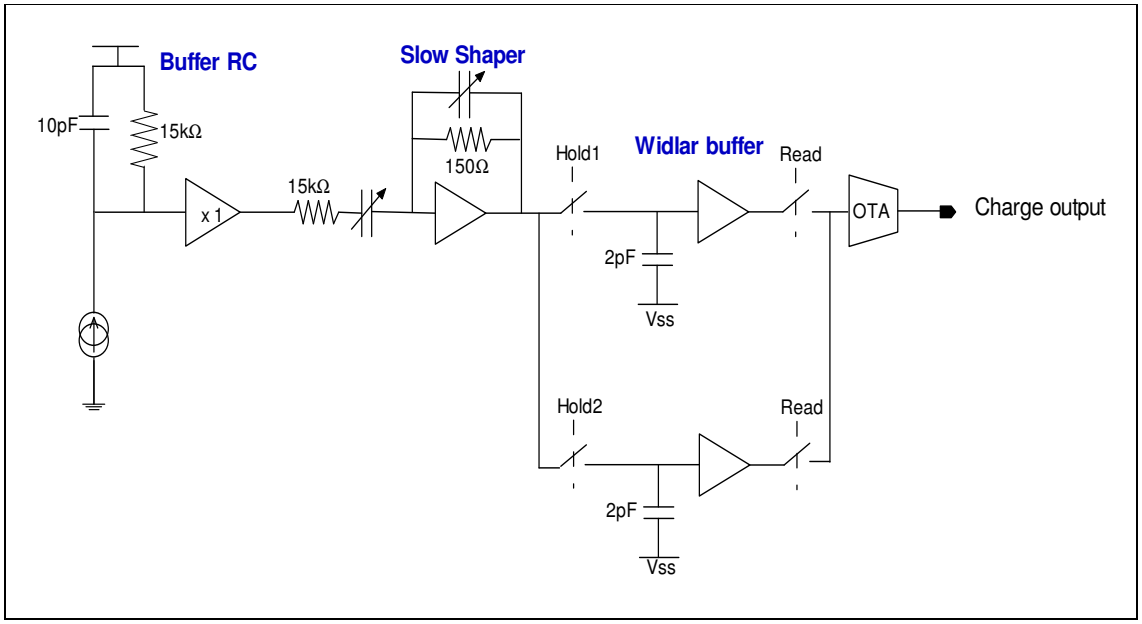


Figure 11: Slow channel schematic

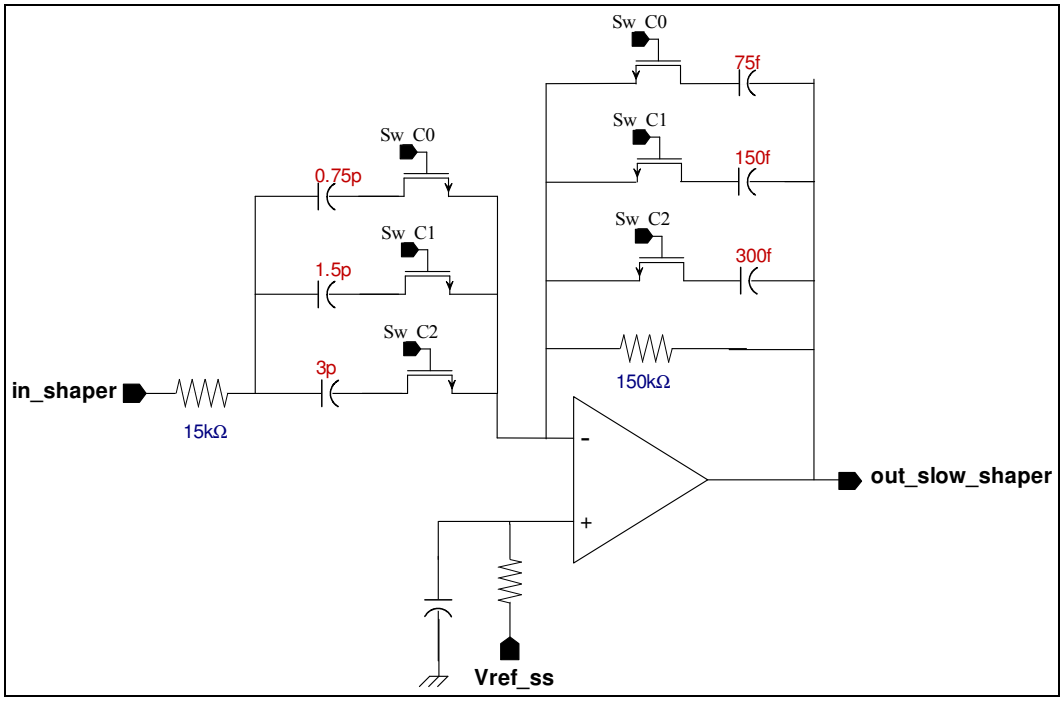


Figure 12: Slow shaper schematic

Figure 12 represents the slow shaper schematic. There are 3 feedback capacitors, common for the 64 channels, that can be switched on and off independently.

Switch configuration			Feedback Capacitance
Capa SW_C2=300fF	Capa SW_C1=150fF	Capa SW_C0=75fF	300fF
OFF	OFF	OFF	525 fF
OFF	OFF	ON	450 fF
OFF	ON	OFF	375 fF
OFF	ON	ON	300fF
ON	OFF	OFF	225fF
ON	OFF	ON	150fF
ON	ON	OFF	75fF
ON	ON	ON	0fF

4.b. Measurements

➢ DC measurements

Figure 13 represents the charge output pedestal as a function of the channel number for both track and hold. The dispersion is very small (~ 1 ‰). Figure 14 shows that the stability over time is nice (variation < 1 ‰).

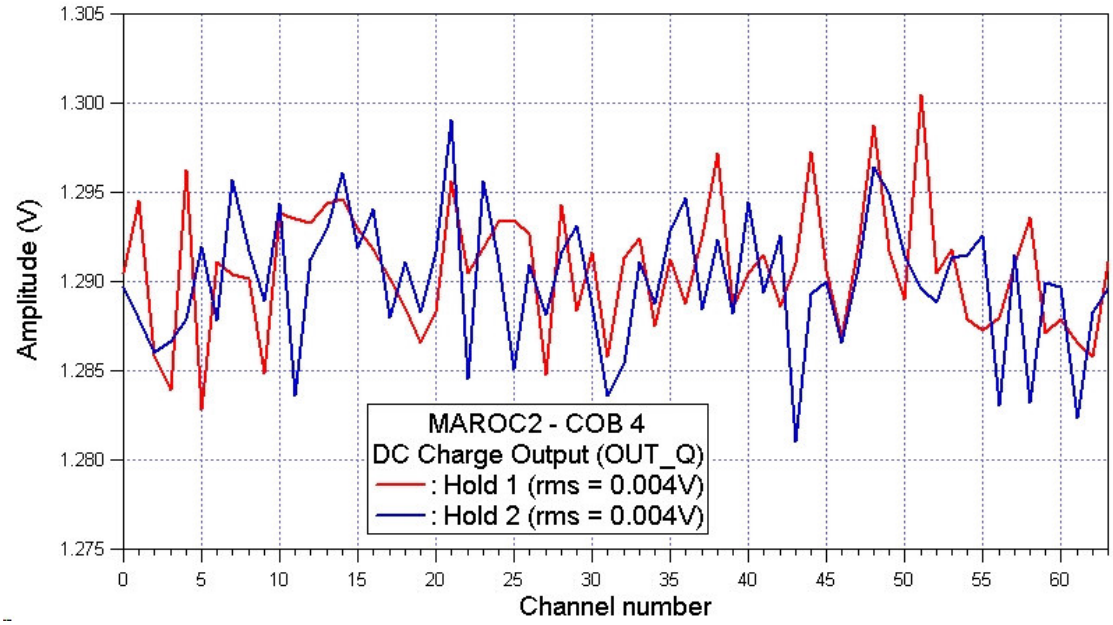


Figure 13: The DC charge output for each channel

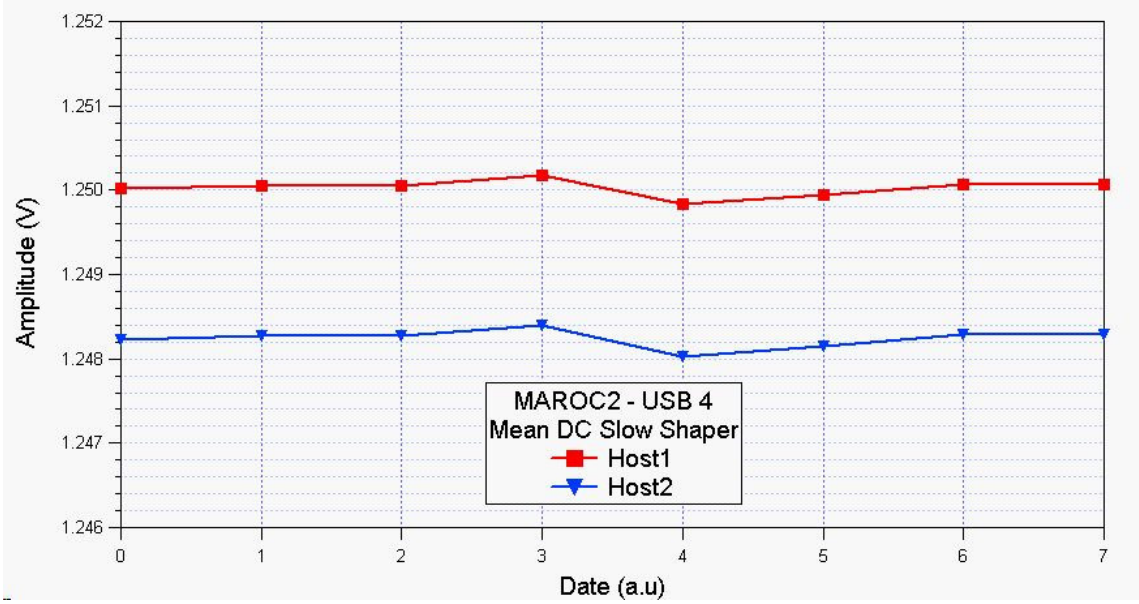


Figure 14: DC charge output stability versus time

The test board used for the measurements has an ADC which allows charge measurement. Figure 15 represents the distribution of the pedestal measured with this external ADC for all channels and for both track and hold. Figure 16 gives an example of pedestal distribution for a single channel.

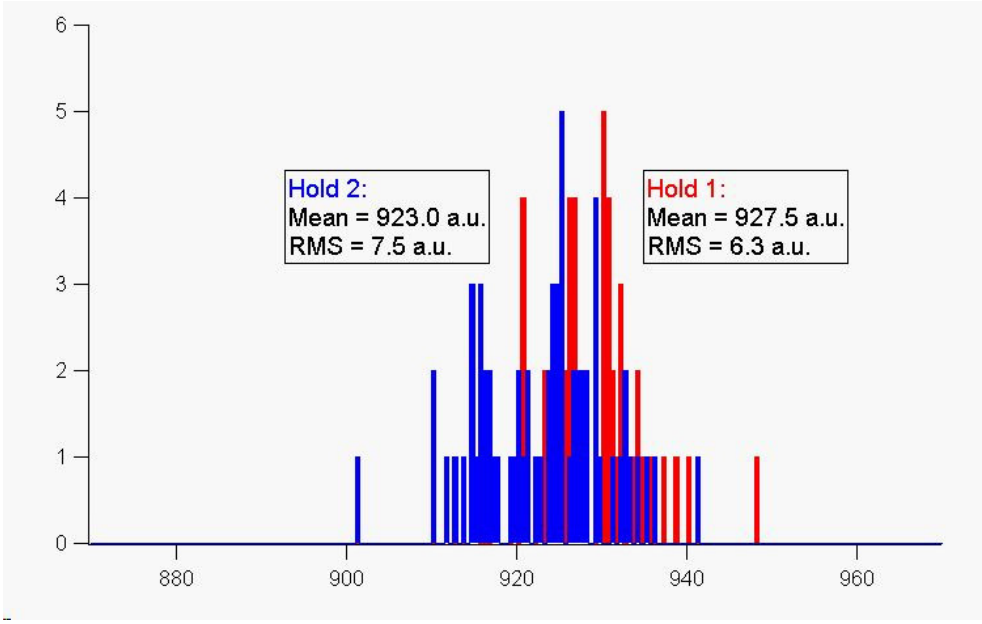


Figure 15: The pedestal distribution charge output for each channel with external12-bit ADC

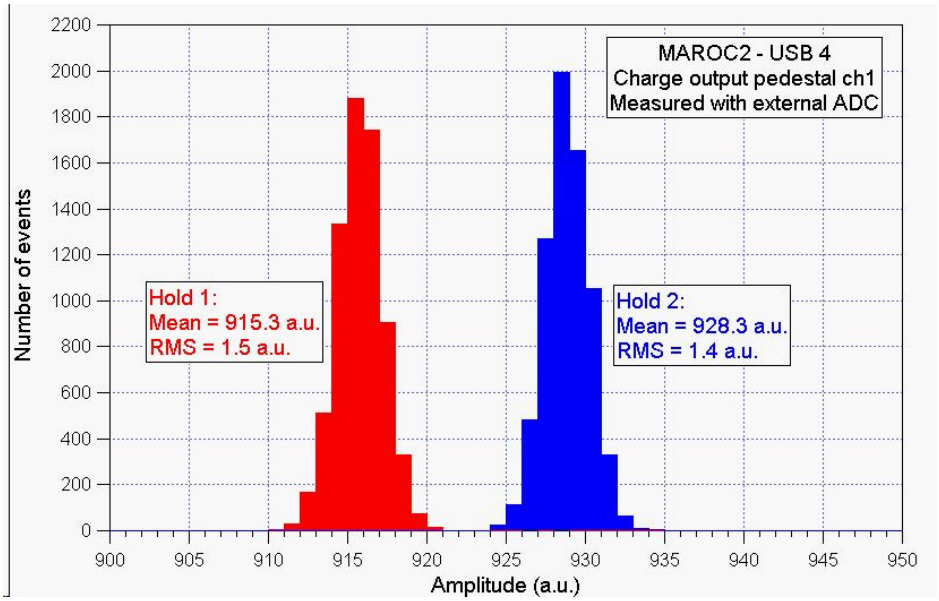


Figure 16: pedestal distribution charge output for channel 1 with external12-bit ADC

➢ Pulse measurements

Figure 17 shows the effect of the feedback capacitors on the slow shaper waveforms for a input charge of 300 fC.

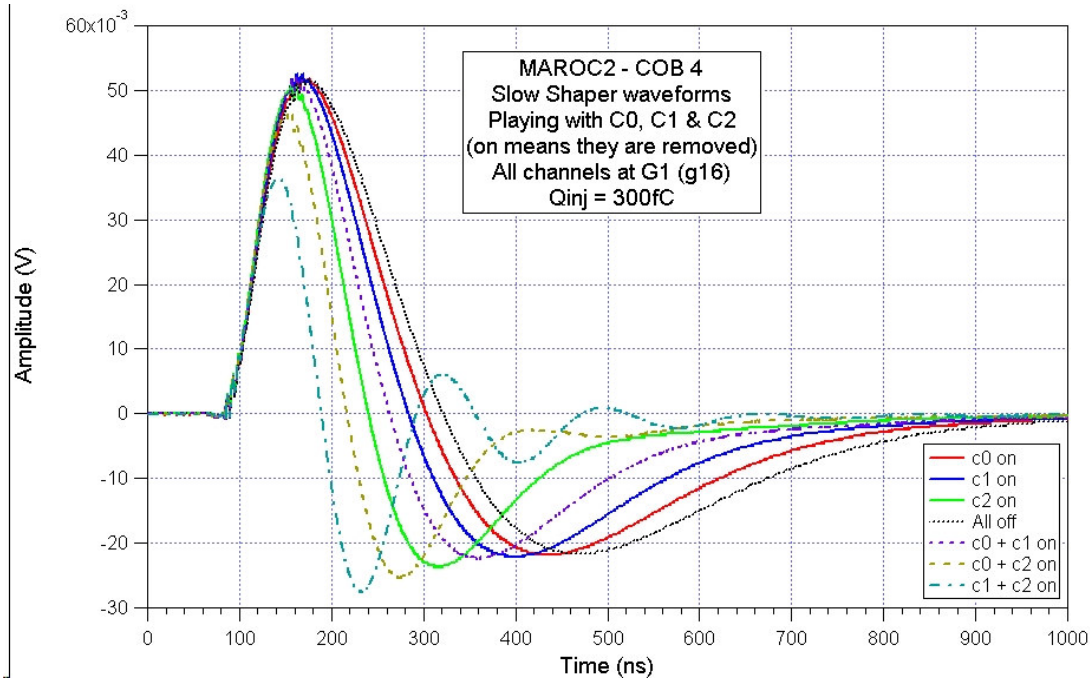


Figure 17: Slow shaper waveforms versus the feedback capacitor

Figure 18 shows the slow shaper waveforms for a fixed injected charge and variable gains.

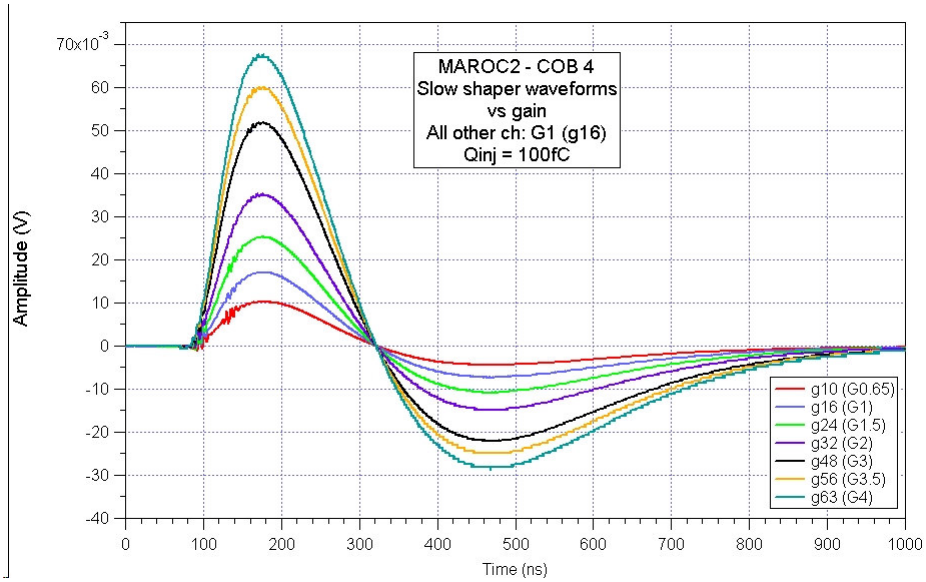


Figure 18: Slow shaper waveform versus the preamplifier gain value

Figure 19 shows the slow shaper waveforms for a fixed gain and variable injected charges in the range 50 fC to 50 pC. The linearity of the maximal amplitude as a function of the injected charge is given by the figure 20. The slow shaper gain obtained from this linear fit is equal to 160 mV/pC in agreement with MAROC1 measurements.

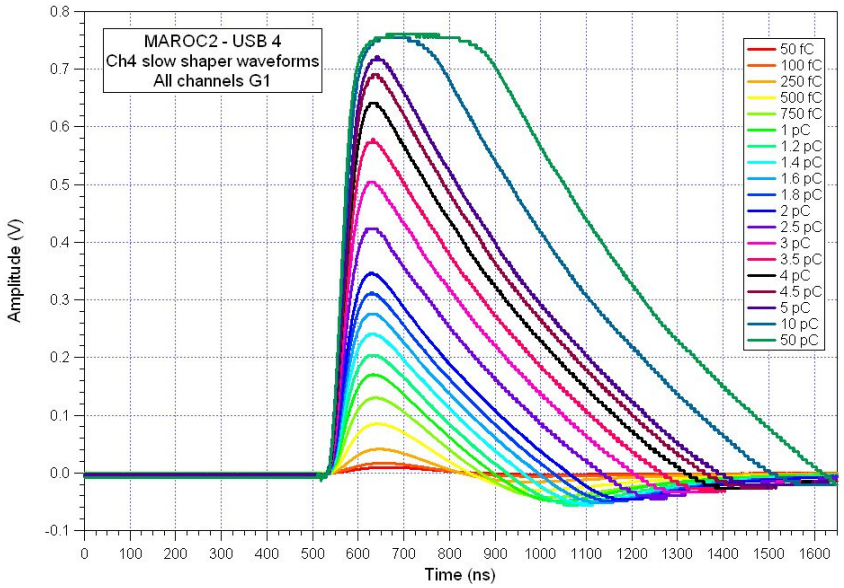


Figure 19: Slow shaper waveforms for different input charge

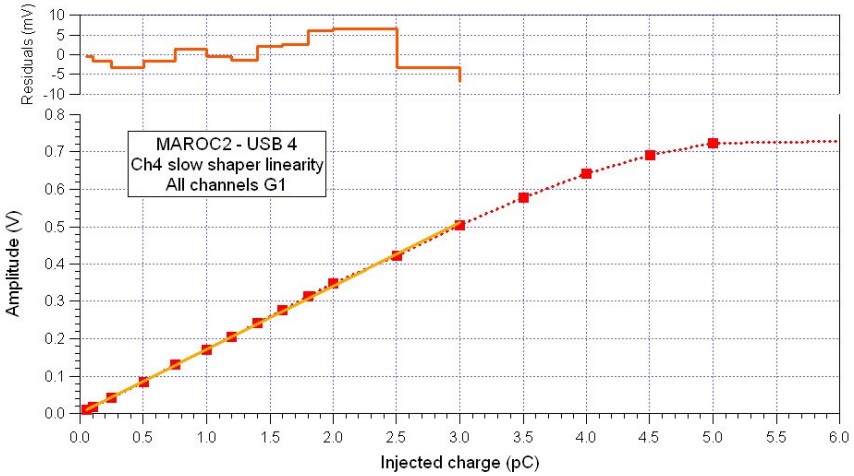


Figure 20: Linearity of the slow shaper

Figure 21 represents the distribution of the charge measured by the external ADC for different injected signals.

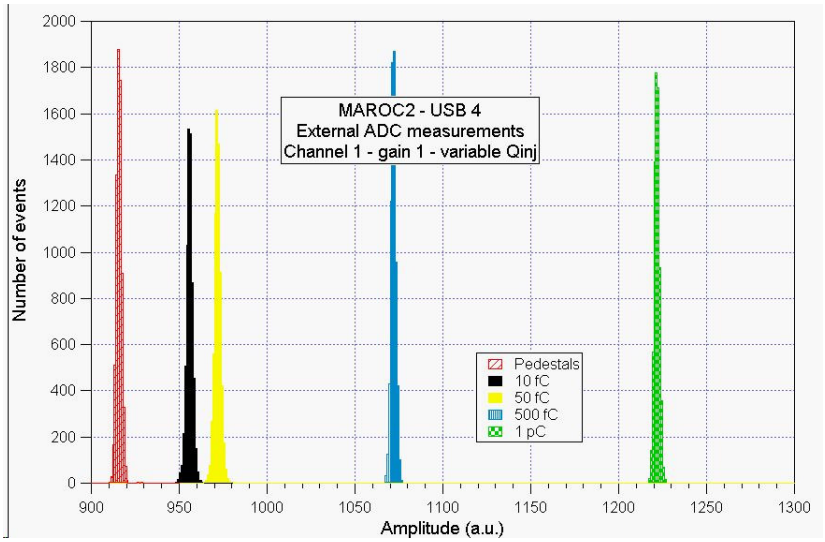


Figure 21: Slow shaper output for different input charge with the external 12-bit ADC

5. DAC

The 3 discrimator thresholds are set by 3 DACs. The simplified schematics exhibit 2 parts: One 16 bits thermometer DAC made of 16 switched identical current sources (iref_dac=20uA) for coarse tuning and 8 bits switched scaled current sources DAC for fine tuning.

Therefore 3*(16+8) bits must be sent serially to load whole DACs.

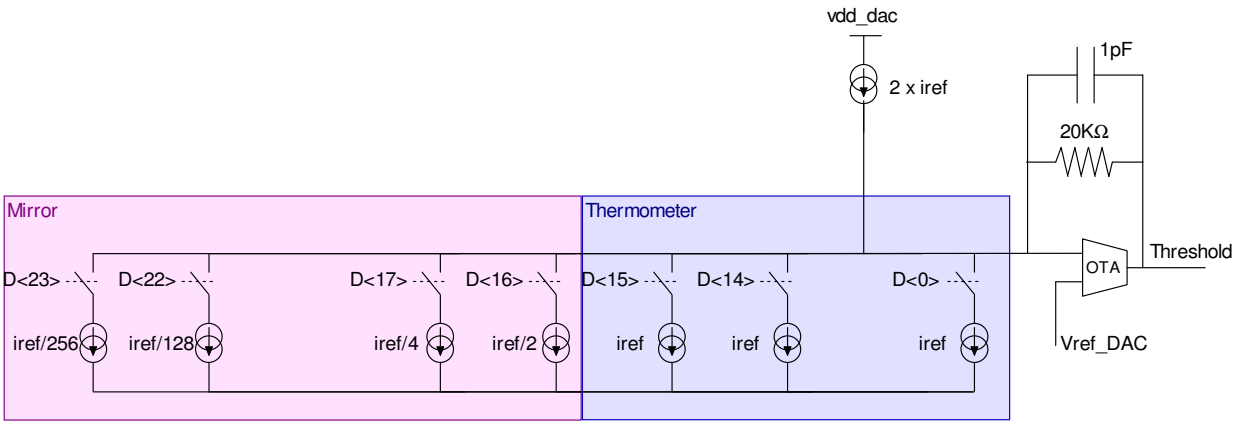


Figure 22: DAC principle

For example, when DAC value=0 we obtain a threshold=Vref_dac + 20k*2iref=0.63V

To create the threshold, the DAC current is converted into a voltage thanks to an OTA with a 20K feedback resistor. The iref_dac can be changed thanks to an external resistor. A 240kΩ resistor was added to decrease iref_dac, so for measurements, the iref_dac is about 15µA. The LSB of the DAC is about 0.7mV on 10 bits. After 10 bits, the DAC isn't linear anymore as one can see on figures 23-25.

The threshold set for the discriminator used for the Bipolar Fast Shaper is about 2V and for the Unipolar Fast Shaper is about 1.15V.

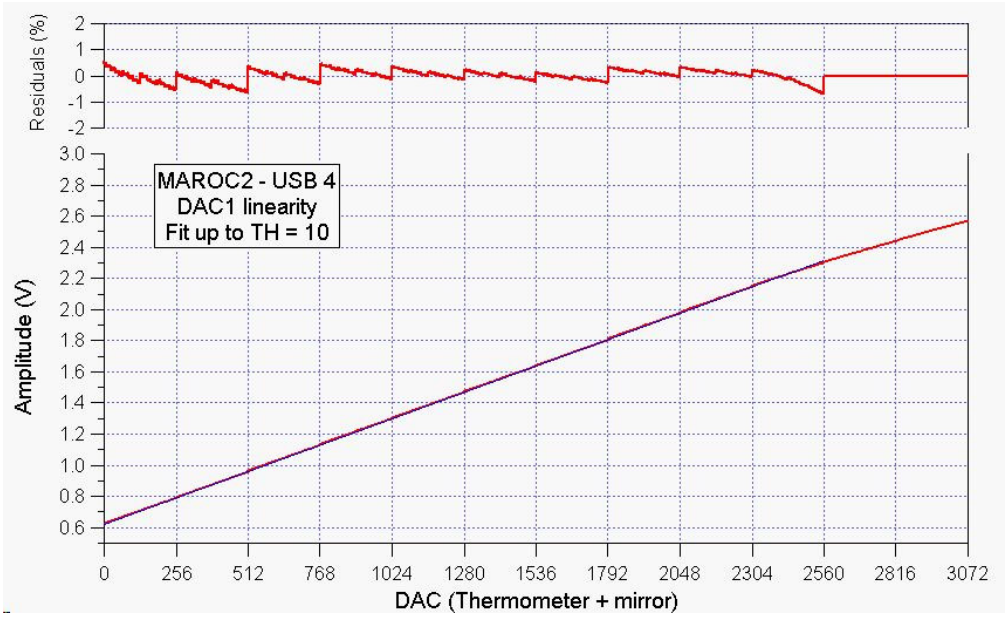


Figure 23: DAC1 linearity

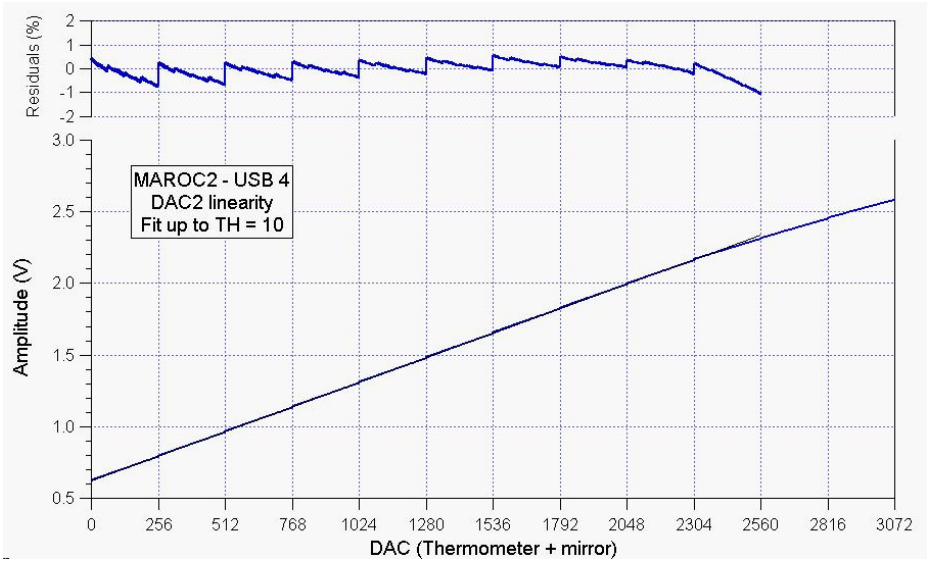


Figure 24: DAC2 linearity

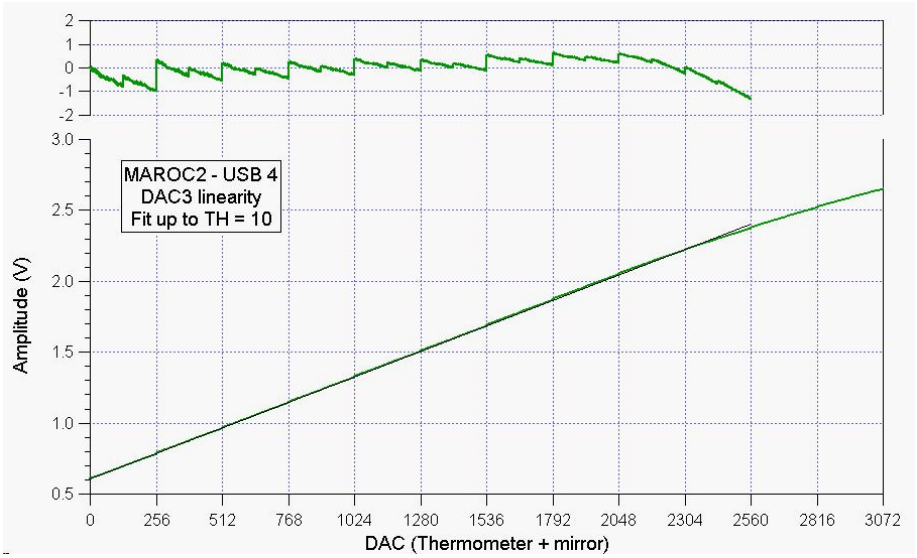


Figure 25: DAC3 linearity

6. Fast channel

6.a. Schematic

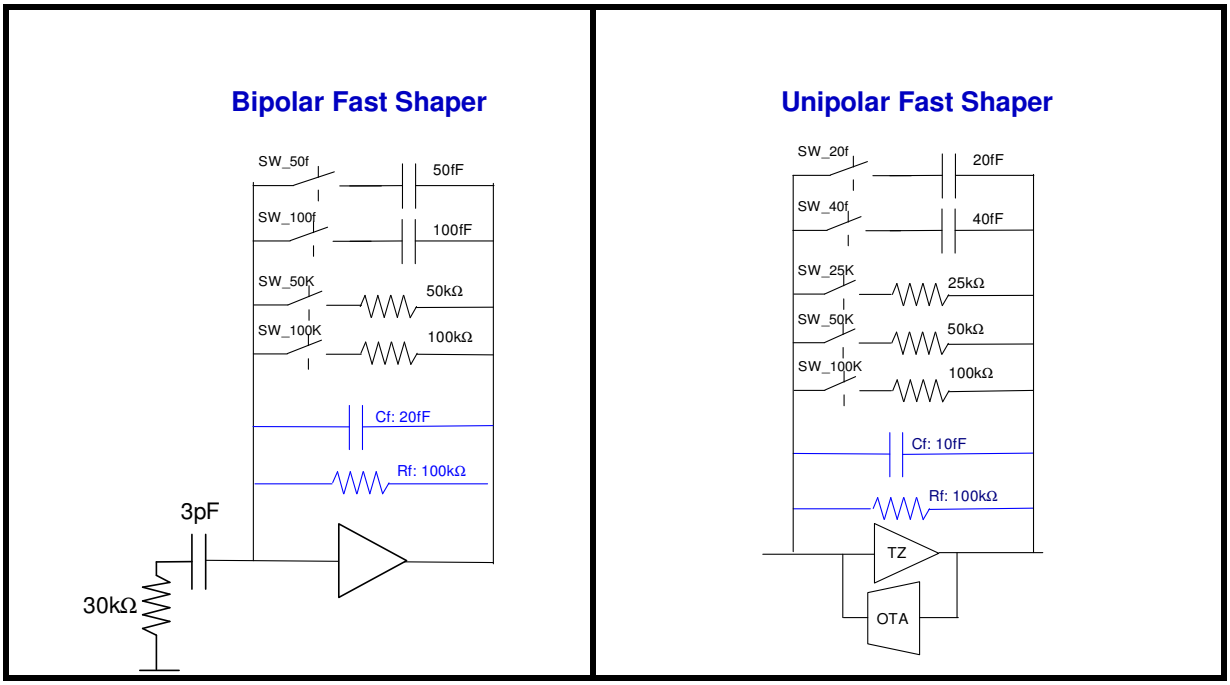


Figure 26: Fast Shapers schematics

The bipolar fast shaper is a CRRC shaper built around a PMOS differential pair with a W/L=60/1 to minimise the offset which must be kept small compared to the 0.3 pe- threshold of the discriminator.

6.b. Measurements

➢ DC measurements

Figures 27 and 28 represent respectively the evolution of the bipolar and unipolar fast shaper pedestals as a function of the channel number. Figure 29 shows the distributions of the slow and fast shapers with a small dispersion (~1 ‰).

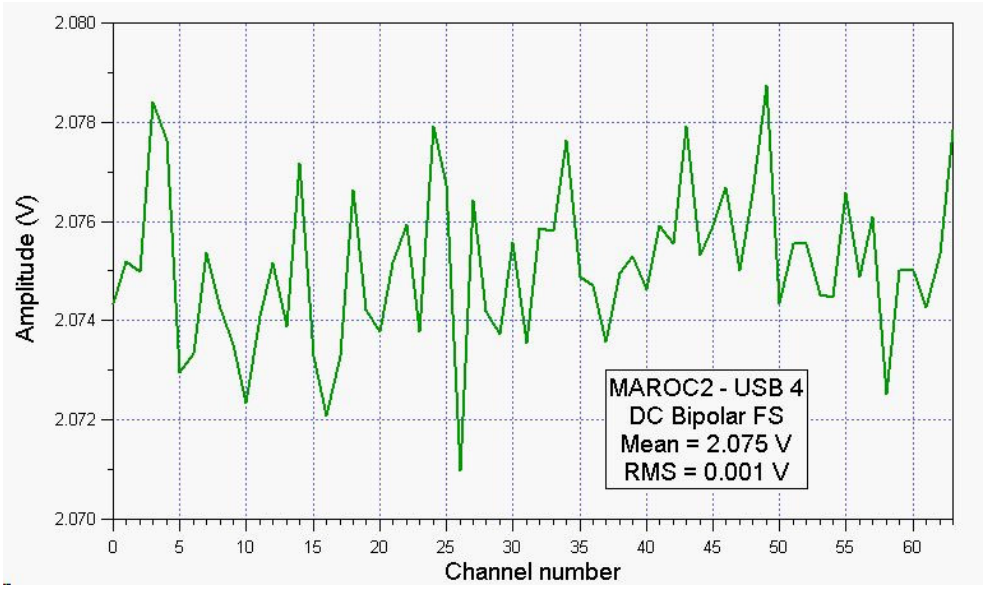


Figure 27: Bipolar Fast Shaper Pedestals

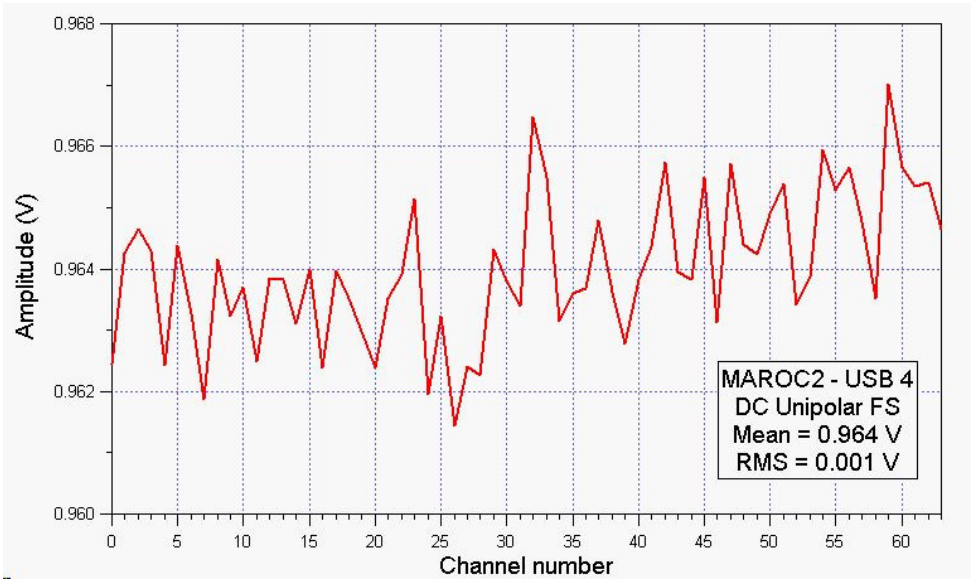


Figure 28: Unipolar Fast Shaper Pedestals

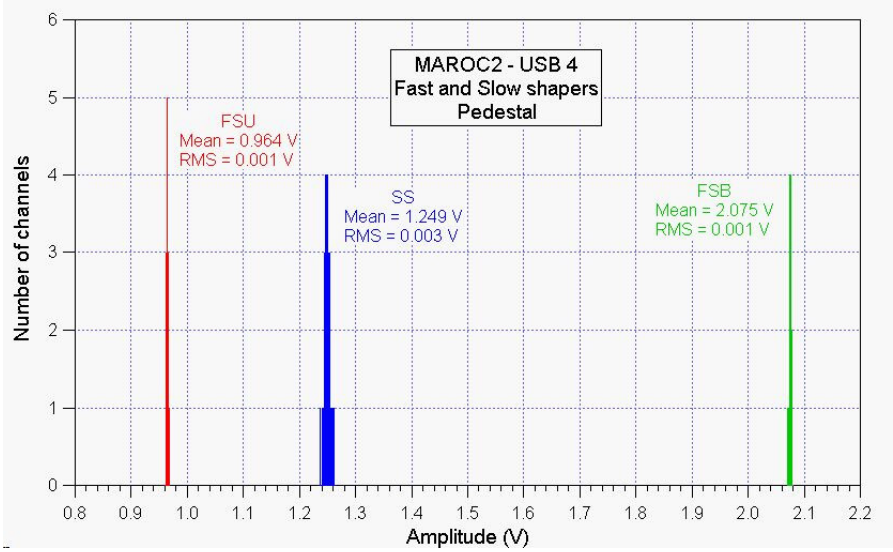


Figure 29: Fast and Slow Shapers Pedestals

Figure 30 shows that the fast shaper pedestals are stable with time, with a variation lesser than 1 ‰.

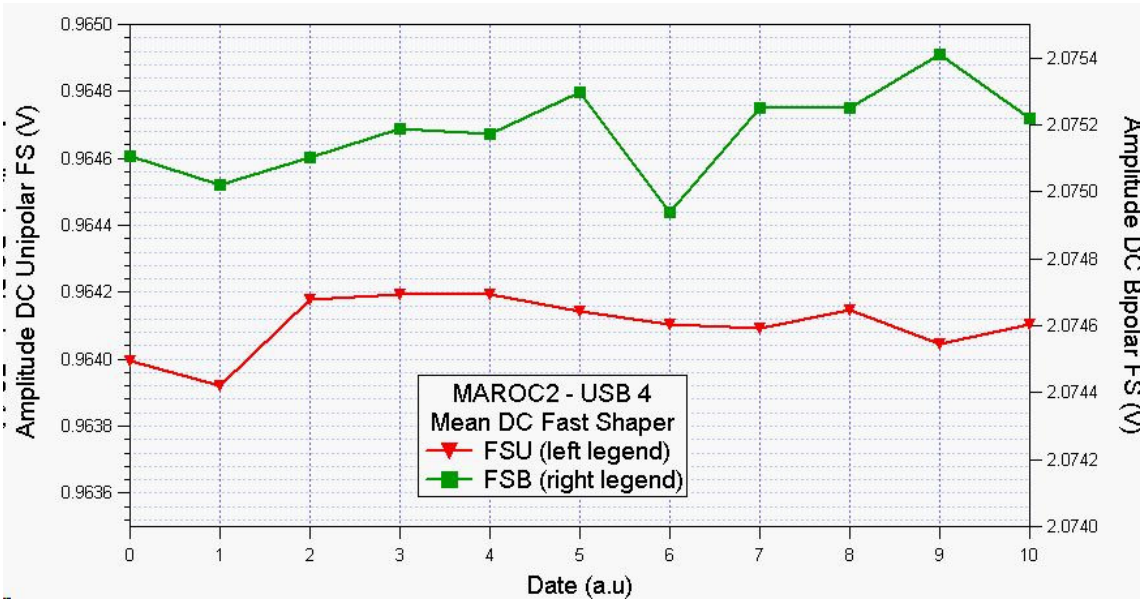


Figure 30: DC Fast Shapers outputs stability versus time

7. S-curves

In order to check the trigger output performances, the Unipolar Fast shaper has been used with Cf=10fF and Rf=100kΩ.

Figure 31 shows the evolution of the trigger efficiency as a function of the injected charge for the 64 channels of MAROC2, all set at gain 1. The threshold was set to a fixed value which induces the S shape of the plot.

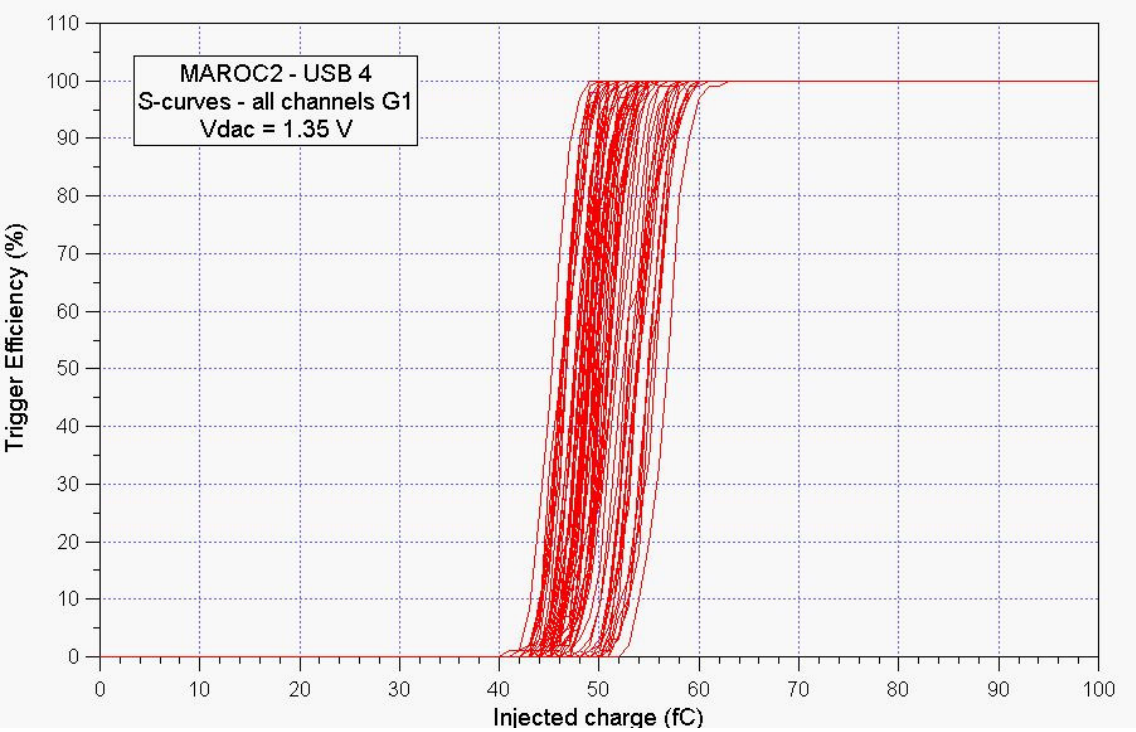


Figure 31: Scurve versus injected charge

We extracted the 50% trigger efficiency input charge from figure 31. Figure 32 shows the evolution of this point versus the channel number. There is a nice homogeneity.

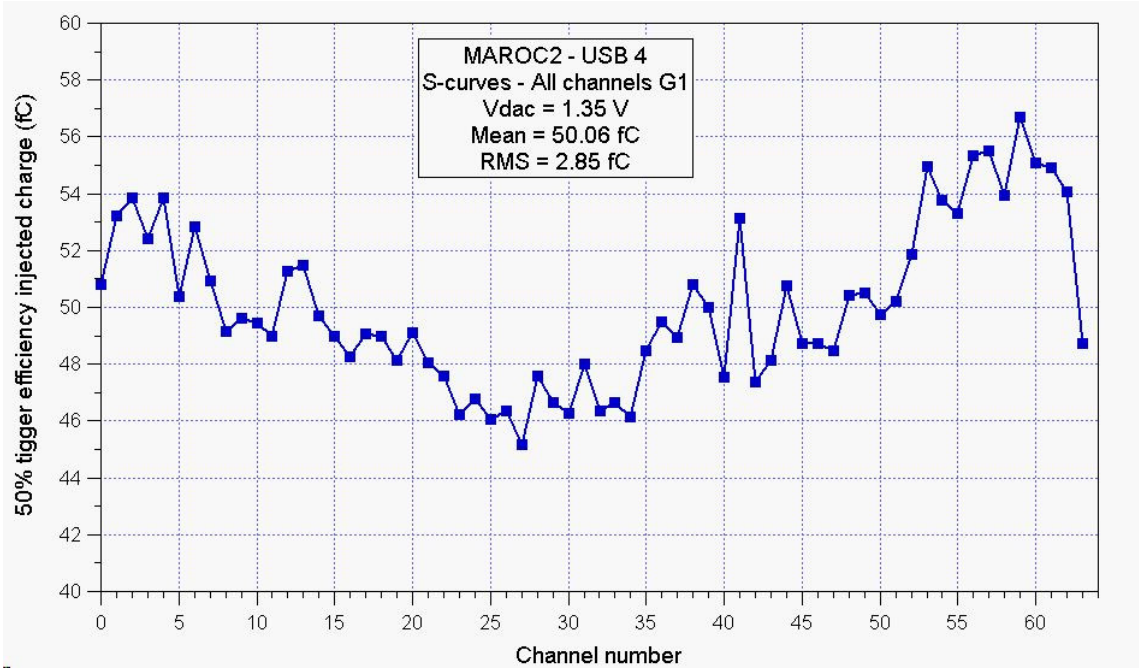


Figure 32: 50% trigger efficiency versus injected charge

The effect of the threshold on this type of s-curves was studied. Figure 33 represents the s-curves obtained for a single channel for 60 different DAC values. The evolution of the

50% trigger efficiency injected charge as a function of the threshold is given by the figure 34 and exhibits a linearity better that ± 1%. This linearity does not vary with the gain as figure 35 shows.

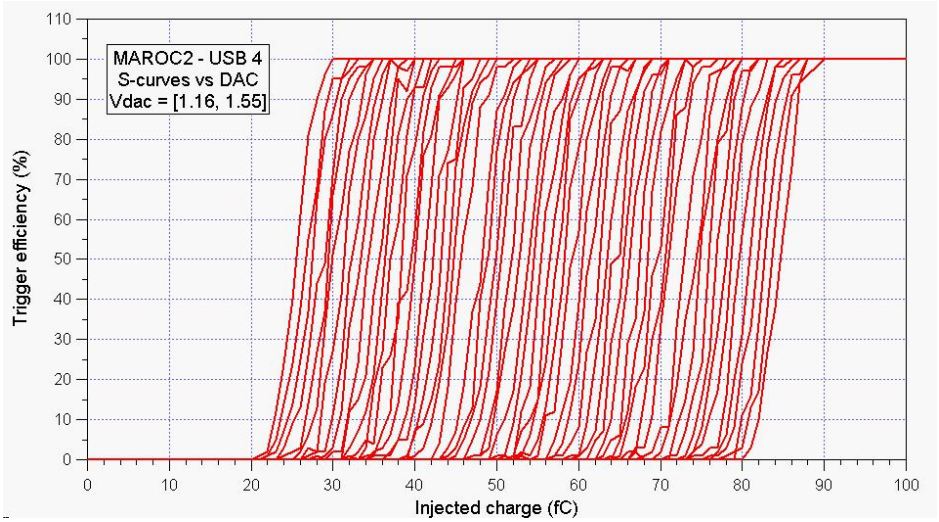


Figure 33: Scurve versus injected charge with different threshold

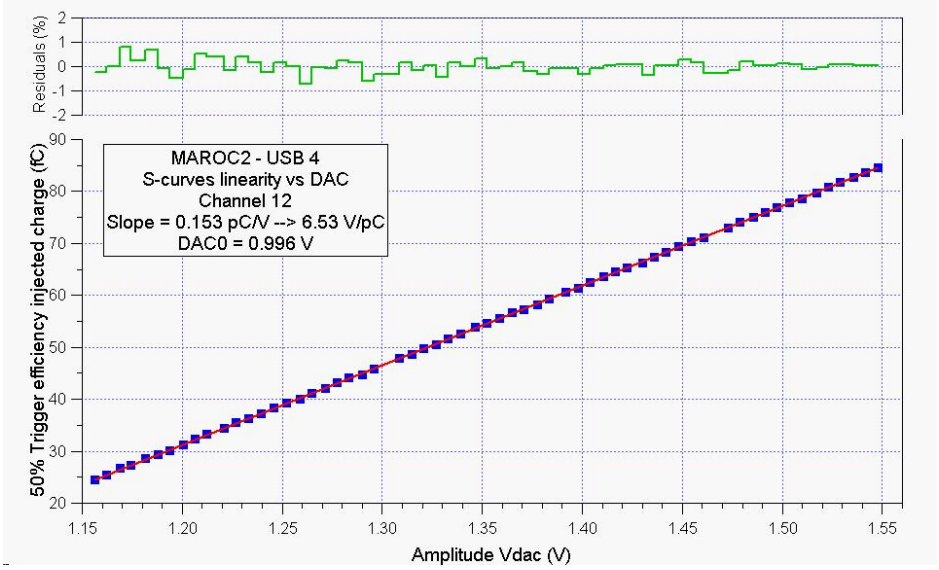


Figure 34: 50% trigger efficiency versus threshold for channel 12

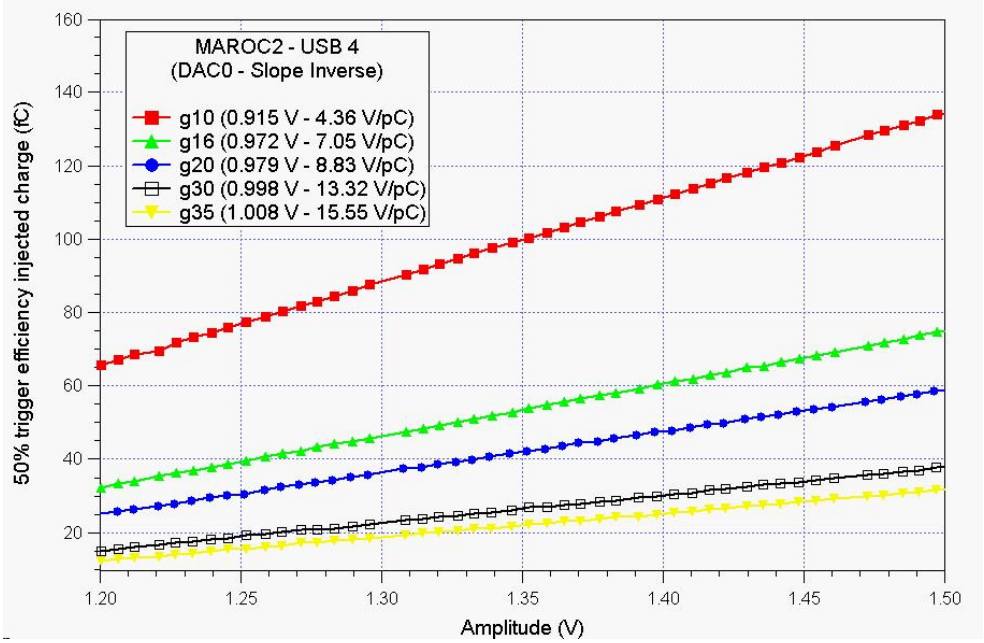


Figure 35: 50% trigger efficiency versus threshold for channel 12 for different preamplifier gains.

Figure 36 shows similar type of s-curves for different preamplifier gain values.

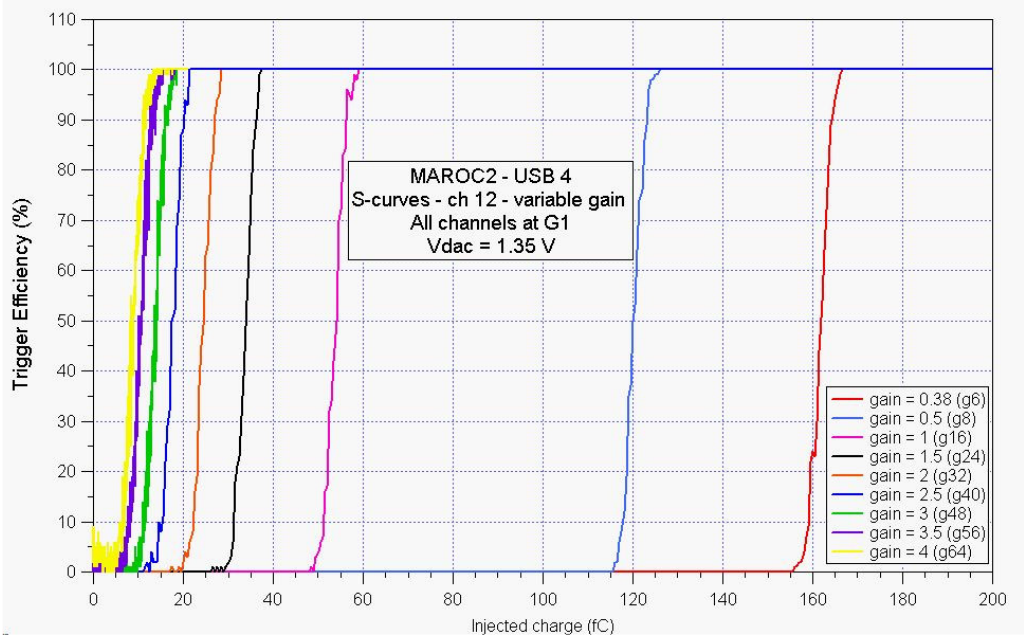


Figure 36: Scurve versus injected charge with different gain

Figure 37 represents the evolution of the trigger efficiency versus the DAC amplitude for different injected charges.

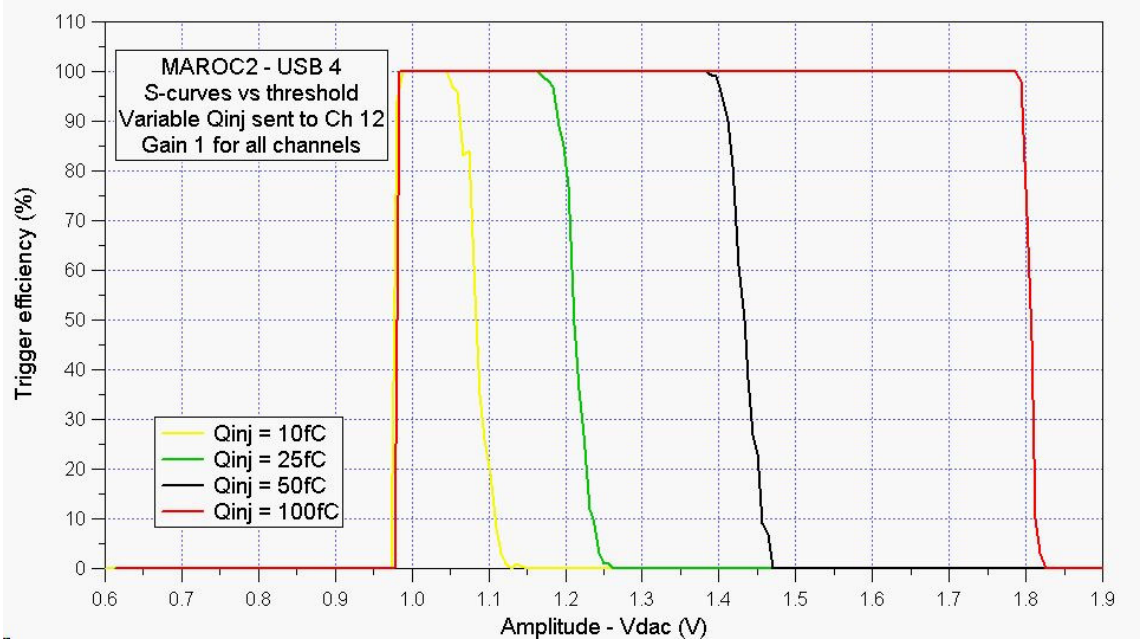


Figure 37: Scurve versus threshold for different injected charge

8. Cross talk

In order to study the cross talk, a variable signal was sent to a central channel (8 in our example) and output trigger from this channel and the two neighbours (7 and 9) was recorded. The threshold was set in order to get 100 % trigger efficiency at 50 fC for the central channel. The maximal signal delivered was 10 pC and the gain was 1 for all channels.

Figure 38 represents the s-curves obtained for the three channels, on the full input charge range ([0-10] pC). No trigger signals were seen before 1.7 pC for the two neighbouring channels leading to a cross talk smaller than 3%, a bit larger than what is expected. For understanding the s-curves of the channels 7 and 9 are also given for three other preamplifier gains (0.75, 0.5 and 0.25) on the Figure 38. As one can see the cross-talk is sensitive to the gain value which means that it comes from the test board, the preamplifier or the input since the gain is applied at an early stage of the ASIC.

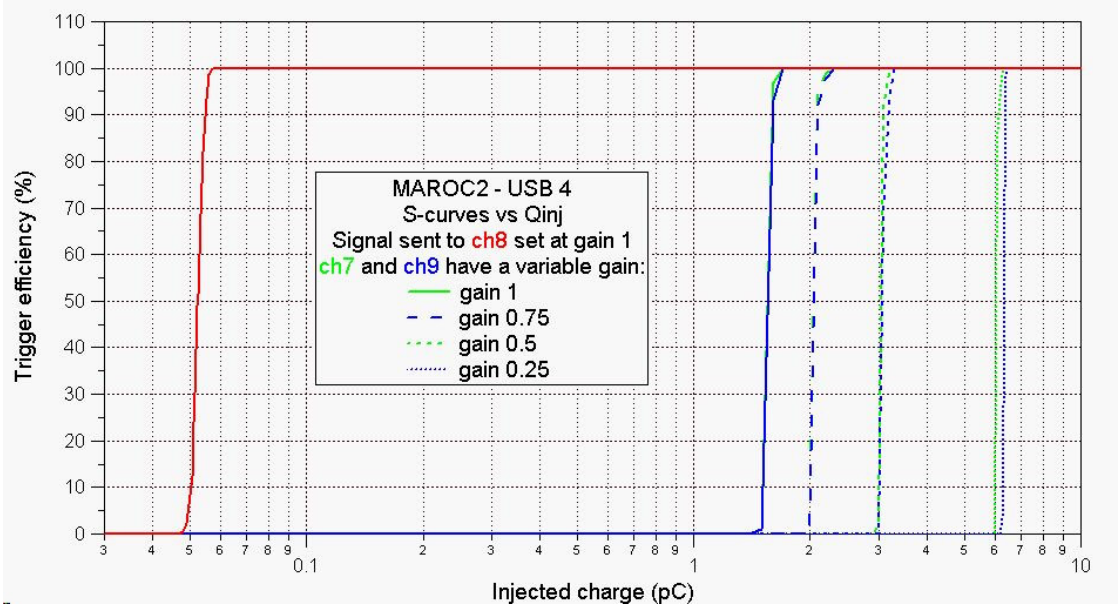


Figure 38: S-curves for channel 9 at gain 1 and its two neighbours for four different gains in the range [0.25, 1.].

Even if the cross-talk is larger than expected, we can be confident by the fact that is only appears above large values of injected charge. Figure 39 gives the distribution of the injected signal, in photo-electrons, for which cross-talk appears for 64 channels. For most of them this signal is greater than 10 photo-electrons.

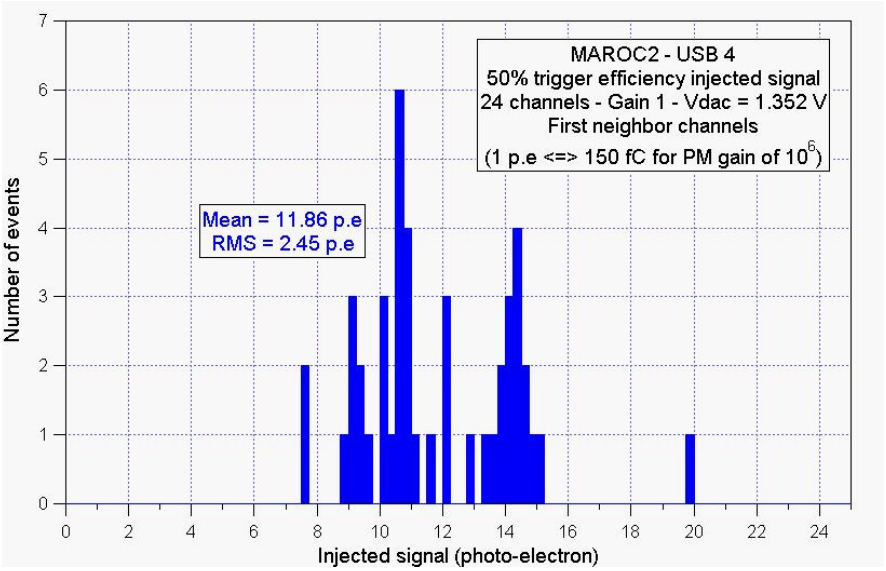


Figure 39: Injected charge for which the cross talk appears.

In the case of the ATLAS Luminometer, which the main application using MAROC2, this corresponds to the queue of the expected signal distribution. Indeed the expected signal from the fibers is supposed to be Poisson distributed, with a mean at 3 to 5 p.e depending on the type of fiber. By convoluting the Poisson distribution with the s-curve of each channel and looking at the ratios of the integrals we obtained a more physic approach of the cross-talk with an average value closer to the requirements (1 %, see figure 40).

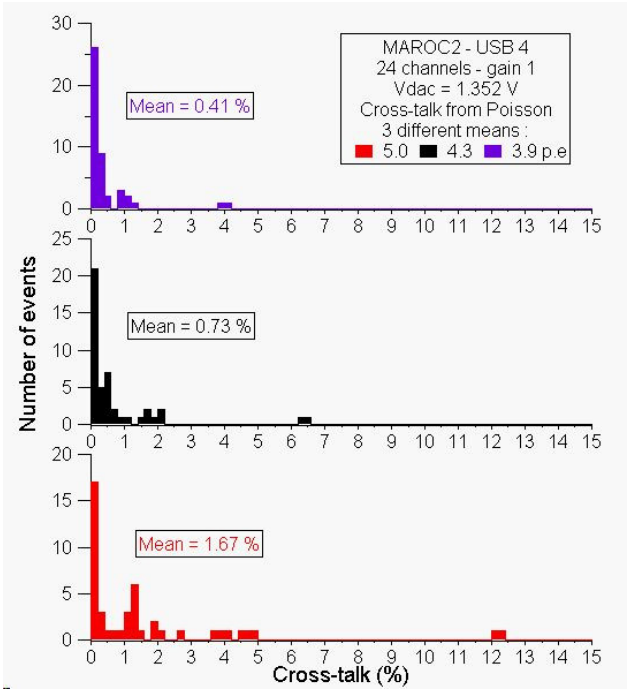


Figure 40: Cross talk distribution for different Poisson distributions.

Figure 41 represents the waveforms of the channel 8 and its neighbours for an injected charge of 2 pC. The amplitude of the channels 7 and 9 is multiplied by 100. The calculation of maximum ratio gives a cross-talk lesser than 1%.

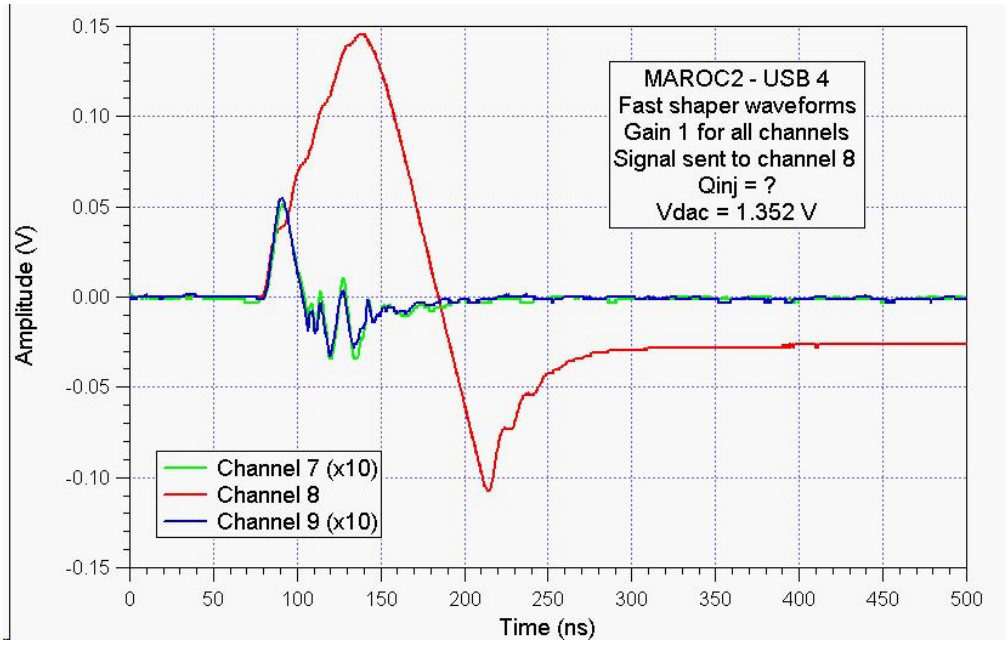


Figure 41: Slow shaper waveforms for channel 8 and its two neighbours for an injected charge of 2 pC on the central channel.

III.TEST BOARD (05/06/06)

1. MAROC2 chip Input/Output

1.a. Pinout Table

pin number	pin name	connect to	DC voltage	Current	Bias
1	in<3>	detector	0.8V		
29	in<31>	detector			
30	**gnd_PA**	**gnda**			
31	in<32>	detector			
60	in<61>	detector			
61	IN<62>	detector			
	IN<63>	detector			
	gnd_PA	**gnda**			
	D_G	D_Gain			TTL 3.3 from FPGA
65	**vssa**	**gnda**			
	RST_G*	RST_Gain*	3.5V		TTL 3.3 from FPGA
	vdd_PA	**vdda**		23mA	
	CK_G	CK_Gain			TTL 3.3 from FPGA
	vb_PA	100nF to gnd	2.5V	7mA	150Ω vdd_PA
70	ibi_SS	13k to gnd	0.9V	50uA	56kΩ vdd_SS
	vcasc_PMOS	NC	1.5V		2kΩ vdd_PA // 1,5kΩ gnd_PMOS
	ibo_SS	NC	0.9V	50uA	56kΩ vdd_SS
	gnd_NMOS	**gnda**			
	ib_BUF	NC	0.8V	50uA	50kΩ vdd_BUF2
75	vref_SS	100nF to gnda	1.4V		2,1kΩ vdd_BG // 1,4kΩ gnd_SS
	Qbuf_R	Q_Read			TTL 3.3 to FPGA
	gnd_H	**gnda**			
	CK_R	CK_Read			TTL 3.3 from FPGA
	Hold1	Hold1 (TTL 3.3 from FPGA)	3.5V		
80	RST_R*	RST_Read*	3.5V		TTL 3.3 from FPGA
	Hold2	Hold2 (TTL 3.3 from FPGA)	3.5V		
	D_R	D_Read			TTL 3.3 from FPGA
	vdd_H	**vdda**		3.6mA	
	ib_DAC	NC	1.3V	700uA	3kΩ vdd_DAC

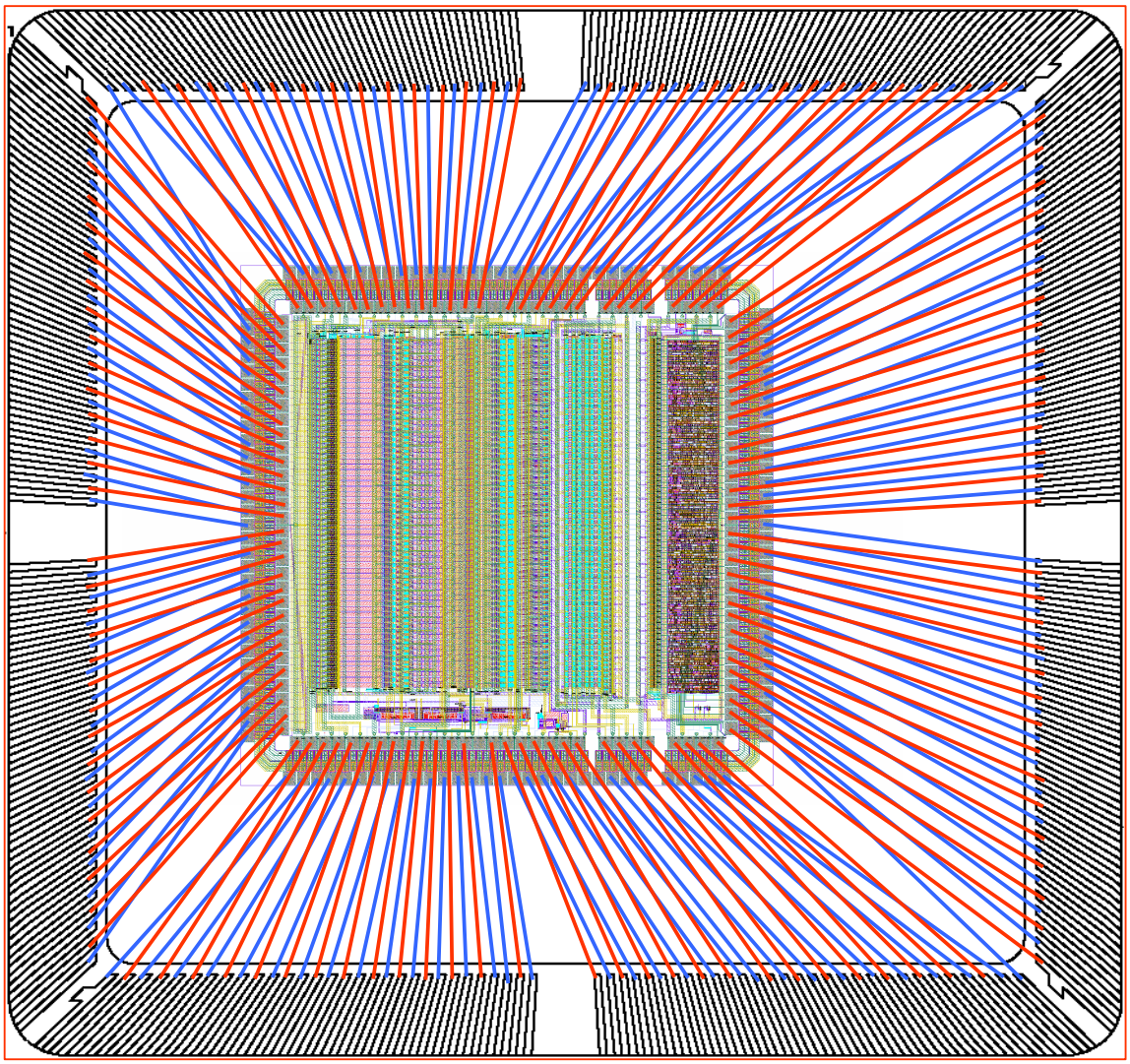
85	**gnd_DAC**	**gnda**			
	iref_DAC	240k to vdda		11uA	220kΩ gnd_DAC
	vdd_DAC	**vdda**			
NC	vcasc_DAC	NC			2,5kΩ vdd_DAC // 1kW gnd_DAC
	vref_DAC	100nF to gnda	1V		2,5kΩ vdd_BG // 1kW gnd_DAC
	ibi_TZ	15k to vdda+100nF to gnd	2.23V	65uA	34kΩ gnd_FSU
90	**vdd_FSU1**	**vdda**		1.2mA	
	G_diode	NC	1V		220kΩ gnd_DAC
	E_FSU	**gnda**			
	ibo_TZ	10k to vdda+100nF to gnd	0.96V	65uA	40kΩ vdd_FSU2
	vcasc_FSU	NC	1V		2,5kΩ vdd_FSU1 // 1kΩ gnd_FSU
95	vslope	100nF to gnda	800mV		154kΩ vdd_BG // 46kΩ gnd_Wilk
	vref_FSU	100nF to gnda	1V		2,5kΩ vdd_BG // 1kΩ gnd_FSU
	Ramp	Test output			
	gnd_Wilk	**gnda**			
	vref_Ramp	100nF to gnda	1.3V		126kΩ vdd_BG // 74kΩ gnd_Wilk
100	**vdd_Wilk**	**vdda**		800uA	
	ib_integ	NC		50uA	15kΩ gnd_Wilk
	vssa	**gnda**			
	vssm	**gnda**			
	ibi_D	NC	0.96V	65uA	40kΩ vdd_D1
105	**vdd_D1**	**vdda**		6mA	
	ibm_D	NC	2.34V	23uA	100kΩ gnd_D
	vdd_D2	**vdda**		11mA	
	ibo_D	22k to vdda+100nF to gnd	2.6V	25uA	100kΩ gnd_D
	gnd_D	**gnda**			
110	**vdd_D3**	**vdda**		8mA	
	vssd	**gndd**			
	gndd	**gndd**			
	vddd2	**vddd**		35u	
	out_ADC	ADC data output			HSTL to FPGA
115	ADC_DAV	ADC Data Valid			HSTL to FPGA
	start_ADC*	start acquisition			TTL 3.3 from FPGA
	ADC_CK_ON*	enable ADC clock	3.5V		TTL 3.3 fromFPGA
	out<63>	HSTL to FPGA			
	out<62>	HSTL to FPGA			
120	out<61>	HSTL to FPGA			
121	out<60>	HSTL to FPGA			
150	**vssd**	**gndd**			
180	out<2>	HSTL to FPGA			
181	out<1>	HSTL to FPGA			

	out<0>	HSTL to FPGA			
	gndd	**gndd**			
	RST*	ADC reset (TTL 3.3 from FPGA)			
185	**vddd**	**vddd**		2m	
	CK80M*	encoder clock and ADC clock			LVDS from FPGA
	vref_HSTL	600mV reference voltage + 100nF to gnda	600mV		
	CK_80M	encoder clock and ADC clock			LVDS from FPGA
	vssd	**gndd**			
190	cmd_HSTL	NC	3.5V		
	ibo_Dwilk	NC			
	vth2	100nF to gnda			
	vdd_D1	**vdda**		6mA	
	vth1	100nF to gnda			
195	**gnd_D**	**gnda**			
	vth0	100nF to gnda			
	vssm	**gnda**			
	vssa	**gnda**			
	Qbuf_G	Q_Gain			TTL 3,3 to FPGA
200	**vdd_BG**	**Reference voltage (3,3V)**		22mA	
	DC_FS	test output	1V // 2,2V		
	gnd_FSU	**gnda**			
	ib_OTA	NC (FSU OTA bias)	2.7V	5u	500kΩ gnd_FSU
	vdd_FSU2	**vdda**		12mA	
205	ibo_FSB	NC	2V	40uA	50kΩ gnd_FB1
	gnd_FSB1	**gnda**			
	ibi_FSB	NC	2.4V	47uA	50kΩ gnd_FB1
	vref_FSB	100nF to gnda	2.2V		1,3kΩ vdd_BG // 2,2kΩ gnd_FB1
	ibo_W	NC	0.8V	25uA	100kΩ vdd_W
210	**vdd_FSB**	**vdda**		6mA	
NC	ibi_W	NC			50kΩ vdd_W
	gnd_FSB0	**gnda**			
	ib_SUM	NC	1V	500uA	5,6kΩ vdd_OTAQ
	EN_OTAQ	enable charge output (from FPGA)			
	SUM8	test point	2,1V		
215	out_Q	charge output	1,4V		
	SUM7	test point			
	gnd_CAPA	**gnda**			
	SUM6	test point			
	gnd_SS	**gnda**			
220	SUM5	test point			
	vdd_SS	**vdda**		17mA	
	SUM4	test point			

	vdd_BUF1	**vdda**		1.5mA	
	SUM3	test point			
225	**vdd_OTAQ**	**vdda**		15mA	
	SUM2	test point			
	gnd_OTAQ	**gnda**			
	SUM1	test point			
	vcasc_NMOS	NC	1.5V		2kΩ vdd_NMOS //1,5kΩ gnd_NMOS
230	SUM0	test point			
	gnd_NMOS	**gnda**			
	Ctest_odd	Ctest1 (charge input)			
	vdd_PA	**vdda**		23mA	
	Ctest_even	Ctest2 (charge input)			
235	**vssi**	**gnda**			
	vdd_NMOS	**vdda**		1mA	
	gnd_PA	**gnda**			
	in<0>	detector			
	in<1>	detector			
240	in<2>	detector			

All vdd=3.5V

1.b. Bounding



2. pin description

2.a. I/O pins

IN<0:63>: 64 Inputs

- Switches (1 bit common for the 64 Ch): ALL internally set by default
  - **G_diode**: anti saturation diode. Default =1V
  - **Hold1** and **Hold2** (Slow Shaper readout): default=3.5V=ON (Track)
  - **cmd_HSTL**: TTL to HSTL conversion (Vref_HSTL= 0.6V)
- **D_R, RST_R, CK_R**:
  - 1 bit for multiplexed charge measurement (Slow Channel).

- **D_G, RST_G, CK_G:**
  - shift register (D flip flop) for gain selection: 64 * 7 bits serially loaded (6 gain+1 sum)
  - 3 integrated DACs to set the 3 discri thresholds. (16 + 8) bits *3 serially loaded
  - Slow Control bits loaded

- **FS_bipolaire, FS_unipolaire, out_gain:** outputs available if valid_ch_selec=3.5V. For DC measurements only.

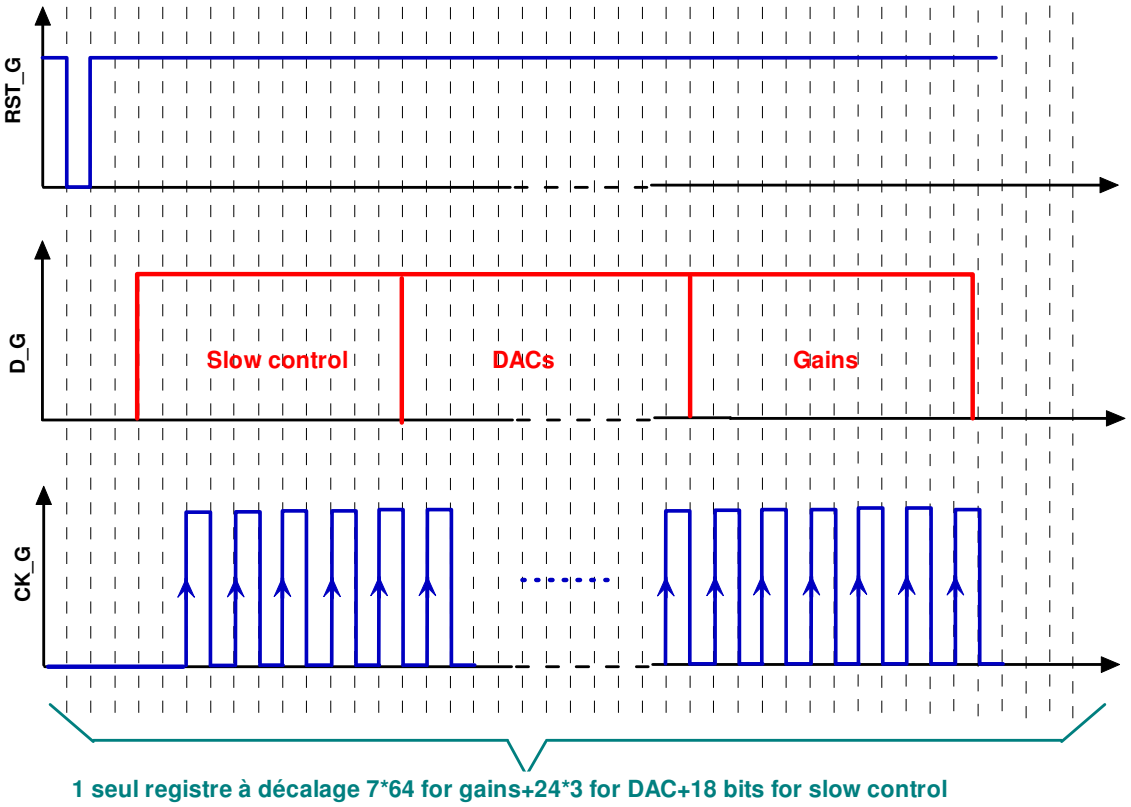
- **Qbuf_G and Qbuf_R**: use of integrated drivers for Q_G and Q_R read back

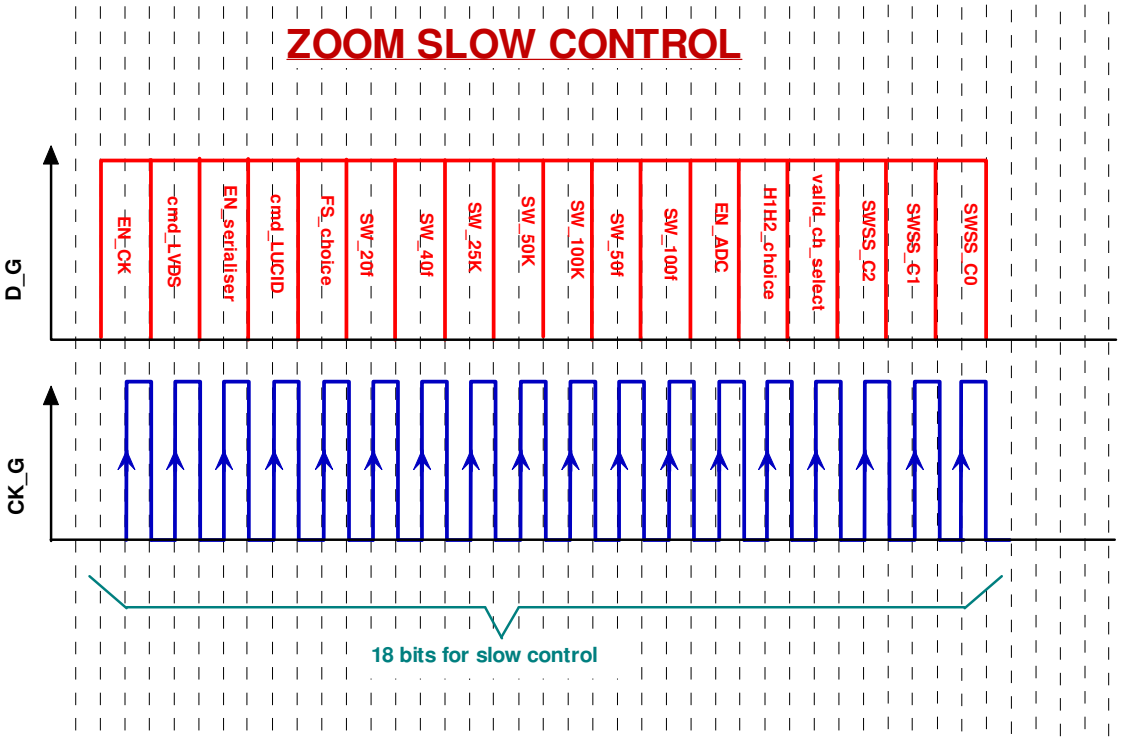
- **OTA_Q**: Charge output (Slow channel)

- **trigger<0:63>:** 64 outputs.
  - HSTL if cmd_HSTL=3.5V (and Vref_HTL=0.6V)
  - TTL if cmd_HSTL=0V.

3. ASIC Registers

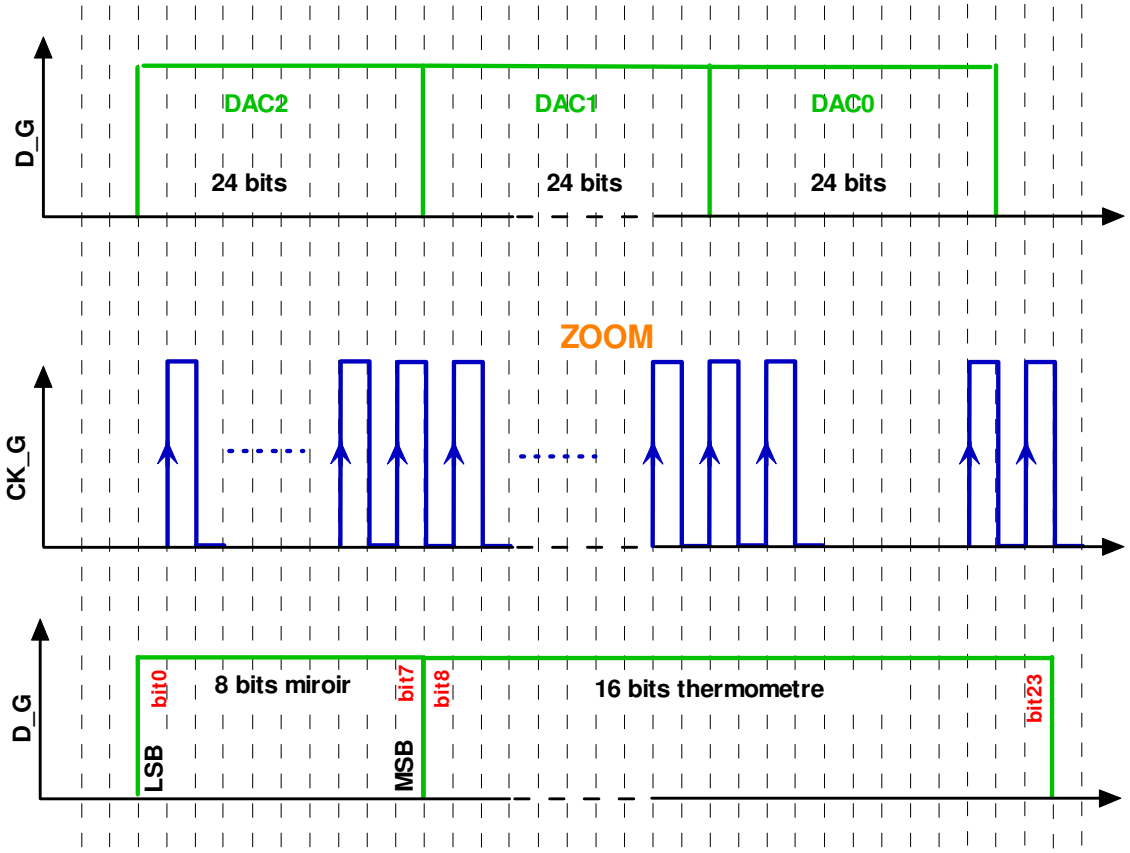
3.a. D_Gain, CK_gain and RST_G* (Static Register)



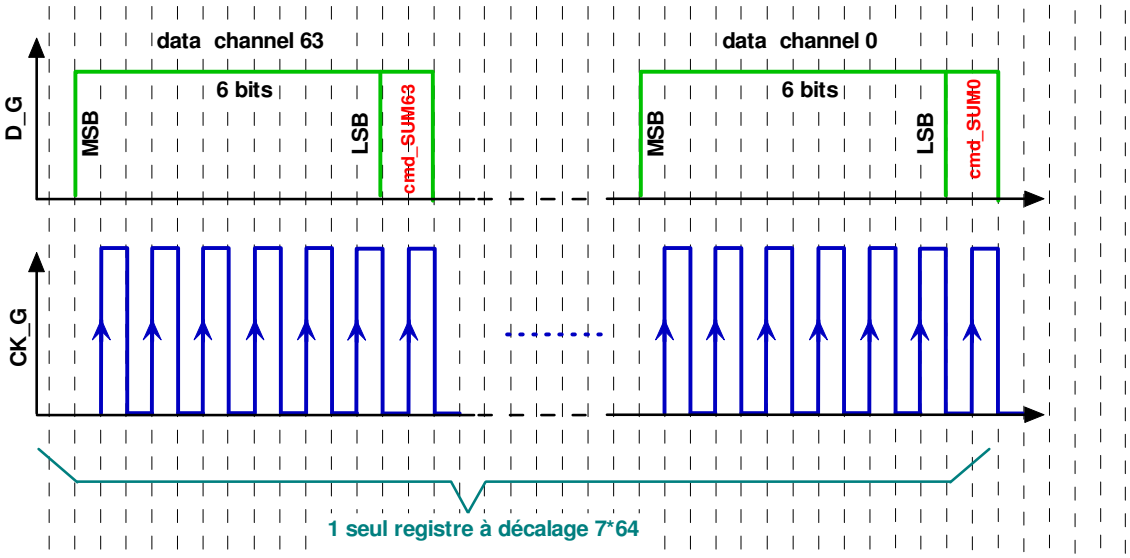


- **EN_CK** : Enable clock for encoder
- **cmd_LVDS** : enable internal LVDS/CMOS translator
- **EN_serialiser** : enable encoder for trigger output
- **cmd_LUCID** : use of the LUCID discriminators. Default= 0V= OFF
- **FS_choice** : choice between Bip (0V) or Unipolar Fast Shaper (3.5V). Default = 3.5V
- **SW_20f**(Default=OFF), **SW_40f**(Default:OFF)): Choice of Unip FS feedback Cf
- **SW_25K** (Default=OFF),**SW_50K** (OFF), **SW_100K** (OFF): Unip FS feedback Rf
- **SW_50f** (Default:OFF),**SW_100f** (Default:OFF)**:** Bipolar FS feedback Capacitor
- **EN_ADC**: Enable Wilkinson ADC input
- **H1H2_choice**: Choice between first or second Track and Hold for wilkinson ADC
- **valid_ch_select**: for DC measurements (3.5V). Default=0V
- **SWSS_C2** (OFF), **SWSS_C1** (OFF), **SWSS_C0** (default= OFF): Slow Shaper time constant

ZOOM DACs

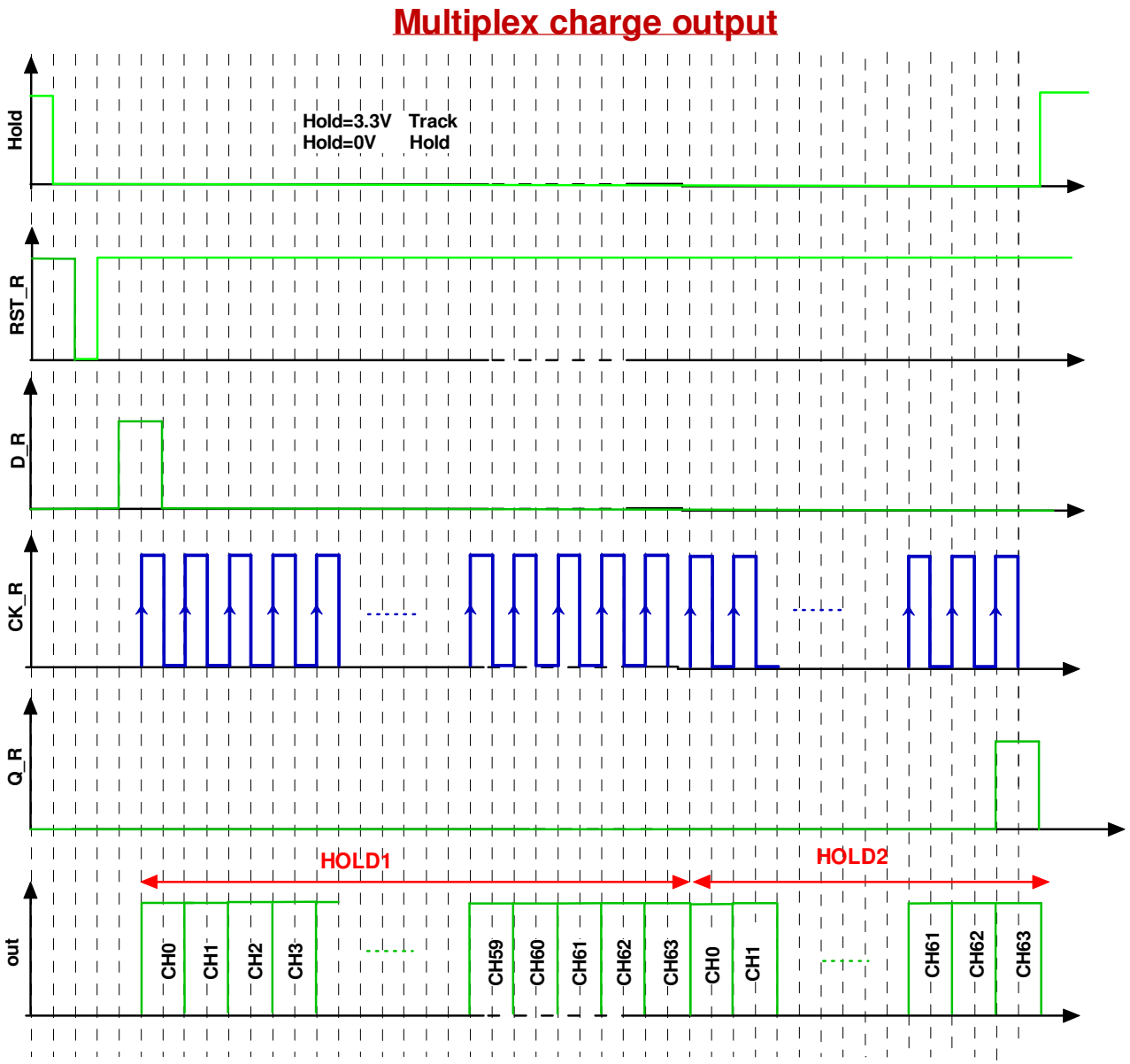


ZOOM GAIN

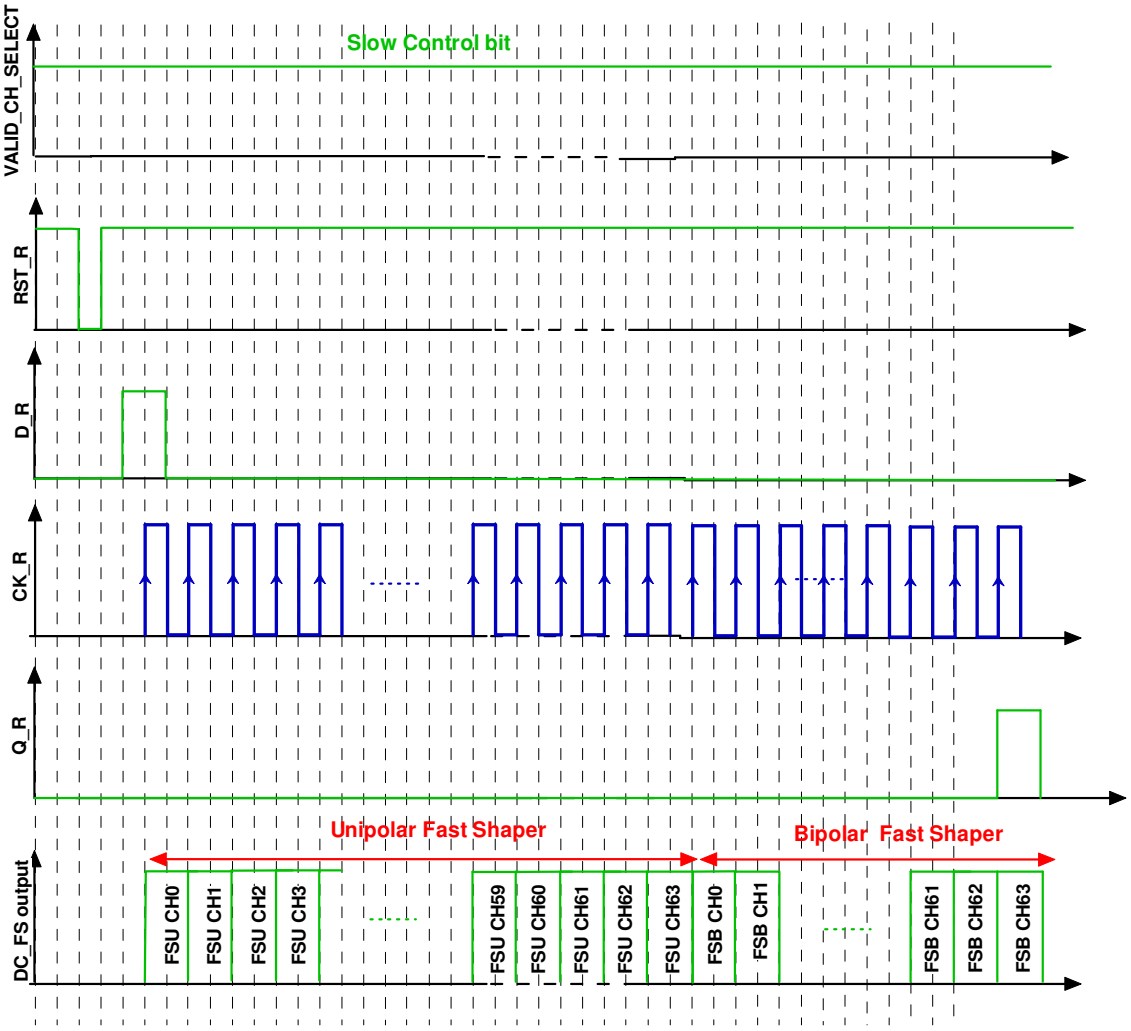


3.b. D_R, CK_R and RST_R* (Dynamic Register)

➢ **For multiplex charge output**



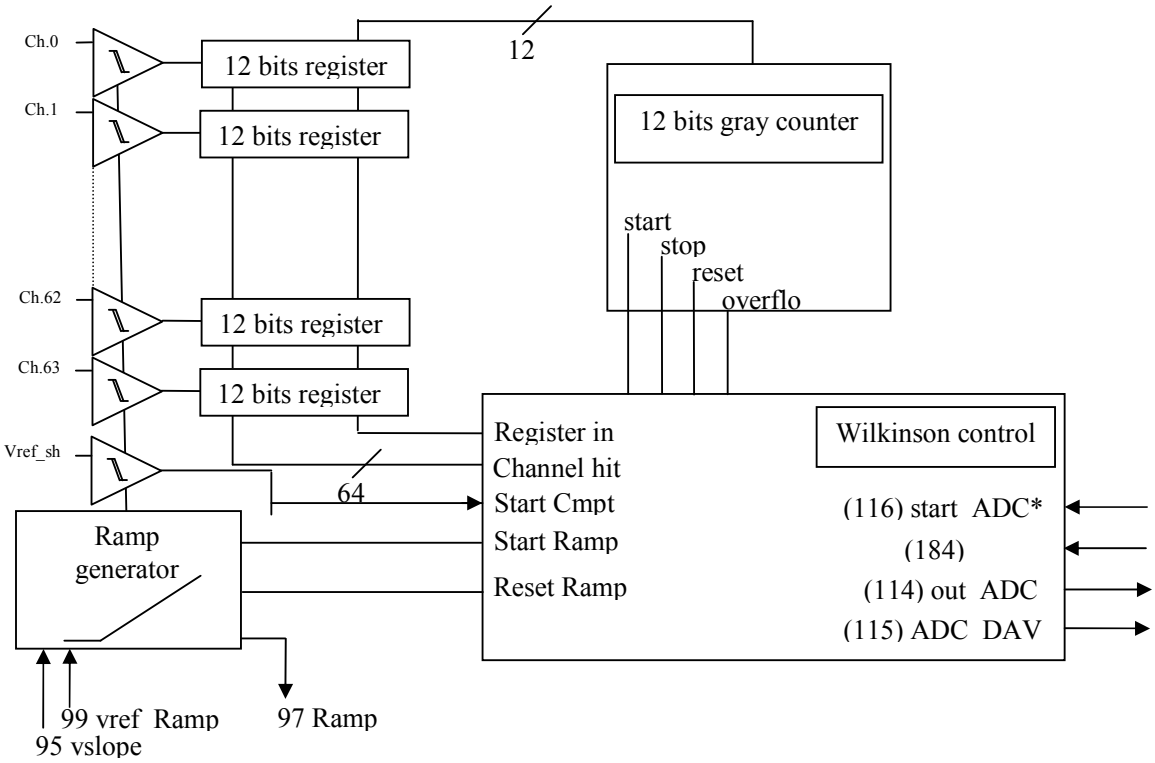
➢ For DC_FS output (pin 201)



DC_FS out put

4. ADC Wilkinson (dynamic register)

4.a. Block scheme

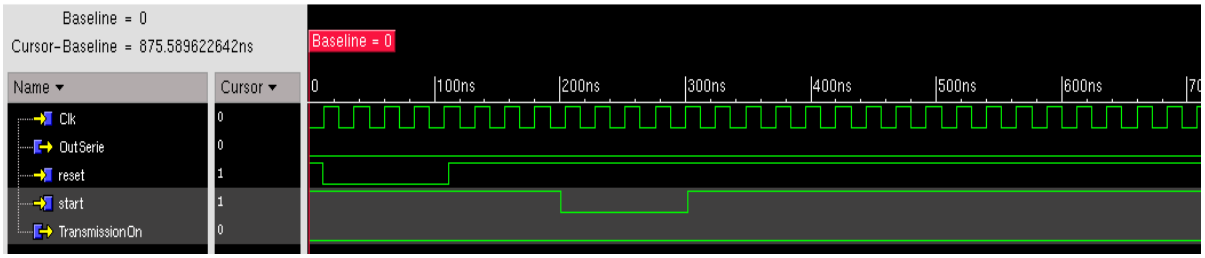


4.b. I/O description

Pin #	Pin Name	Type	Description
95	Vslope	INPUT Analog	Range : 0.4V – 1.2V / Nom. 0.8V Wilkinson ramp slope tuning
97	Ramp	OUTPUT Analog	Range : 1V-3V Wilkinson ramp output
99	vrefRamp	INPUT Analog	Range : 0.8V – 2V / Nom 1.2V Wilkinson ramp starting voltage
114	Out_ADC	OUTPUT Digital	Sync : clk rising edge Data serial output
115	ADC_DAV	OUTPUT Digital	Sync : clk rising edge Data outputting flag, active high
116	Start_ADC*	INPUT Digital	Falling edge detection, $T_{low}>3*T_{clk}$ ADC start command
184	RST*	INPUT Digital	Falling edge detection, $T_{low}>3*T_{clk}$ ADC general reset
117	ADC_CK_ON*	INPUT Digital	Level detection (active low) ADC clock validation

4.c. Chronogram

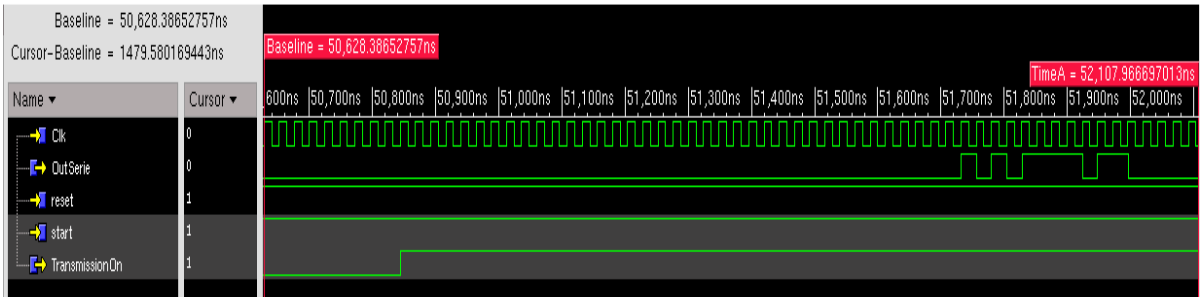
Start chronogram



The command START* is active on a falling edge. In order for the internal machine to work properly, it is needed to maintain START* at a low level at least during 2 clock pulses. If the timing is wrong the ADC will be converting for ever (loop of the machine).

The ADC conversion lasts from 3 to 4099 clock ticks. The end of the conversion is indicated by the rising edge ADC_DAV (TransmissionOn in the simulation).

Data outputting chronogram



The ADC data go out when the TransmissionOn signal changes to up state. This signal will stay up during 12bit * 64 channels = 768 clock counts. The data extracted from the Out-ADC pin (OutSerie in the simulation) will change at each rise edge clock. The first data corresponds to the MSB of the channel 0 while the last one corresponds to the LSB of the channel 63. The data changes after each clock rising edge, therefore one should read at the clock falling edge.

768 bits have to be read in total (64 12 bits ADC channels).

4.d. Measurements

Figure 42 represents respectively the mean and the RMS of the pedestal measured with the Wilkinson ADC as a function of the channel number.

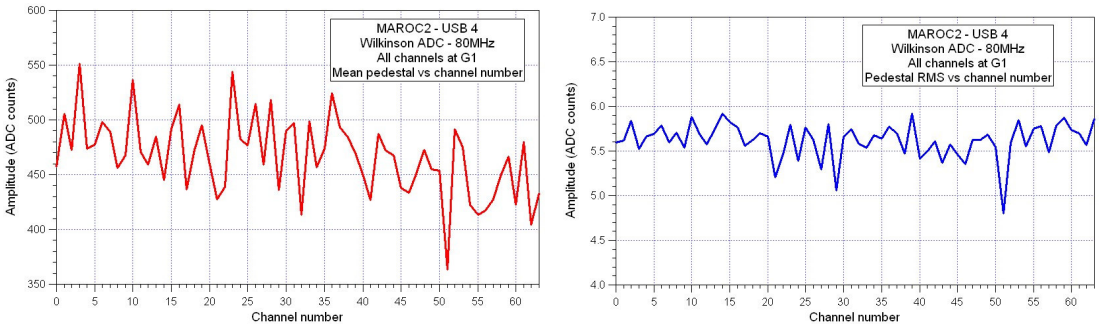


Figure 42: Mean and RMS of the pedestal measured with the Wilkinson ADC versus the channel number.

Figure 43 represents the evolution of the signal measured with the Wilkinson ADC versus the channel number for different values of the injected charge sent on the channel 30. Figure 44 shows the linearity obtained from these measurements. Figure 45 shows that the RMS of the signal measured does not vary a lot with respect to the injected charge.

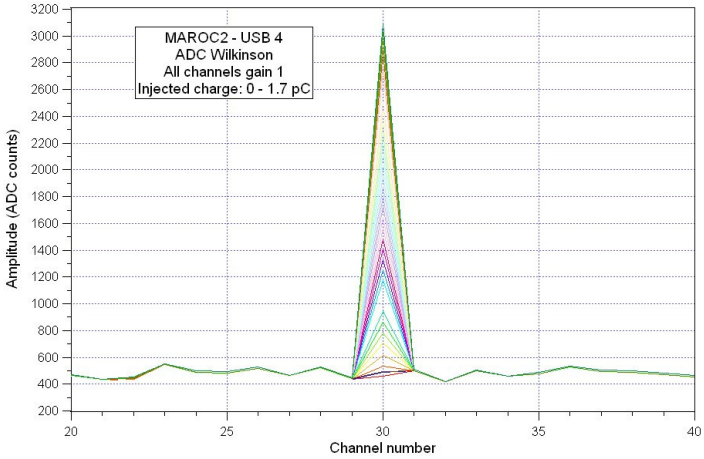


Figure 43: Mean signal amplitude measured with the Wilkinson ADC versus channel number for different injected charges.

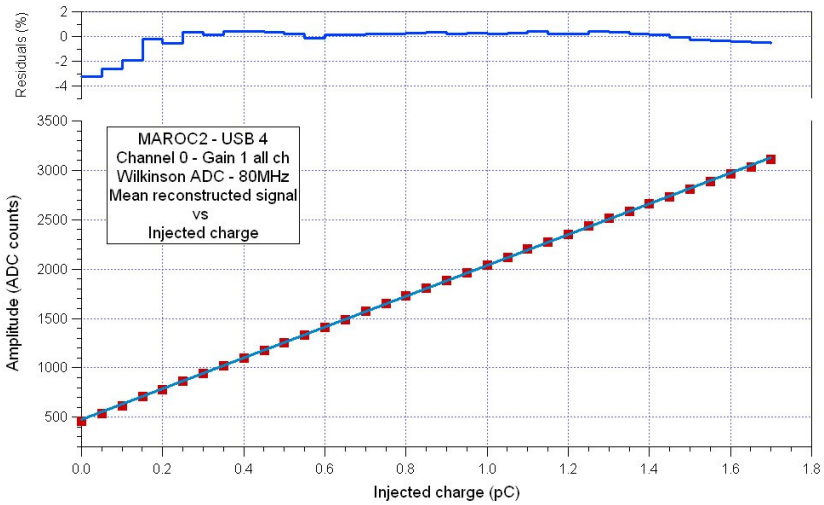


Figure 44: Mean signal amplitude measured with the Wilkinson ADC versus injected charge.

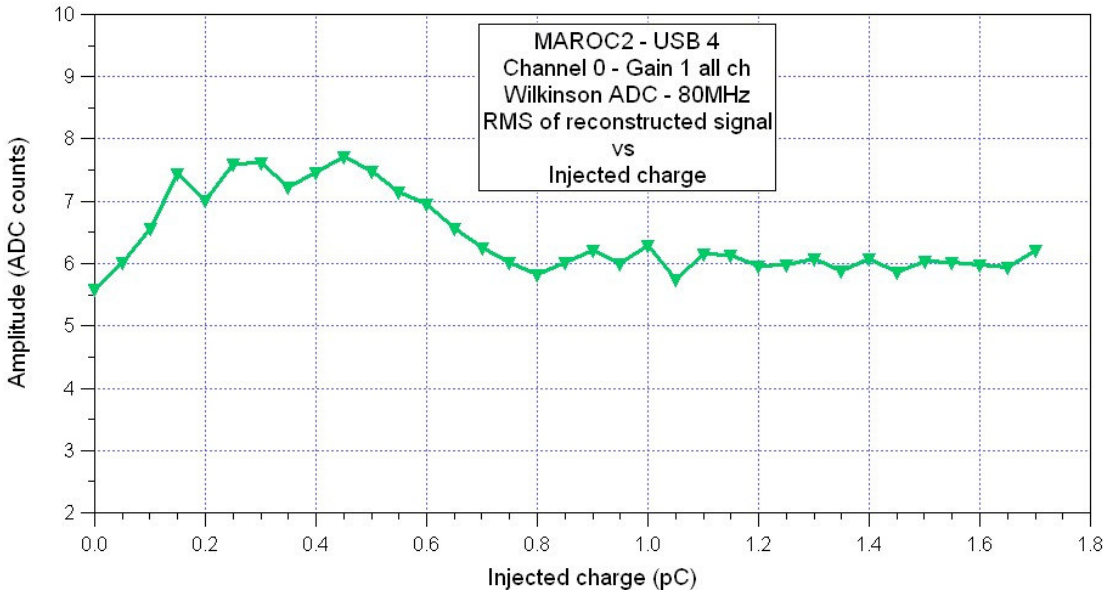
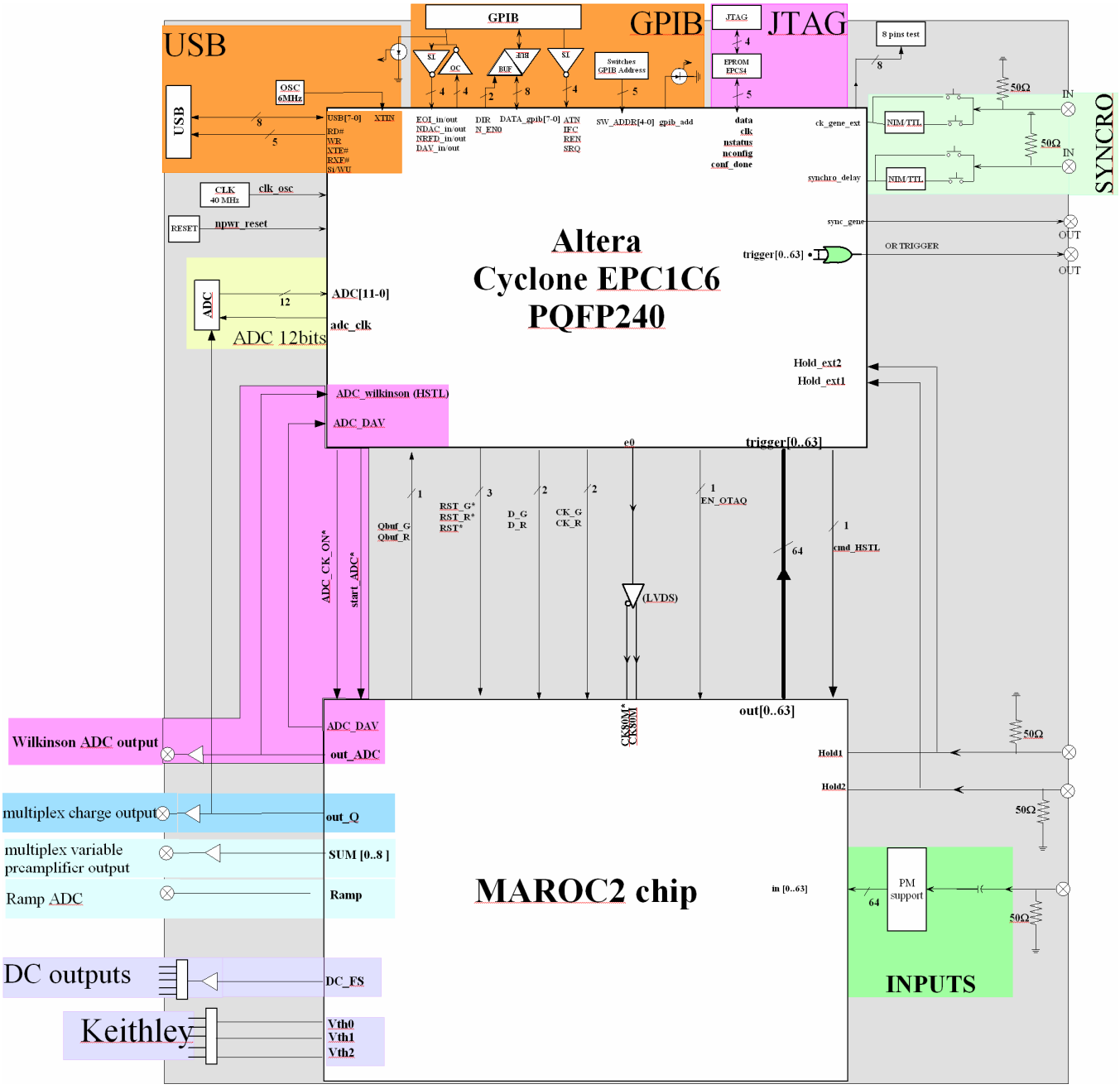


Figure 45: RMS of the signal measured with the Wilkinson ADC versus the injected charge.

ANNEXES

Test board schematic



Registres MAROC2_FPGA

LSB WORD 0 MSB

Wrreq : Sel 1 (1) Sel 0 (0)	ADC_ext (0) ADC_W (1)	Sync_gene : PLLouGéné (1) GPIB (0)	PulseStart GPIB : (0->1->0)	Enable_ Sync_gén: validé (1) hiZ(0)	reset (0->1->0)	encoded (1) non_encoded (0)	modefifo 0-> trigger 1-> adc.

WORD 1

Block Start _shift (1)	Init 40mhzaltera (1->0->1)	Sel_ChStart _shift (1)	Acq_start (1)	clear_ Selword 90 : (0->1->0)	clear_ Selword 91 : (0->1->0)	clear_ Selword 92 : (0->1->0)	gén_ext (1) /gén_ext (0)

WORD 2

RST_ GAIN : (1->0->1)	RST_ ADC_W : (1->0->1)	RST_ R : (1->0->1)	clear_fifo (0->1->0)	fréq/1	fréq/8	fréq/16	fréq/32

←---------- Ou exclusif----------→

WORD 3

num_ch[0]	num_ch[1]	num_ch[2]	num_ch[3]	num_ch[4]	num_ch[5]	num_ch[6]	hold1=0 hold2=1

WORD 4

en_LVDS (1)	EN_ OTAQ	wrreq sel_delay0 ou strt_cmpt W_delay0	wrreq sel_delay1 ou strt_cmpt W_delay1	wrreq sel_delay2 ou stat_cmpt W_delay2	wrreq sel_delay3 ou strt_cmpt W_delay3	En_serial_ link : validé (1) hiZ(0)	En_adc_clk : validé (1) hiZ(0)

WORD 5

ORD 6

Nb_acq 0	Nb_acq 1	Nb_acq 2	Nb_acq 3	Nb_acq 4	Nb_acq 5	Nb_acq 6	Nb_acq 7

WORD 7

Nb_acq 8	Nb_acq 9	Nb_acq 10	Nb_acq 11	Nb_acq 12	Nb_acq 13	Nb_acq 14	Nb_acq 15

WORD 8

SWSS_ C0	SWSS_ C1	SWSS_ C2	valid_ch_ select	H1H2_ choice	EN_ADC	SW_100f	SW_50f

WORD 9

sw_100k	sw_50k	sw_25K	sw_40f	sw_20f	FS_choice	cmd_ LUCID	EN_ serializer

WORD 10

cmd_ LVDS	EN_CK						

WORD 11

DAC10	DAC11	DAC12	DAC13	DAC14	DAC15	DAC16	DAC17

WORD 12

DAC18	DAC19	DAC110	DAC111	DAC112	DAC113	DAC114	DAC115

WORD 13

DAC116	DAC117	DAC118	DAC119	DAC120	DAC121	DAC122	DAC123

WORD 14

DAC20	DAC21	DAC22	DAC23	DAC24	DAC25	DAC26	DAC27

WORD 15

DAC28	DAC29	DAC210	DAC211	DAC212	DAC213	DAC214	DAC215

WORD 16

DAC216	DAC217	DAC218	DAC219	DAC220	DAC221	DAC222	DAC223

WORD 17

DAC30	DAC31	DAC32	DAC33	DAC34	DAC35	DAC36	DAC37

WORD 18

DAC38	DAC39	DAC310	DAC311	DAC312	DAC313	DAC314	DAC315

WORD 19

DAC316	DAC317	DAC318	DAC319	DAC320	DAC321	DAC322	DAC323

WORD 20

SUM 0	**GAIN0 0**	**GAIN0 1**	**GAIN0 2**	**GAIN0 3**	**GAIN0 4**	**GAIN0 5**	

WORD 83

SUM 63	**GAIN63 0**	**GAIN63 1**	**GAIN63 2**	**GAIN63 3**	**GAIN63 4**	**GAIN63 5**	

Registre de READ : channel select

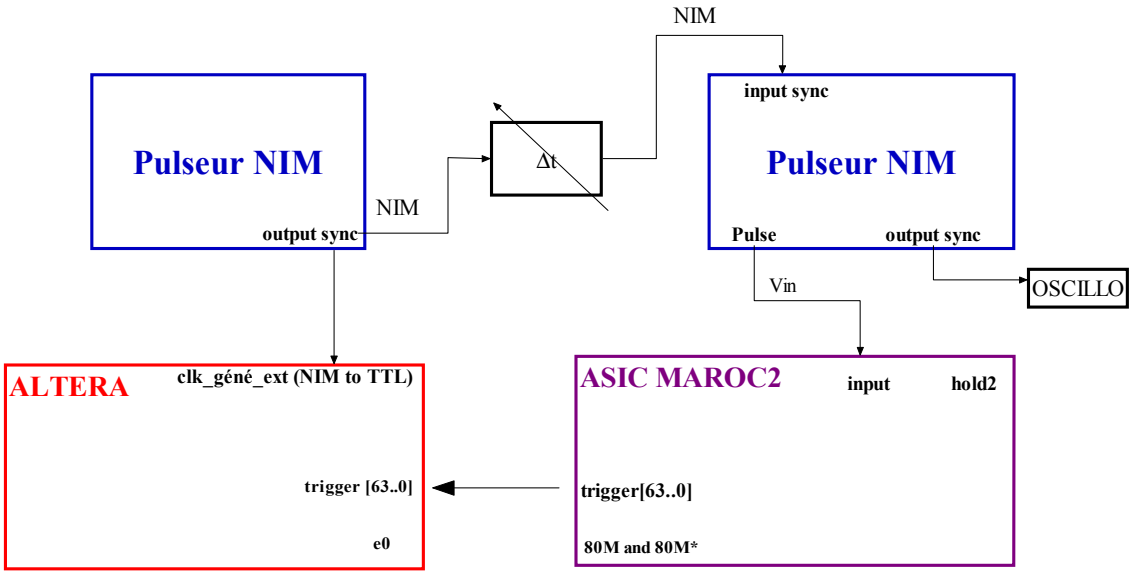
D<0..63> AND Valid_ch_select=1 alors output DC_FS=DC Fast Shaper Unipolaire
D<64..127> AND Valid_ch_select=1 alors output DC_FS=DC Fast Shaper Bipolaire

D<0..63> AND EN_OTAQ=1 alors output out_Q=output for Hold1
D<64..127> AND EN_OTAQ=1 alors output out_Q=output for Hold2

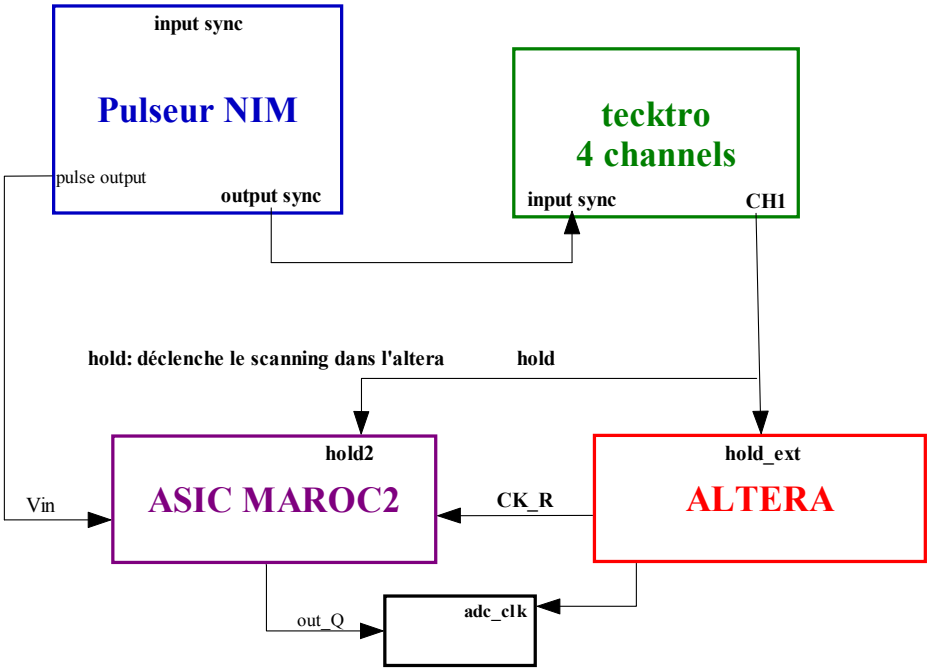
EN_ADC=1 AND H1H2_choice=1 alors output_ADCcomp=out_widlar_hold1
EN_ADC=1 AND H1H2_choice=0 alors output_ADCcomp=out_widlar_hold2

Banc de test

Appareil : 2 pulsers NIM maison



Pilotage de l'ADC_externe



Pilotage de l'ADC_Wilkinson