Electronic Methods in the Physical Laboratory

Stephan Eisenhardt
S.Eisenhardt@ed.ac.uk

Joe Rendle
j.rendle@ed.ac.uk

Junior Honours

Semester 1, 2012

Introductory Notes

Laboratory work commences **Monday 17th September** and finishes on **Friday 23th November** - with a two-week break from **Monday 22th October** to **Friday 02th November**. There will be four laboratory sessions per week: on Monday, Tuesday, Thursday and Friday, at the times 15.00—17.00 in the weeks the lectures are held, i.e. until Friday 19th October, and 14.00—17.00 thereafter. The laboratory sessions will be held in JCMB 3301. Each member of the class should attend **one** of the four laboratory sessions per week.

There are five (digital and analogue) practical exercises identified as D1, D2, A0, A1, A2 which are described in the notes that follow. Generally speaking, we expect students to find the earlier exercises a little simpler.

You should maintain a clear record of your work (as you do it!) in a laboratory notebook as directed in the checkpoint instructions. This must include a diagram of the circuit built and a table or sketch of the results obtained. Bode plots should be drawn accurately on a graph (A2). You will find it useful for the design exercises, later in the course, if you note down key points about the circuit you have built. The demonstrators will need to review your notebook as part of the assessment.

Students each have their own set of apparatus in the third year laboratories however you are still encouraged to discuss the problems and potential solutions with your colleagues. The major items of equipment (e.g. oscilloscopes, signal generator, power supply, digital multimeter, tools) will be used by different members of the class on each afternoon. However, if you build an electrical circuit on a prototype board and wish to preserve it for use the following week, you can leave it in the box of parts with which each student is provided. Remember to label the box with your name.

Assessment

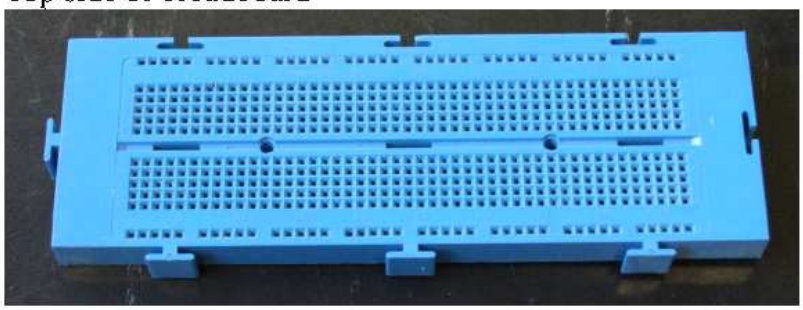
The work performed in the laboratory is subject to continuous assessment. The assessment will be based upon: your laboratory notebook, your demonstration of working circuits to the demonstrators, and discussion with the demonstrators of the work undertaken and conclusions drawn.

Assessment will be performed when you decide that you have completed the tasks up to each 'checkpoint' indicated in the following notes. At each checkpoint a mark out of 10 will be awarded by one of the demonstrators. **You will only get a mark if you can demonstrate that the relevant circuit functions correctly.** The overall laboratory assessment will be the sum of marks awarded: the weighting is specified at the start of each checkpoint. In sum of the marks for the checkpoints will provide 60% of the total assessment of the course, while the sum of the marks for the design exercises will provide 40% of the total.

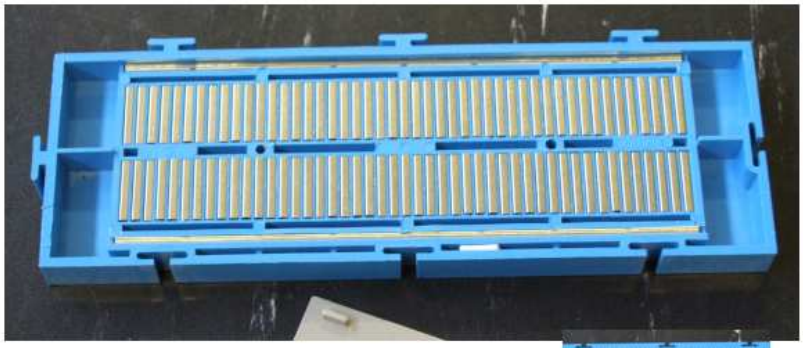
Please take note of the suggested completion date for each checkpoint as given at it end. Falling behind will incure a significant risk of missing out the final checkpoints which bear a large weight.

Basic Apparatus

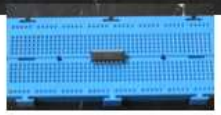
Top side of breadboard



Underneath the breadboard



This is where you put the chips:



You build all your circuits on a breadboard

You need to supply a voltage to get the chips to perform...

Check the input to and discover the output from your circuits using a multimeter

Practical Advice for Building Circuits

The following are suggestions for building the circuits in the practical exercises.

- Lay out the physical circuit so that it models the layout of the circuit diagram.
- Lay out circuits neatly.
- Use coloured wires systematically.
- Connect the circuit ground, oscilloscope ground, signal generator ground and power supply ground together.
- Test complicated circuits as you build them — it is much easier to spot faults as they occur.

You will need to learn how to use various new pieces of apparatus as the course progresses. These are the multimeter, power supply, function generator and oscilloscope. Have a go! Ask a demonstrator when you get stuck.

Troubleshooting

A common experience of students in this laboratory is that they build an electronic circuit which (initially!) fails to work as expected. This is normal. One of the purposes of the laboratory is to teach you how to respond to this situation, that is, what to do next. You will get lots of practice ...

- Don't panic!
- Be logical and systematic — proceed in small, secure steps rather than one giant intuitive leap.

More specifically, check the following:

1. Is everything switched on?
2. Is the wiring correct? Check again with pencil and paper.
3. Is the earth wiring correct?
4. Poor connections to the breadboard can be a problem — ensure that any wires inserted into the breadboard are held securely.
5. The wires used by the breadboard are single strand and can fracture if flexed unduly — check the continuity of the wires with the digital multimeter.
6. Unplug the power supply from your circuit and test it with the digital multimeter. Do you have the voltage you expect?

7. Unplug the signal generator from your circuit and test it with the oscilloscope. Do you have the input waveform that you expect?

8. Are the correct d.c. voltages reaching the breadboard? The circuit components? Test with the digital multimeter.

9. Is the oscilloscope probe attenuation set correctly? Is the oscilloscope set to AC or DC coupling? What are your trigger settings?

10. Are the correct components being used?

11. Are one (or more) components faulty? Try swapping components.

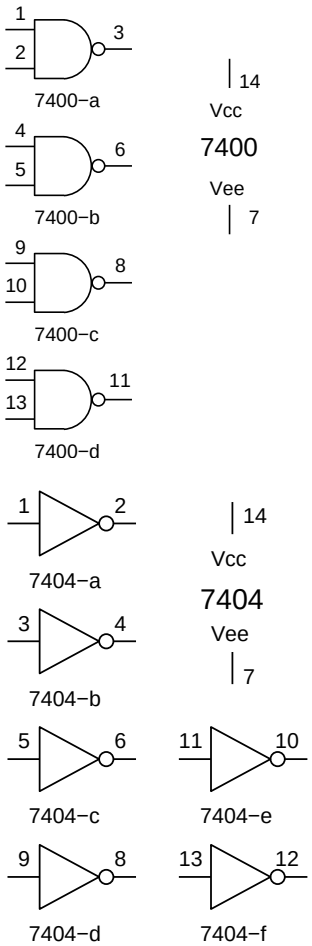
- None of these help? Do panic!

Checkpoint D1: Sequential Logic

Aim: The aim of the first checkpoint is to introduce you to building circuits via simple combinations of logic gates. **It is worth 6% of the total course mark**. Checkpoint D1.1 requires that you understand the relationship between voltages and logic levels and that you realise that a chip will need a power supply. Checkpoint D1.2 and D1.3 require progressively more elaborate combinations of chips.

Introduction to Logic Gates

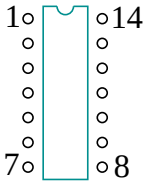
Here you will acquire practical experience in the design and use of circuits using logic gates. For this exercise 74 series NAND gates (7400) and NOT (inverter) gates (7404) are provided.



74 Series NAND (7400)

V_{CC} +5V (nominal)

V_{EE} 0V (nominal)



74 Series NOT (7404)

	Minimum (V)	Nominal (V)	Maximum (V)
Supply Voltage V_{CC}	4.75	5.00	5.25
High input (logic 1)	2.00		5.25
Low input (logic 0)	0.00		0.80
High output (logic 1)	2.40	3.40	
Low output (logic 0)		0.20	0.40

The supply voltage (V_{CC}) rail of the breadboard can be used to provide high (logic 1) inputs to the logic gates. Similarly, the ground (V_{EE}) rail of the breadboard can be used to provide low (logic 0) inputs to the logic gates. Output levels from the logic gates can be monitored by using the digital voltmeter or the oscilloscope (dc-coupled input).

D1.1 — two-input coincidence circuit

- Verify the truth tables for the logic gates fed by pins 1 & 2 and pins 12 & 13 on the 7400 chip. Verify the truth tables for the gates fed by pin 1 and pin 13 on the 7404 chip.
- Use the 7404 and 7400 logic gates to make a two-input coincidence circuit, that is, a logic circuit which gives a TRUE output if, and only if, both of the inputs are TRUE.
- Sketch symbolically the logic gate circuit used in your coincidence circuit design and write it in the form of a Boolean equation that specifies the output (Z) in terms of inputs (A and B).
- Write out the truth table you measure in each case – specify the voltage that you record at the output and the logic level this corresponds to.
- Draw a circuit diagram showing the chips, the 5 V rail, the ground rail, the input (A and B) and output (Z) connections and all intermediate connections.

D1.2 — two-input anti-coincidence circuit

- Use the 7404 and 7400 logic gates to make a two-input (A and B) anti-coincidence circuit, that is, a logic circuit which gives a TRUE output if, and only if, A is TRUE and B is FALSE.
- Sketch symbolically the logic gate circuit used in your anti-coincidence circuit design and write it in the form of a Boolean equation that specifies the output (Z) in terms of inputs (A and B).
- Write out the truth table you measure in each case – specify the voltage that you record at the output and the logic level this corresponds to.
- Draw a circuit diagram showing the chips, the 5 V rail, the ground rail, the input (A and B) and output (Z) connections and all intermediate connections.

D1.3 — exclusive OR circuit

- Use the 7404 and 7400 logic gates to make a two-input (A and B) exclusive OR circuit, that is, a logic circuit which gives a TRUE output (Z) if, and only if, one, and only one, of the two inputs is TRUE. In Boolean terms $Z = A.\bar{B} + \bar{A}.B$
- Sketch the logic gates used in your design and write down a truth table which includes the logic levels at intermediate points in your circuit.
- Draw a circuit diagram showing the chips, the 5 V rail, the ground rail, the input (A and B) and output (Z) connections and all intermediate connections.
- Complete a truth table (filling in the measured voltage levels) while showing your functioning circuit to a demonstrator.

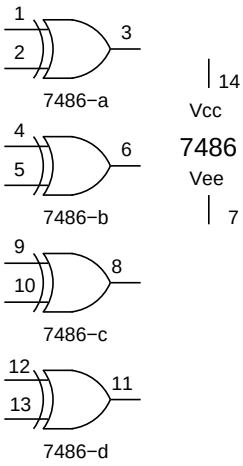
Suggested completion date: **at the beginning(!) of your session in the week of Monday 24^{th} - Friday 28^{th} September**.

Checkpoint D2: Combinational Logic

Aim: The aim of the second checkpoint is to give you experience measuring electrical quantities that vary with time. It is essential that you gain familiarity with the relevant apparatus for the subsequent analogue checkpoints (A0–A2). **Checkpoint D2 is worth 12% of the course.** To begin with checkpoint D2.1 introduces you to the idea that it takes a finite time for a logic gate to respond to a change in voltage level. Checkpoint D2.2 and D2.3 give you experience with asynchronous and synchronous logic respectively.

D2.1 — Propagation delays

Here you will see the problems which can arise due to the finite propagation time through a logic gate. If signals follow different paths through a circuit to reach a particular logic gate, the difference in propagation times along the different paths may lead to an unintended output. For this exercise 74 series NOT gates (7404) and exclusive OR gates (7486) are provided.



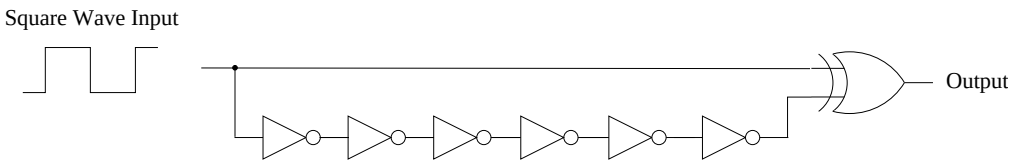
74 Series Exclusive OR (7486)

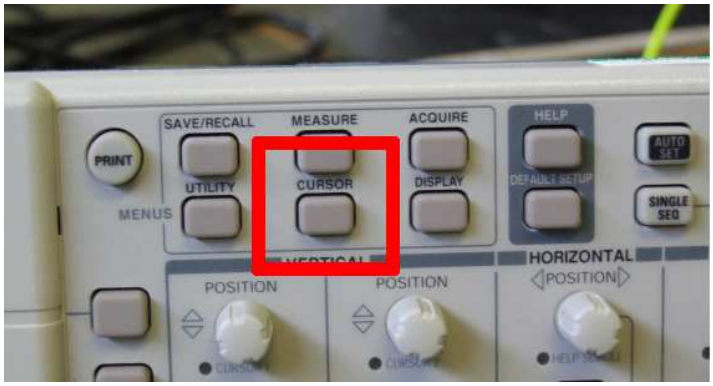
V_{CC} +5V (nominal)
V_{EE} 0V (nominal)

The following circuit uses a series of NOT gates to introduce a propagation delay on one of the inputs to the exclusive OR gate. Take the TTL output from the signal generator and feed it into channel 1 (CH1) on the digital oscilloscope. Is the voltage level observed consistent with switching between TRUE and FALSE? Set the frequency on the generator to $\sim 500\,\text{Hz}$.

- (a) Sketch the waveform. Check that the separation of pulses in time is what you anticipate by examining the trace on the oscilloscope.

Build the circuit, illustrated below, out of the 7404 and 7486 chips. Use the oscilloscope to compare the wave form from the signal generator with that at the end of the NOT gates and also with that at the output of the exclusive OR gate. You will need to use CH1 and CH2 to observe relative timing information



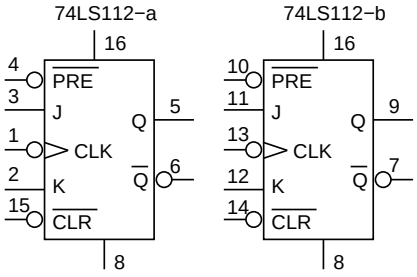


Cursor button on the oscilloscope: can be used to measure time delays accurately.

- (b) Sketch these waveforms, one above the other, on a single graph with one time axis. The resolution of the time axis of your graph will need to be below 50 ns so that you can show the pertinent behaviour.
- (c) Either by eye, of via the cursor button and *Delta*, infer a typical propagation time per logic gate.
- (d) Draw a circuit diagram showing the chips, the 5 V rail, the ground rail, the input (A) and output (Z) connections and all intermediate connections.

D2.2 — Asynchronous Logic

Here you will make use of sequential logic. For this exercise a 74 series 74112 J-K Flip-Flop will be used to construct a simple, asynchronous, two-bit binary counter circuit.



74 Series J−K Flip−Flop
V_{CC} +5V (nominal)
V_{EE} 0V (nominal)

Pin 16 V_{CC}
Pin 8 V_{EE}

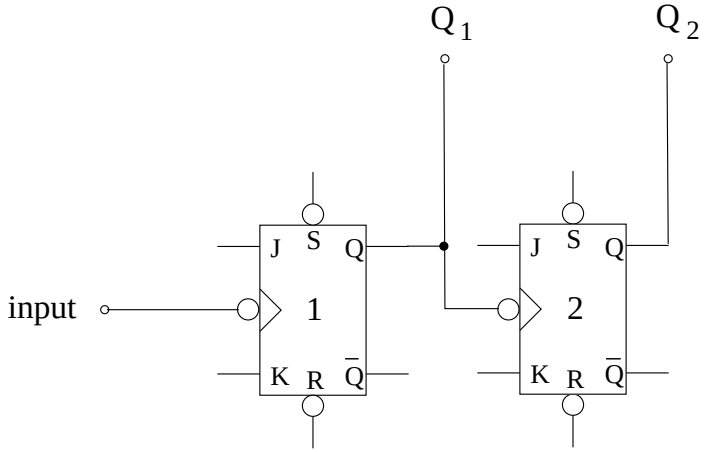
J	K	Q_{n+1}	
0	0	Q_n	storage
0	1	0	reset
1	0	1	set
1	1	$\bar{Q_n}$	toggle

Q_n is the output prior to the application of the nth clock pulse, Q_{n+1} is the output after the nth clock pulse.

Use the pin 3 & pin 2 inputs, the clock input (pin 1), and any other pins you require to demonstrate to yourself the storage and reset operations of the output (pin 5) of one of the J-K flip-flops. (Be aware that there are two flip-flops on a single chip).

- (a) What does PRESET do to the output? What does CLEAR do to the output? What do the lines above letters and abbreviations ($\overline{PRE}$, $\overline{Q}$) imply? What values do you need on pins 4 & 15?

The following circuit illustrates a simple, asynchronous, two-bit binary counter circuit using 74112 J-K Flip-Flops. Construct and test this circuit. Use LEDs (with 1kΩ in series to limit the current drawn from the gate outputs) to indicate the state of the gate outputs. Use the TTL output from the signal generator at a frequency of 10 Hz to provide the logic input for the circuit. Note that the J, K, Preset and Clear inputs must be held at appropriate logic levels for the circuit to function.

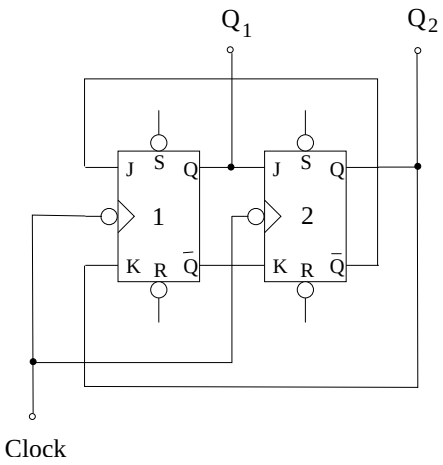


- (b) Use the behaviour of the lights to guide you drawing a time trace showing the input (clock) and the outputs (Q_1 and Q_2) while the circuit counts from 0 to 3. Explain how flip-flops **1** and **2** act in concert to give the two-bit binary counting action
- (c) What does the D in LED stand for? Is this important?
- (d) Draw a circuit diagram showing the chip, the 5 V rail, the ground rail, the input (Clock) and outputs (Q_1 and Q_2) connections and all intermediate connections.

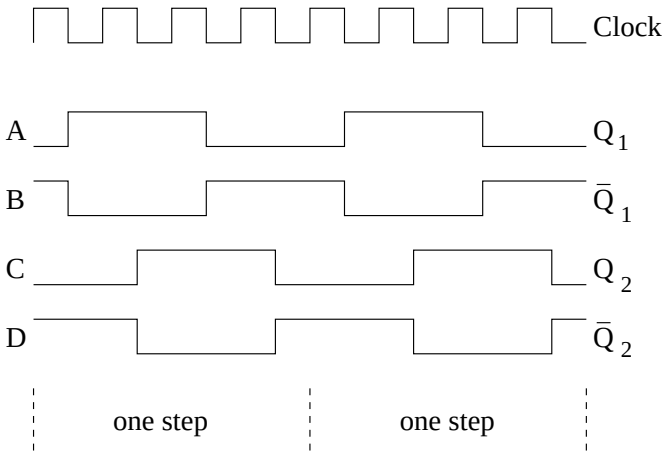
D2.3 — Synchronous Logic

Here you will implement a clocked logic circuit which overcomes the problem of spurious (erroneous) outputs which arise from differences in the propagation time of signals following different paths through a circuit.

The following circuit illustrates a simple, synchronous, two-bit binary motor control circuit using 74112 J-K Flip-Flops. Construct and test this circuit. Use LEDs (with 1kΩ in series to limit the current drawn from the gate outputs) to indicate the state of the gate outputs. **Use the function generator 'Output' to give square waves between 0 V and 4 V at a frequency of 10 Hz to provide the logic input for the circuit (the TTL output will not work reliably in this case).** Changes in the output logic levels of the 74112 J-K Flip-Flops occur at the negative-going edge of the clock pulses. Note that the Preset and Clear inputs must be maintained at logic 1 for the circuit to function.



- (a) Draw a time trace (identical to that on page 12 showing the clock input, Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$. Write down the segment of the truth table (on page 10) that is relevant to the operation of this circuit. Use the time trace and the truth table to explain the behaviour of your circuit.
- (b) Draw a circuit diagram showing the chip, the 5 V rail, the ground rail, the input (Clock) and outputs (Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$) connections and all intermediate connections.
- (c) Show a demonstrator your functioning circuit.



The counting sequence followed by this circuit is relevant to driving a stepper motor. A standard electric motor rotates continuously. A stepping motor is designed to move in finite steps with an accurately defined stepping angle The stepping motor has important applications in the electronic control of the movement of experimental equipment. By making a particular number of steps, the angle of rotation is defined. A typical stepper motor might have 200 steps per revolution. Stepper motors usually have four coils which must be energised in sequence to cause the motor to step, as in the four-phase sequence below. A, B, C and D indicate the pulse trains required by the four motor coils. It can be seen that the required sequences are provided by Q_1, $\bar{Q_1}$, Q_2, $\bar{Q_2}$ outputs of the 74112 J-K Flip-Flop circuit you have constructed.

Suggested completion date: **at the end of your session in the week of Monday 1st - Friday 5th October**.

Checkpoint A0: Basic Analogue Circuits

Aim: The aim of the third checkpoint is to give you the opportunity to manipulate passive analogue components – one of which – the capacitor will be familiar from electromagnetism classes. **It is worth 12% of the total course mark.** This checkpoint will require that you change the way you use the function generator, you will evaluate quantitative results and you will be required to study circuit behaviour as a function of frequency which connects to checkpoint A2.

Introduction — see Physics 2A notes

A capacitor can store a fixed amount of charge at a particular voltage:

$$Q = CV \text{ [coulombs, farads, volts]}$$

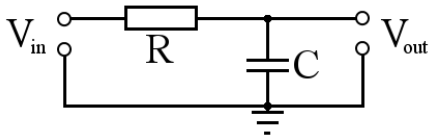
Dynamic properties:
The larger the current the faster the voltage across the capacitor changes:

$$\begin{aligned} \frac{d}{dt}Q &= \frac{d}{dt}(CV) \\ I &= C\frac{dV}{dt} \qquad \text{[amps, farads , volts / sec]} \end{aligned}$$

Discharging a capacitor, C, through a resistor, R, gives: $V = V_0 e^{-\frac{t}{RC}}$

Charging and discharging a capacitor

Build the circuit below and choose values for R and C (100 kΩ and 10 nF would work if you have these). Use the function generator to create a square wave with an amplitude that oscillates between 0 V and 1 V at a frequency of 100 Hz; this is V_{in}. Use the oscilloscope to observe V_{out}.



- (a) What is the amplitude of your input signal – as seen on the oscilloscope? Use CH1 and CH2 to show the input and output on the scope simultaneously. Is the shape of the output what you expect? What is happening as and after the square wave input? Sketch this.
- (b) Expand the timescale on the oscilloscope so you can see the charging and discharging behaviour in detail. Sketch this. By eye or by using the Cursor / Delta option measure the decay time of the circuit. Compare the charging and discharging behaviour to the RC time constant that you have chosen.
- (c) Sketch the output for an input of 1000 Hz and 10,000 Hz (on appropriate timescales). What happens to the amplitude of V_{out} as you increase the frequency of V_{in}? Why?
- (d) Show a demonstrator your circuit with input and output traces on the oscilloscope.

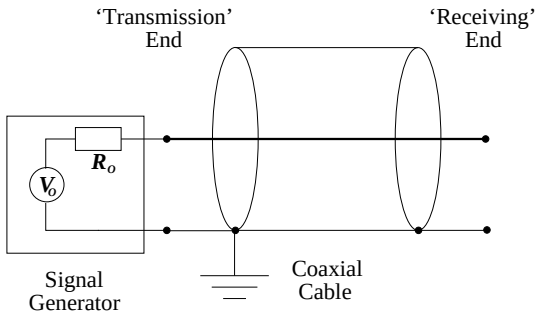
Suggested completion date: **at the end of your session in the week of Monday 8^{th} - Friday 12^{th} October**.

Checkpoint A1: Transmission Lines

Aim: The aim of the fourth checkpoint is to give you experience connecting pieces of apparatus together. This is a common area where problems arise in experimental research. **It is worth 6% of the total course mark.** You will look at what happens to signals for various cable termination conditions. You will need to draw conclusions from your observations.

Moving Signals

Here you will explore and understand the factors which are important to the transmission of signals (for example, from a sensor to subsequent signal conditioning equipment). Specifically, you will use a signal generator (to simulate the output of a sensor) to produce signals for transmission by 30m of coaxial cable.



Set the output impedance of the signal generator to 50Ω, the output signal type to square wave and the frequency to ∼1MHz. Connect the oscilloscope to the signal generator and set the amplitude of the output of the signal generator to ∼ 0.5V (∼1V peak-to-peak). Now connect the 30m coaxial cable to the signal generator (**Use the OUTPUT and the die-cast box!!!!!**) and attach the oscilloscope probes to the 'transmission' and 'receiving' ends of the 30m coaxial cable.

If your function generator doesn't look like this - Joe will have a nervous breakdown.

1. Observe and draw carefully the behaviour of the square wave signals with the 'receiving' end of the 30m coaxial cable 'open circuit'.

2. Repeat with the 'receiving' end of the 30m coaxial cable 'short circuit'.

3. Repeat with a variable resistor (potentiometer) connected across the 'receiving' end of the 30m coaxial cable. Vary the value of this variable resistor from minimum to maximum.

- What do you conclude is the characteristic impedance of the coaxial cable?
- What do you conclude is the velocity of propagation of the signal in the coaxial cable?
- Under what conditions do you obtain reflections of maximum amplitude?
- Under what conditions do you obtain reflections of minimum amplitude?
- Under what conditions do you obtain the maximum amplitude signal at the 'receiving' end of the cable?
- When you have drawn all of the graphs and answered all of the questions - show a demonstrator the behaviour of your cable with the variable resistor attached.

Suggested completion date: **at the end of your session in the week of Monday 15^{th} - Friday 19^{th} October**.

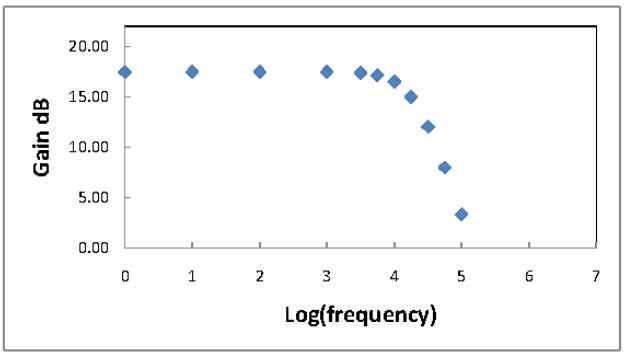
Checkpoint A2: Amplification and Filtering

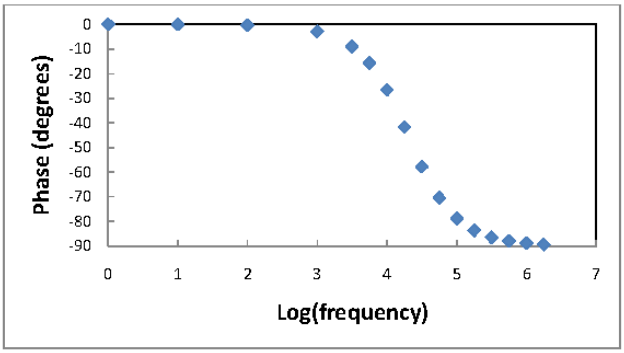
Aim: The aim of the fifth checkpoint is to introduce you to active circuits and to their intrinsic and controllable frequency response. **It is worth 24% of the total course mark.** Checkpoint A2.1 guides you through building an amplifier and assessing its performance. Checkpoint A2.2 involves adding one capacitor to the amplifier to make it a low-pass filter. Checkpoint A2.3 moves this on to a band-pass filter and to using the oscilloscope to observe its performance in the frequency domain directly.

Introduction

Here we use active components (those which amplify power) to shape signals. This builds on checkpoint A0 in that we are going to look at how periodic signals are modified as their frequency is increased. The changes to a signal as a function of frequency are usually described using Bode plots - which have been introduced in lectures:

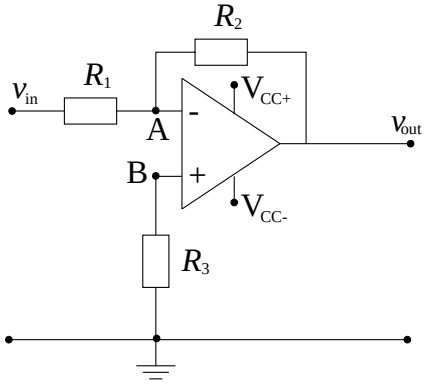
Bode Plots:

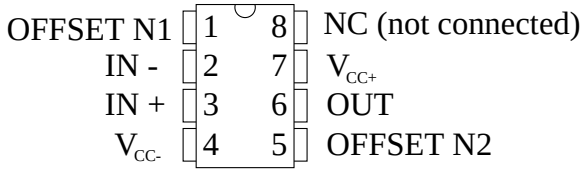




A2.1 — Amplification

Using a type μA741 operational amplifier design and construct an inverting amplifier with a gain of 10 and an input impedance of 1kΩ.

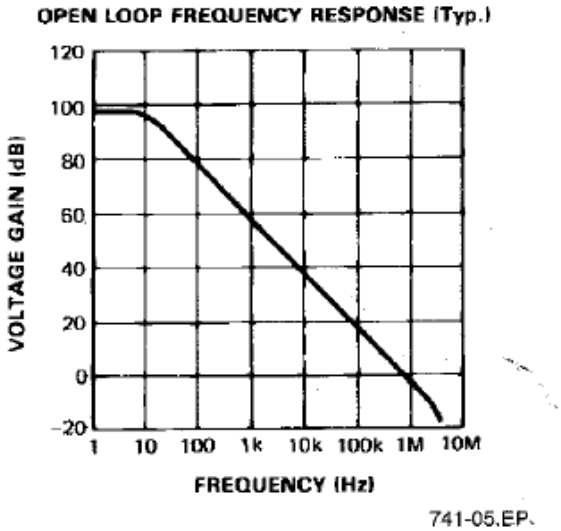




µA741 op-amp

For the purposes of this exercise: you should leave pins 1 and 5 disconnected, set $V_{CC+} = +15V$ and $V_{CC-} = -15V$. Connect the signal generator (output impedance 50Ω, sine-wave output, amplitude ∼0.05V) to the input of the inverting amplifier. Connect the oscilloscope to the output of the inverting amplifier. Measure the gain of the inverting amplifier at 100Hz, 1kHz, 10kHz, 100kHz and 1MHz (additional measurements at other frequencies will be required to answer some of the following questions):

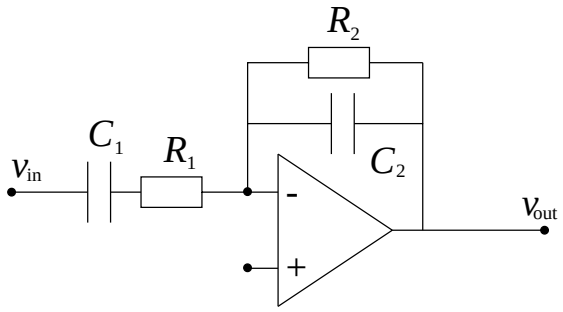
- Draw graphs of gain(dB) versus log(frequency) and phase angle versus log(frequency) (Bode plots) for the inverting amplifier. This must be done accurately on graph paper (or using a spreadsheet package).
- At what frequency does the 'roll-off' (−3dB) point occur? Considering the specifications of the μA741 operational amplifier, is this what you would expect (see graph below)?
- The character of the 'roll-off' tells us how strongly signals at frequencies **beyond** the −3 dB point are attenuated. What is the gradient of the 'roll-off'?
- Draw a circuit diagram showing the chip, the resistors you chose and the connections to the function generator, power supply and oscilloscope.



The open loop performance of a 741 op-amp.

A2.2 — Low-pass Filter

One of the design exercises is heavily based on this problem - so make sure you understand what you are doing! Suppose an application requires the filtering of a 10kHz signal from low frequency interference (e.g. 50Hz mains pickup) and high frequency interference (say, ∼1MHz). The circuit below combines a low pass (integrating) and a high pass (differentiating) filter to form a **bandpass** filter where R_2C_2 is the time constant of the low pass filter and R_1C_1 is the time constant of the high pass filter.



Adapt the inverting amplifier circuit you constructed in A2.1 by adding C_2 to create a low pass filter (integrating amplifier). Choose C_2 to give a 'roll-off' (−3dB) frequency of ∼10kHz. Measure the gain of the integrating amplifier at 100Hz, 1kHz, 10kHz, 100kHz and 1MHz (additional measurements at other frequencies will be required to answer some of the following questions):

- Draw graphs of gain(dB) versus log(frequency) and phase angle versus log(frequency) (Bode plots) for the integrating amplifier. This must be done accurately on graph paper (or using a spreadsheet package).
- At what frequency does the 'roll-off' (−3dB) point actually occur?
- What is the gradient of the 'roll-off'? i.e. how fast does the attenuation increase with frequency beyond the 'roll-off' point?
- Draw a circuit diagram showing the chip, the capacitor (C_2) you chose and the connections to the function generator, power supply and oscilloscope.

A2.3 — Band-pass Filter

Add C_1 to add a high pass filter to the circuit. Choose C_1 to give a 'roll-off' (−3dB) frequency of ∼10kHz. Measure the gain of the bandpass amplifier at 100Hz, 1kHz, 10kHz, 100kHz and 1MHz (additional measurements at other frequencies will be required to answer some of the following questions):

- Draw graphs of gain(dB) versus log(frequency) and phase angle versus log(frequency) (Bode plots) for the bandpass amplifier. This must be done accurately on graph paper (or using a spreadsheet package).

- At what frequency does the high pass −3dB point actually occur?
- What is the gradient of the high pass 'roll-off'? Justify the frequency range you have calculated this over.
- At what frequency does maximum gain occur?
- What is the maximum gain of the bandpass amplifier?
- What do you observe at the output if you input a ∼10kHz square wave? Sketch the input and output waves. Use the oscilloscope to compare the Fourier transform of the square wave before and after the bandpass amplifier (Fast Fourier Transform (FFT) is available via the Math Menu). Sketch the FFT of the input and output waves. What has happened and why?
- Draw a circuit diagram showing the chip, the capacitor (C_1) you chose and the connections to the function generator, power supply and oscilloscope.
- Show your working band-pass filter to a demonstrator.

To obtain a mark for checkpoint A2 you must have shown the working band-pass filter to a demonstrator by: **the end of your session (5 pm) in the week of Monday 19^{th} - Friday 23^{rd} November**. Rather be early to avoid the rush in the end and the risk to miss the deadline!