AIDA Update

presented by
Tom Davinson
on behalf of the AIDA collaboration
(Edinburgh – Liverpool – STFC DL & RAL)

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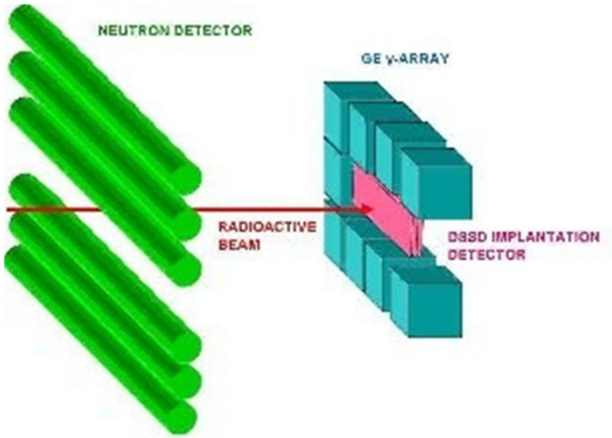
AIDA: Introduction

Advanced Implantation Detector Array (AIDA)

UK collaboration: *University of Edinburgh, University of Liverpool, STFC Daresbury Laboratory & STFC Rutherford Appleton Laboratory*



- SuperFRS
- Exotic nuclei ~ 50 – 200MeV/u
- Implant – decay correlations
- Multi-GeV implantation events
- Subsequent low-energy decays
- Tag events for gamma and neutron detector arrays

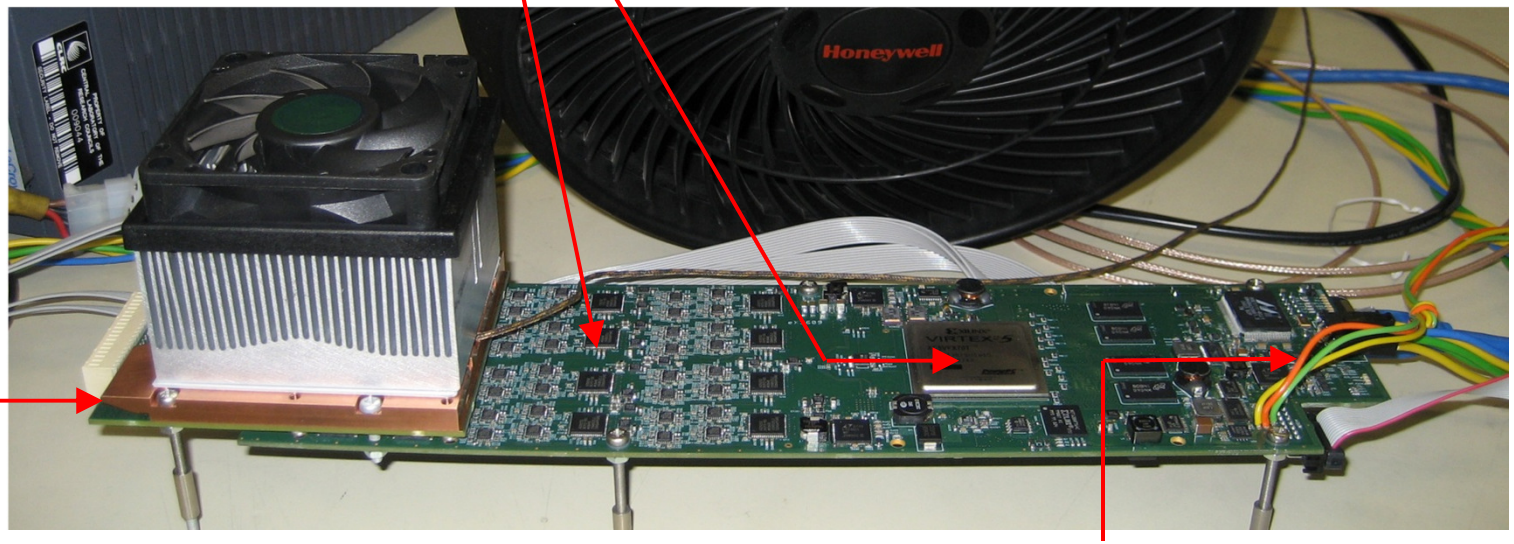
Detector: multi-plane Si DSSD array
wafer thickness 1mm
8cm x 8cm (128x128 strips) *or* 24cm x 8cm (384x128 strips)

Instrumentation: ASIC
low noise (<12keV FWHM), low threshold (0.25% FSR)
20GeV FSR *plus* (20MeV FSR *or* 1GeV FSR)
fast overload recovery (~μs)
spectroscopy performance
time-stamping

AIDA Hardware

Mezzanine:
- 4x 16 channel ASICs
- Cu cover
  - EMI/RFI/light screen
  - cooling

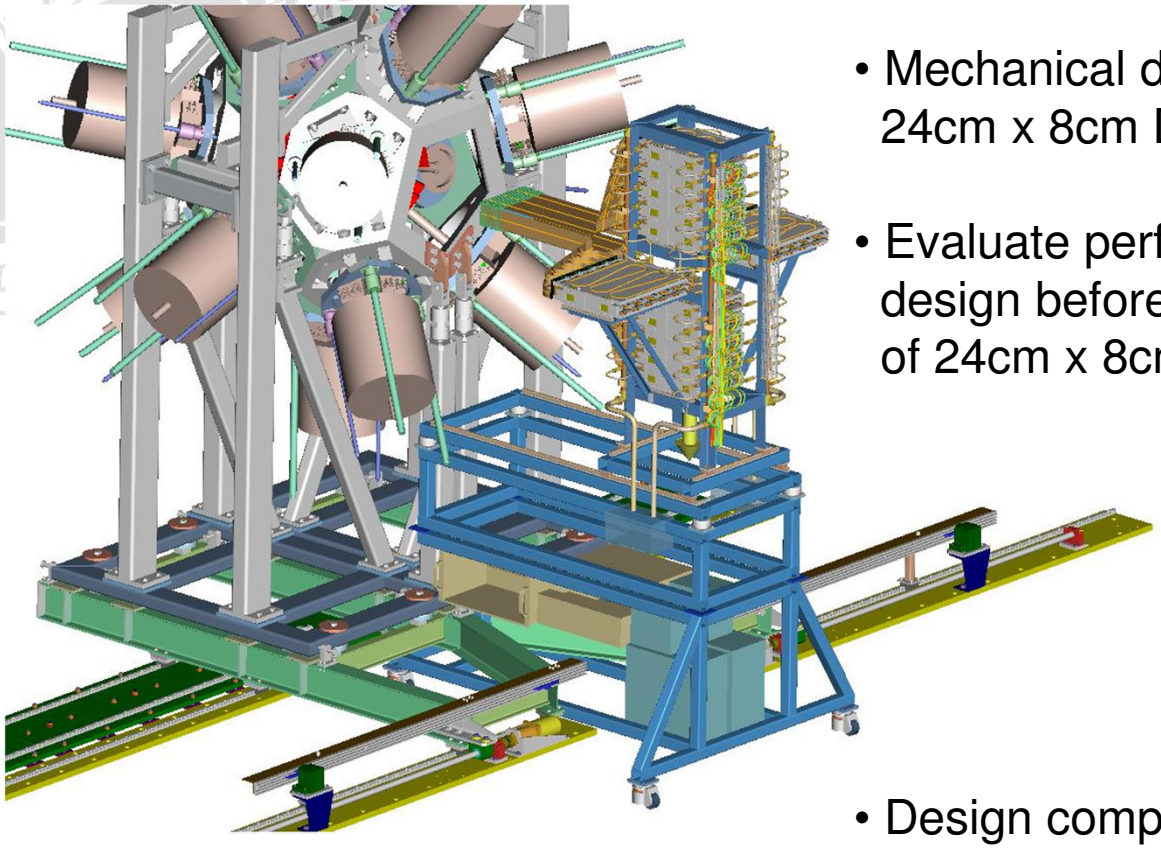
FEE:
- 4x 16-bit ADC MUX readout (not visible)
- 8x octal 50MSPS 14-bit ADCs
- Xilinx Virtex 5 FPGA
  - PowerPC 40x CPU core/Linux OS – DAQ



FEE width: 8cm
Prototype – air cooling
Production – recirculating coolant

Gbit ethernet, clock, JTAG ports
Power

AIDA Mechanical



- Mechanical design for 8cm x 8cm and 24cm x 8cm DSSSDs is complete
- Evaluate performance of 8cm x 8cm design before proceeding to manufacture of 24cm x 8cm design
- Design compatible with BELEN, TAS, MONSTER , RISING, FATIMA etc.

- Design drawings (PDF) available
  http://www.eng.dl.ac.uk/secure/np-work/AIDA/

AIDA: status

- DSSSD with sub-contractor (MSL)
  - 8cm x 8cm & 24 x 8cm mechanical samples
  - 4x 8cm x 8cm prototypes delivered
  - 10x 8cm x 8cm wafers + additional 0.5µm passivation
    production batch in progress
    5 @ QA, 5 @ processing

- Production hardware (ASIC, FEE Mezzanine PCB, FEE PCB) delivered by sub-contractors

- FEE64 Mezzanine assembly
  - 78 completed and delivered

- FEE64 PCB
  - 50 OK
  - 19 (1 of 64) channels noisy, otherwise OK
  - 6 with faults requiring further tests

- FEE module assembly
  - 12 complete and tested OK
  - 20 queued

AIDA: status

- MACB timestamp distribution system for FEE modules
  - delivery complete

- Mechanical design and infrastructure (HV, PSUs, cooling etc.)
  - detector HV, FEE PSUs, cooling & FEE crates delivered
  - support assembly completed

AIDA: outlook

- AIDA production hardware was available for commissioning on schedule in 2011/Q3

- Performance of 20GeV & 1GeV ranges meets specification
  - *need to optimise DSSSD-FEE coupling for 20MeV range*
  - *progress very encouraging*

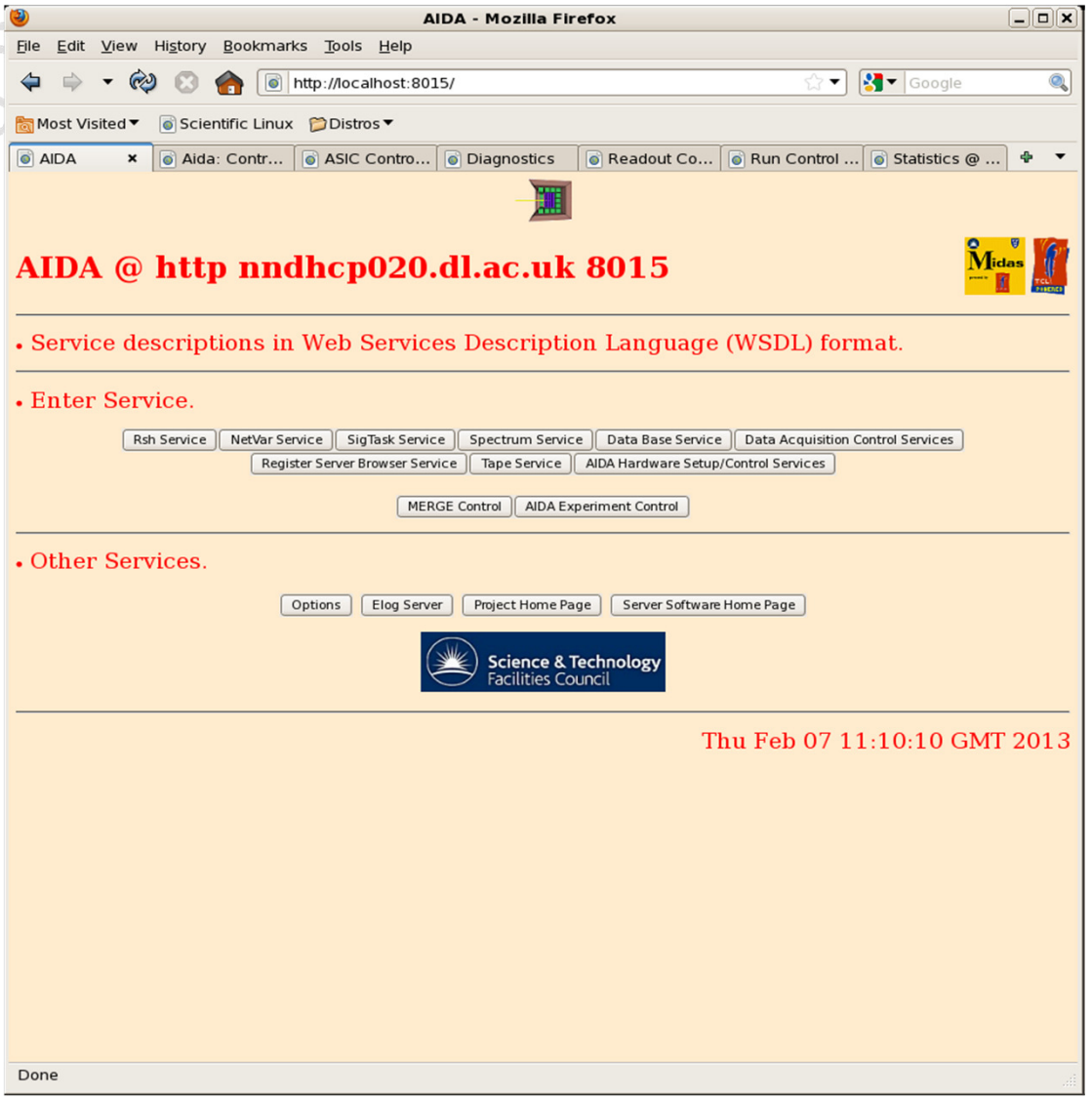
- Basic data merge with MBS successfully demonstrated during AIDA+LYCCA test May 2011
  - *further work required*

- Continuing FEE firmware development work in progress
  - *DSP (64 channel digital CFD being tested)*

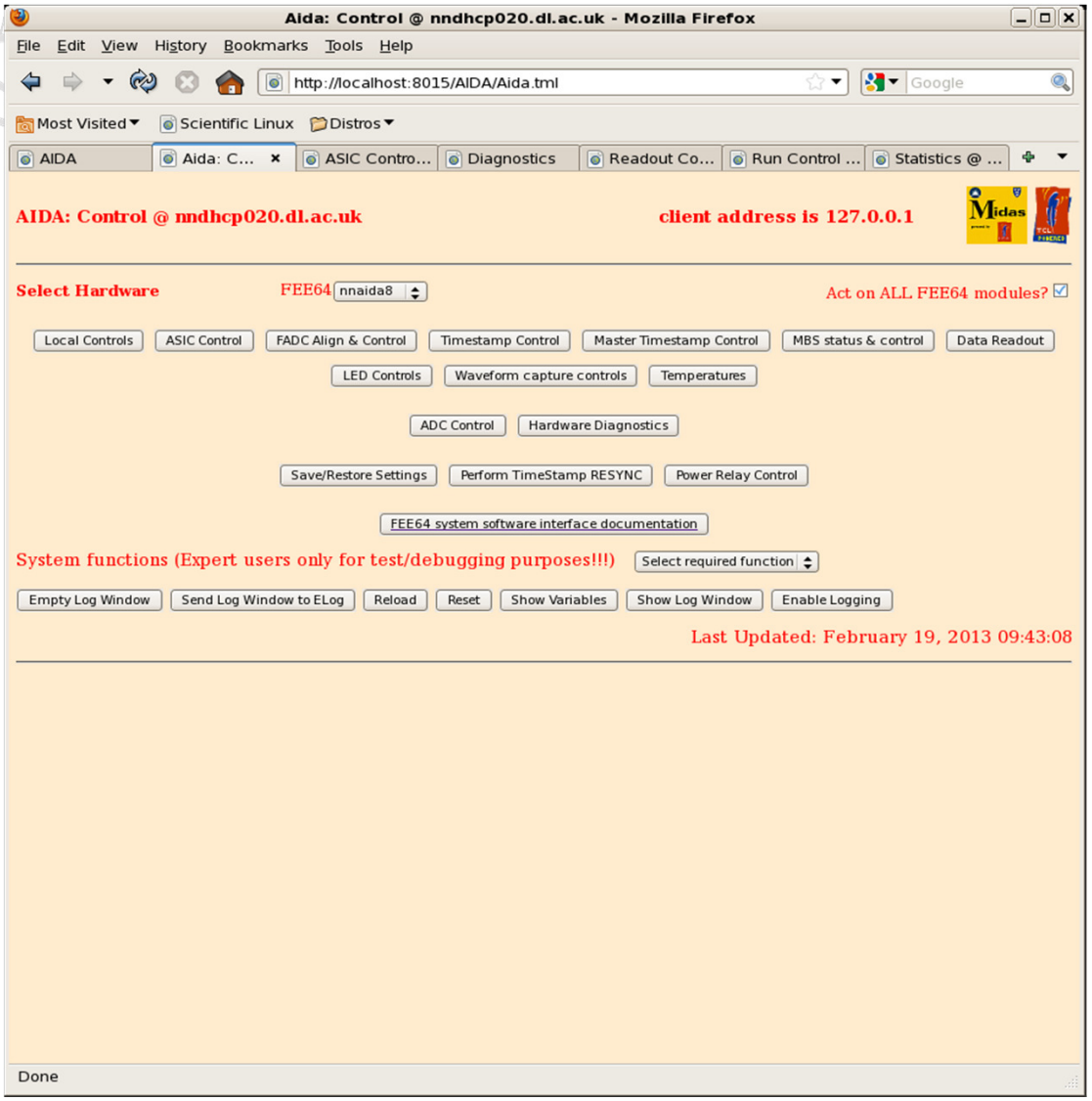
- DAQ software development work in progress
  - interface migrated from Tcl/Tk to XML/SOAP (web-based)
  - control and management of multiple FEE modules
  - timestamp-ordered data merge (GREAT format)

Bottom line – AIDA is ready and needs to be scheduled on FRS

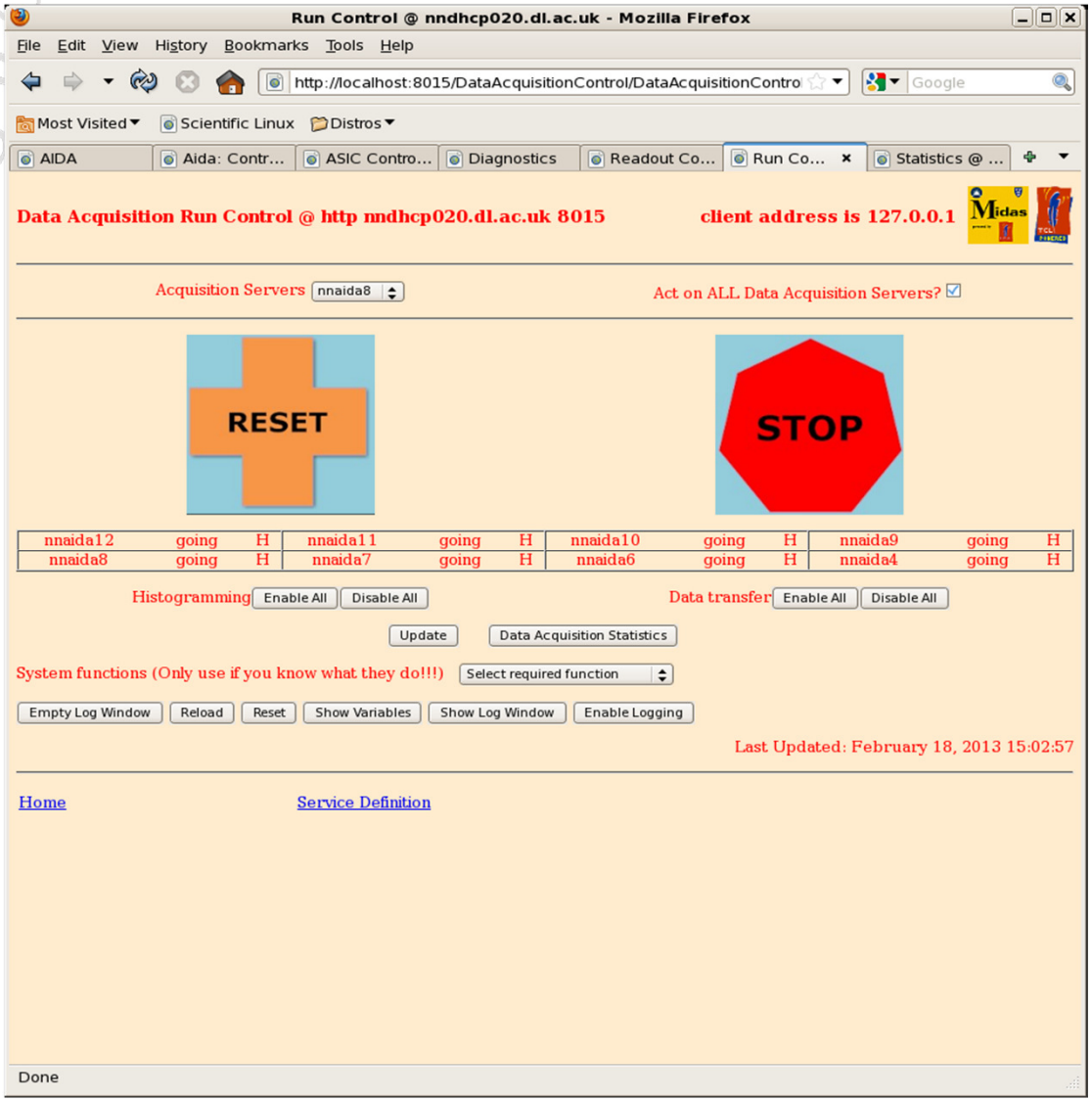
AIDA: homepage



AIDA: DAQ main menu

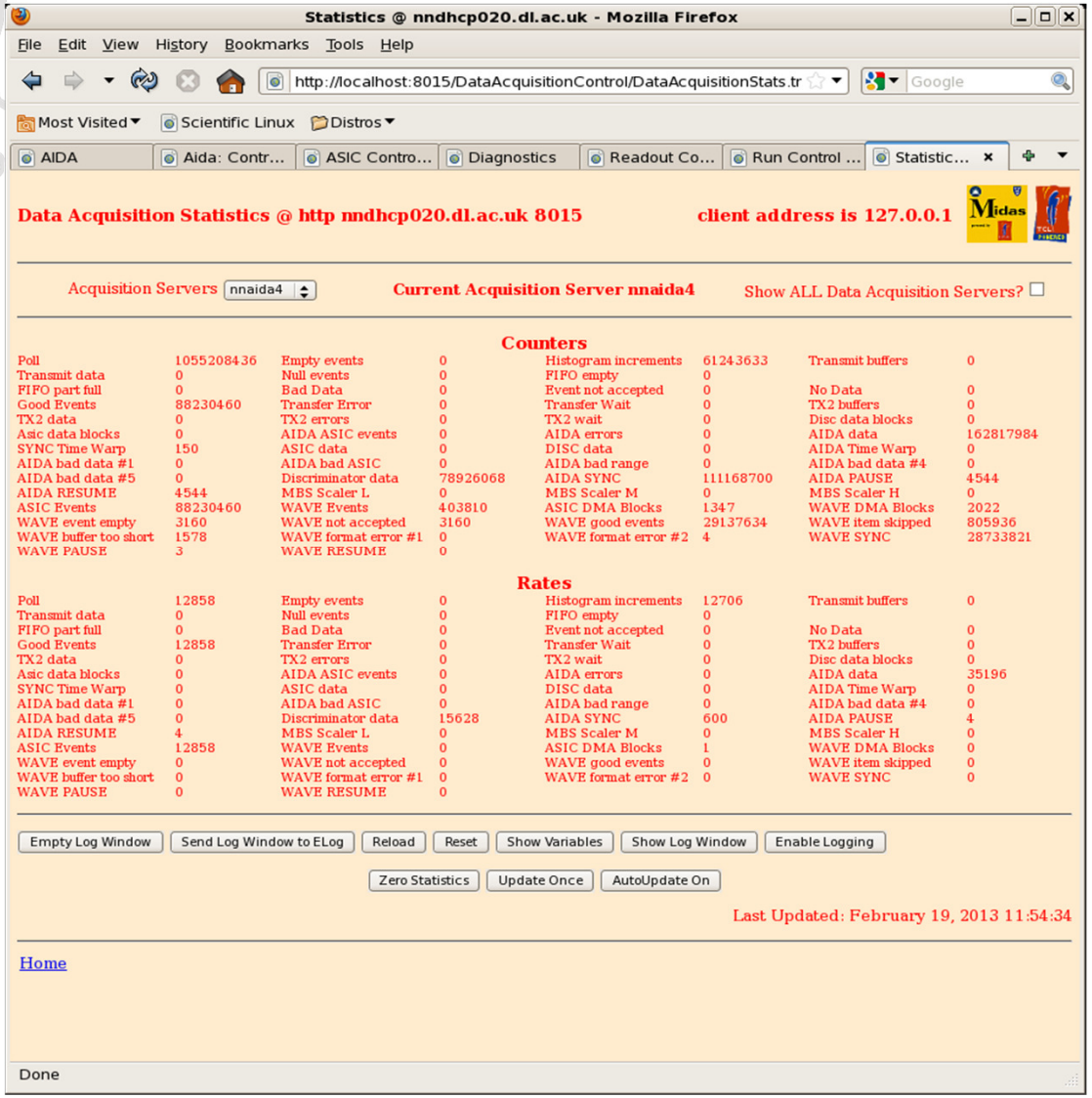


AIDA: experiment control

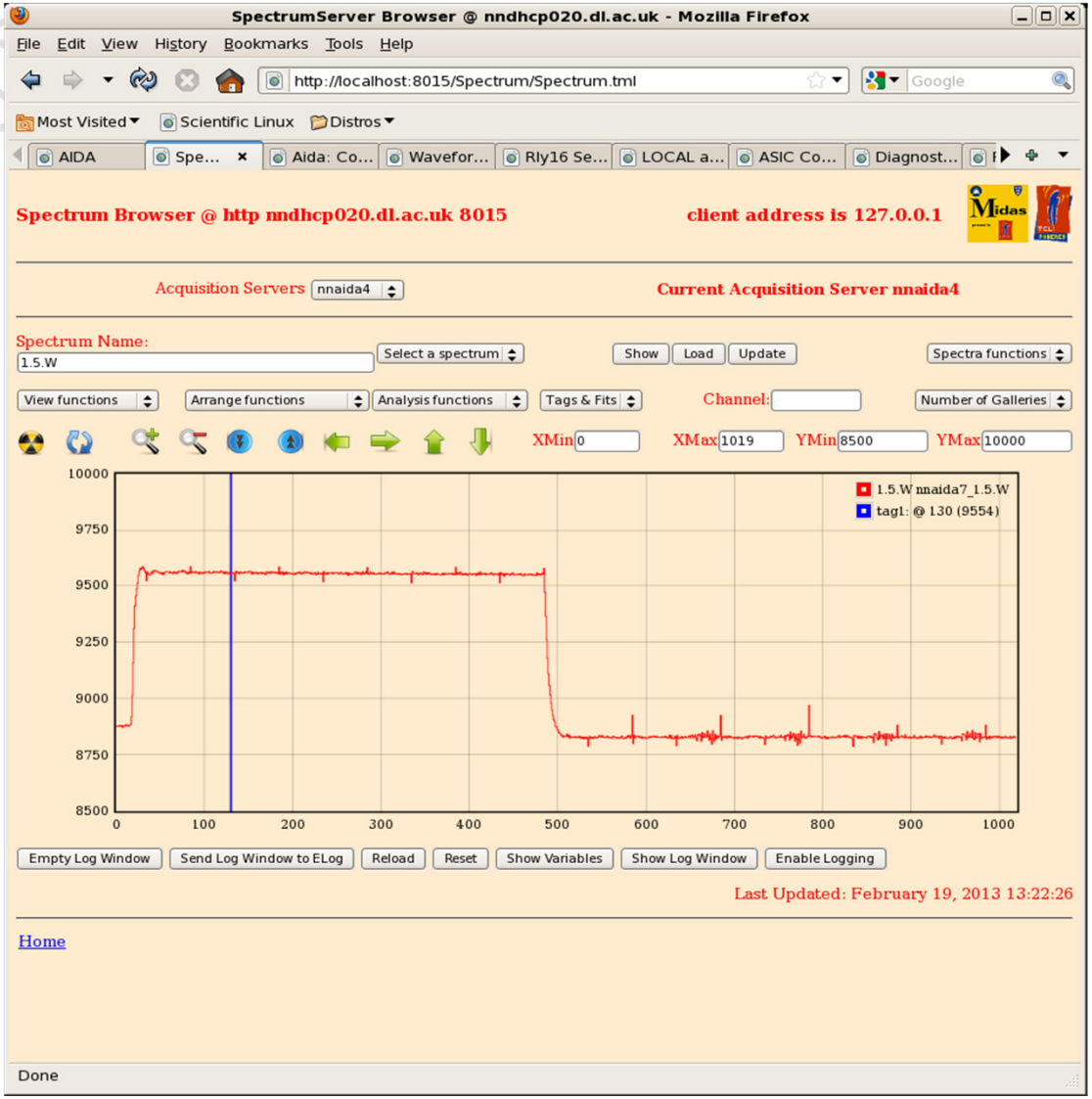


Note – illustrates configuration controlling 8x FEE64 cards

AIDA: DAQ statistics



AIDA: preamplifier waveform capture



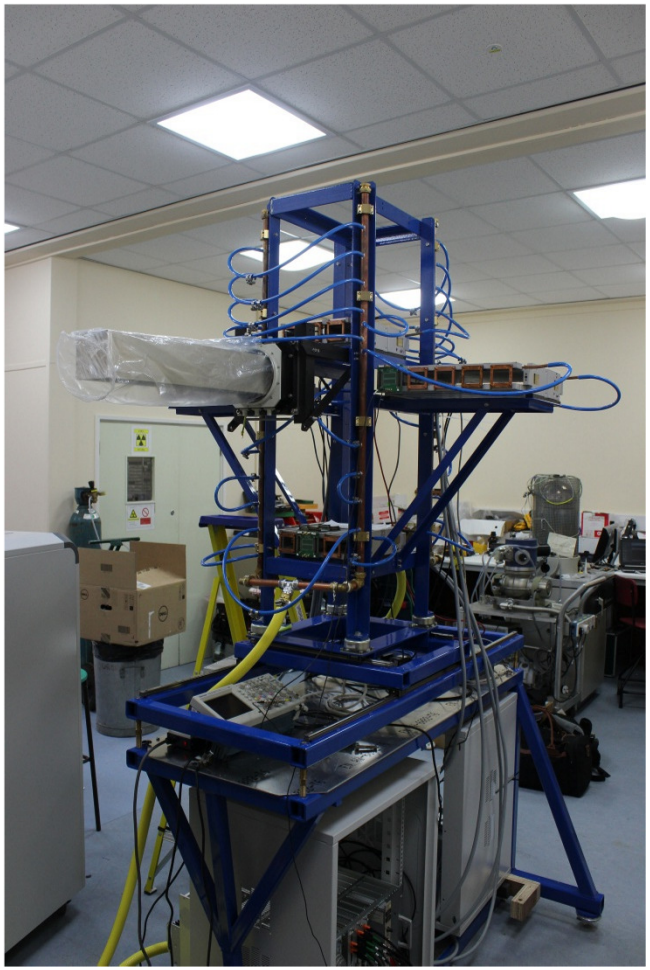
AIDA Plans

S390 "In-beam test of the AIDA detector system for DESPEC"
- 23 shifts parasitic
- investigate ASIC response to high energy, heavy-ion implants
- evaluate and optimise fast overload recovery performance
- optimise ASIC parameters for fast decay-decay correlations

S416 Search for proton emitters in the trans-lead and sub-uranium region
- 15 shifts primary, 9 shifts parasitic
- search proton emitters ^{203}Ac, ^{197}Fr and ^{189,190,191}At
- study alpha decay of other nuclei
- need physics outputs

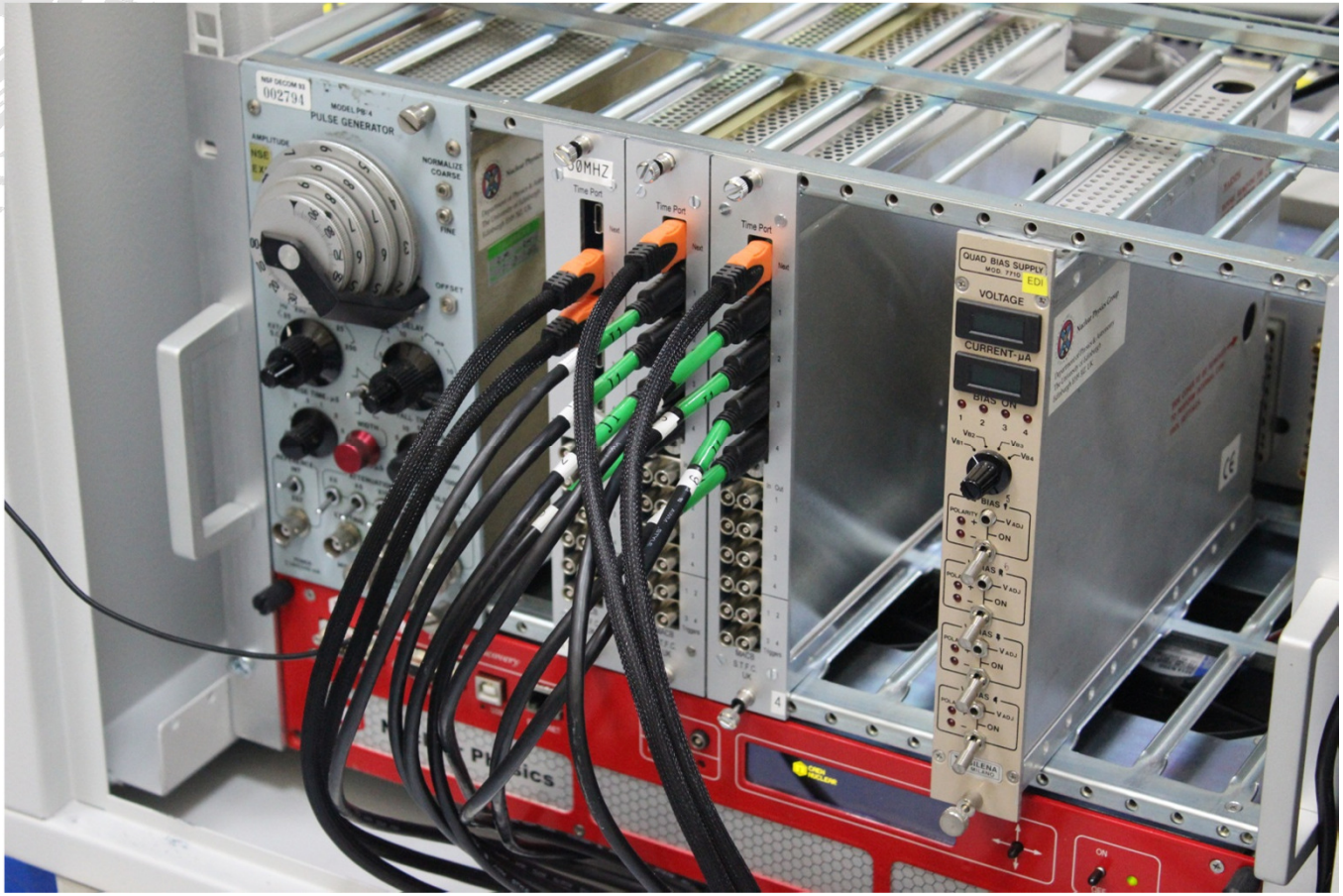
PRESPEC umbrella proposal
"Test of different setups for the HISPEC/DESPEC collaboration"
FATIMA, TAS, BELEN, MONSTER, AGATA …

AIDA: Support Assembly



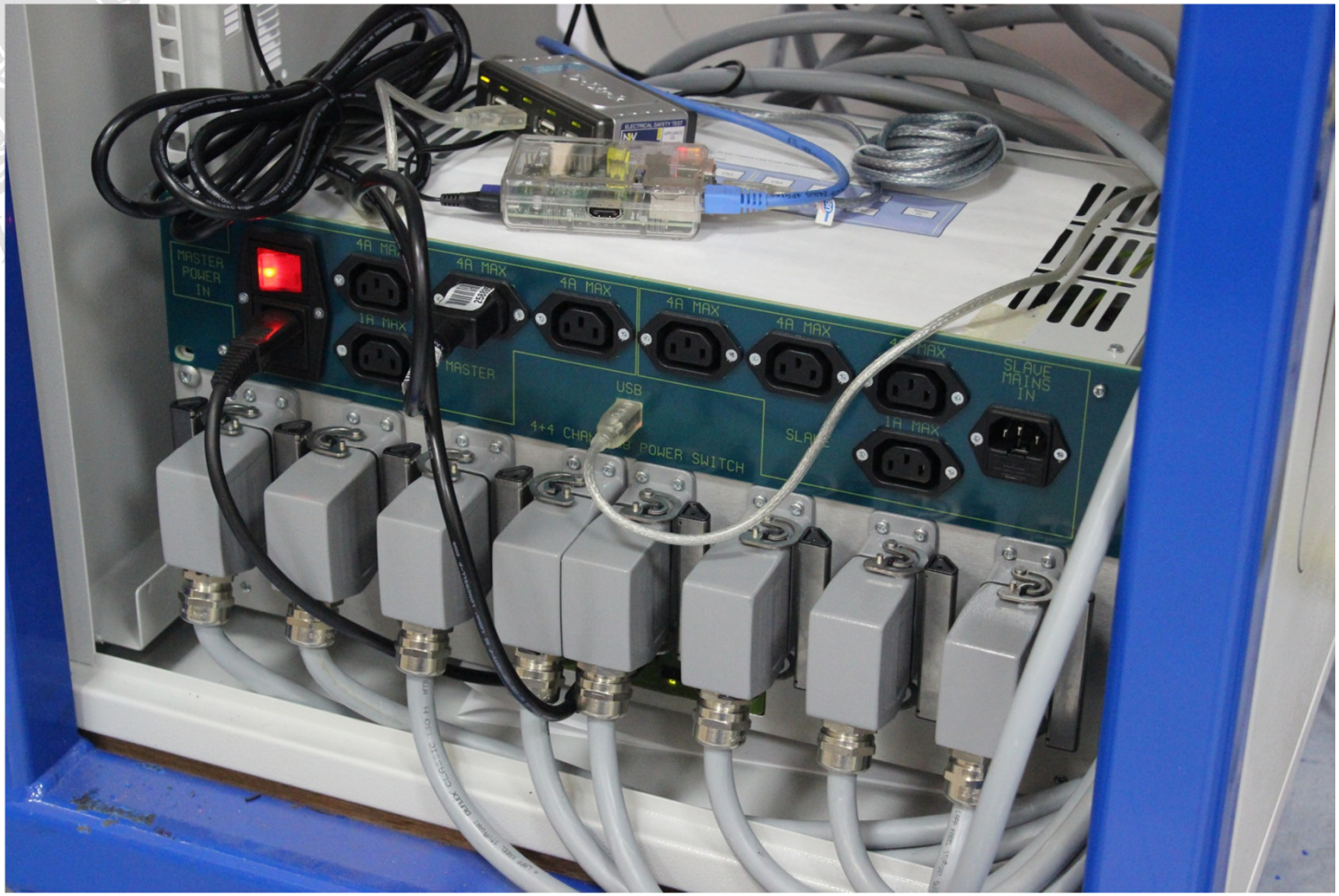
'All up' tests in T4 laboratory STFC Daresbury Laboratory
Note Julabo Recirculating Chiller to side of assembly

AIDA: MACB



Timestamping hardware with HDMI cabling to AIDA FEE modules

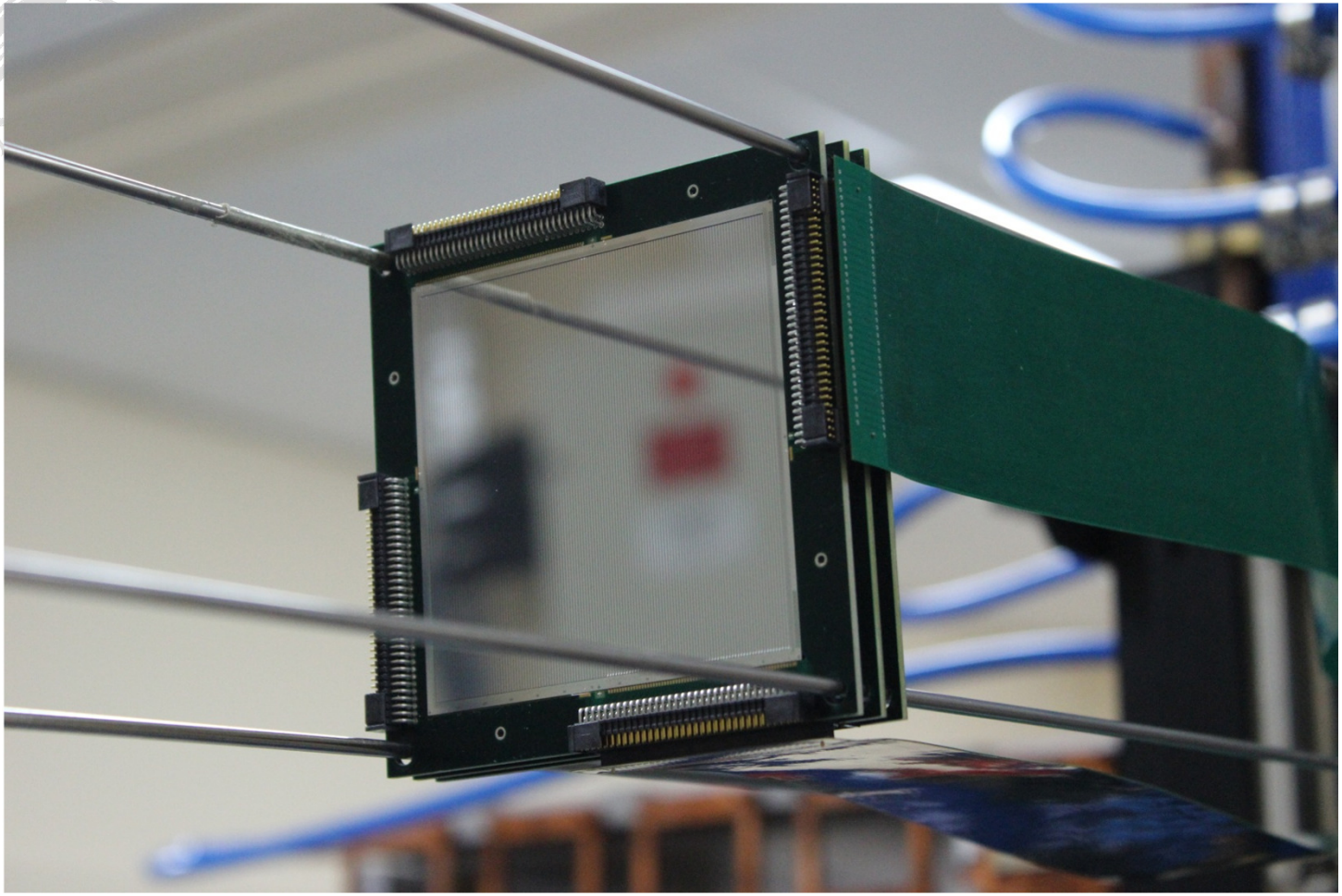
AIDA: FEE Power Supply



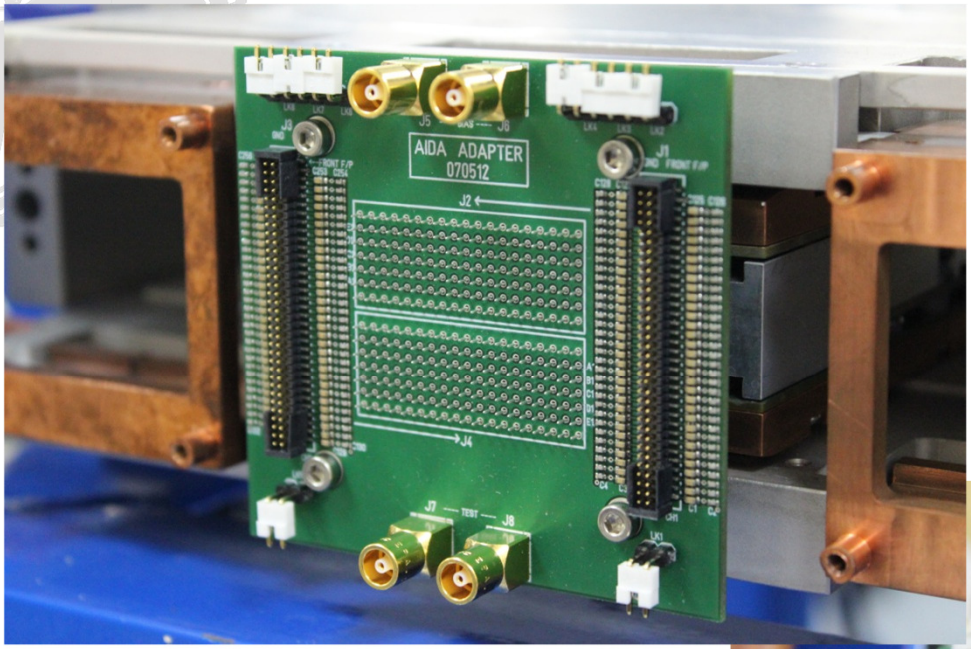
Power Supply Unit (bottom) controlled by Relay unit (top).
Note Raspberry Pi on top of Relay Unit which provides remote control via web

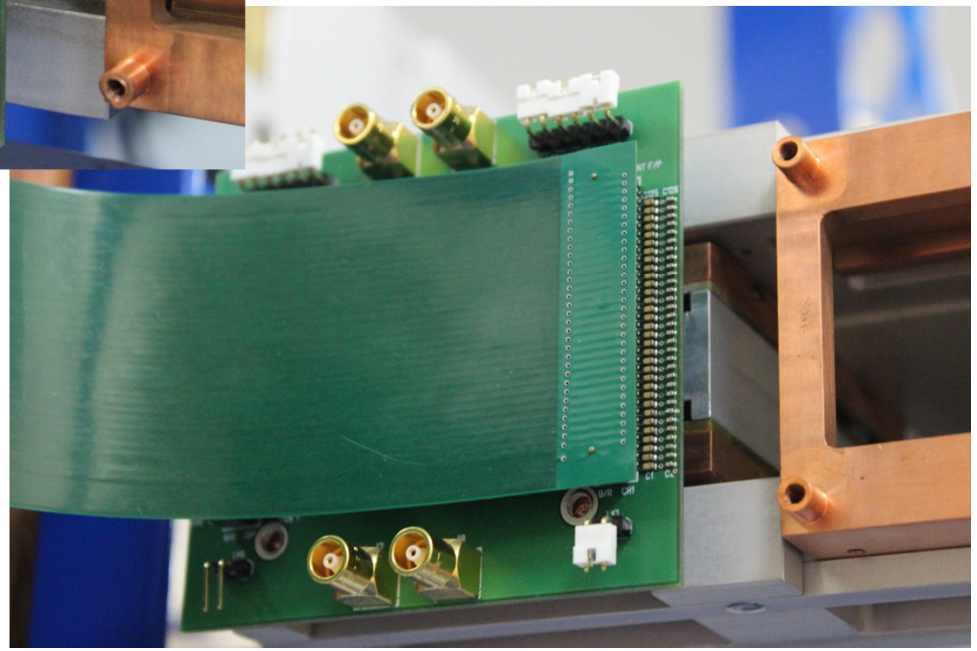
AIDA: Relay Control

AIDA: MSL type BB18-1000 + Kapton cabling



AIDA: Adaptor PCB with Kapton Cabling





Acknowledgements

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AIDA: Project Partners

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- The University of Liverpool
  Rob Page *et al.*
- STFC DL & RAL
  John Simpson *et al.*

Project Manager: Tom Davinson

Further information: http://www.ph.ed.ac.uk/~td/AIDA

TDR - November 2008:
http://www.ph.ed.ac.uk/~td/AIDA/Design/aida_tdr.pdf