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AIDA and LYCCA FEE

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Overview:

1. What are AIDA and LYCCA?
2. AIDA DSSD layout
3. AIDA ASIC
4. AIDA FEE Card
5. AIDA System Concept
6. Status

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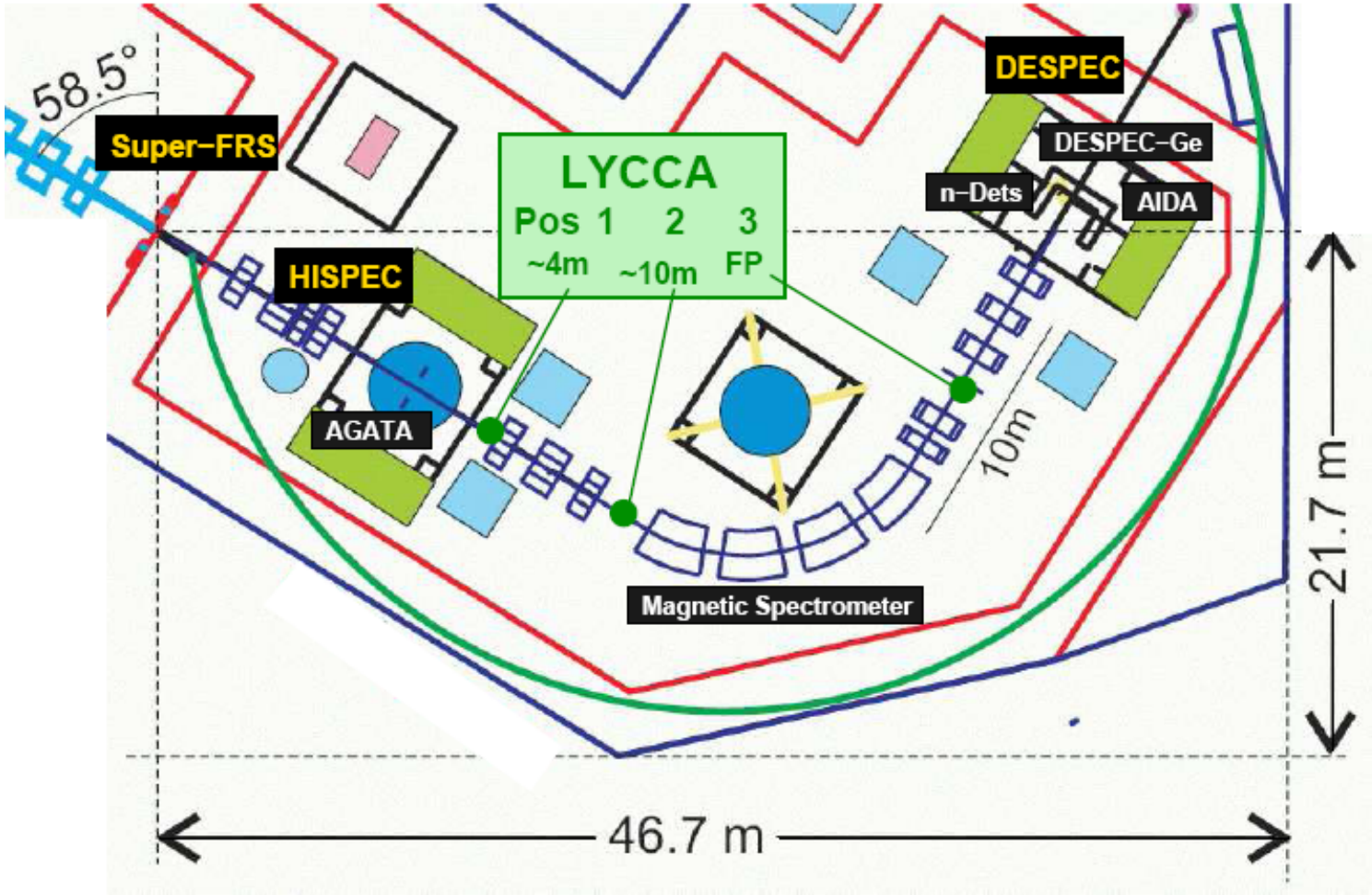
Possible LYCCA Locations



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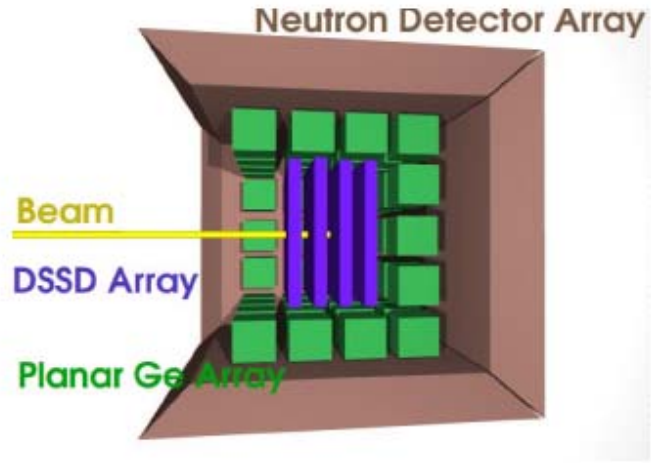
Advanced Implantation Detector Array (AIDA)



- Super FRS Low Energy Branch (LEB)
- Exotic nuclei – energies ~50-150MeV/u
- Implanted into multi-plane DSSD array
- Implant - decay correlations
- Multi-GeV DSSD implantation events
- Observe subsequent p, 2p, α, β, γ, βp, βn … decays
- Measure half lives, branching ratios, decay energies …
- DSSD segmentation ensures average time between implants for given x,y quasi-pixel >> decay half life to be observed.
- Implies quasi-pixel dimensions ~ 0.5mm x 0.5mm

Original slide from Tom Davinson

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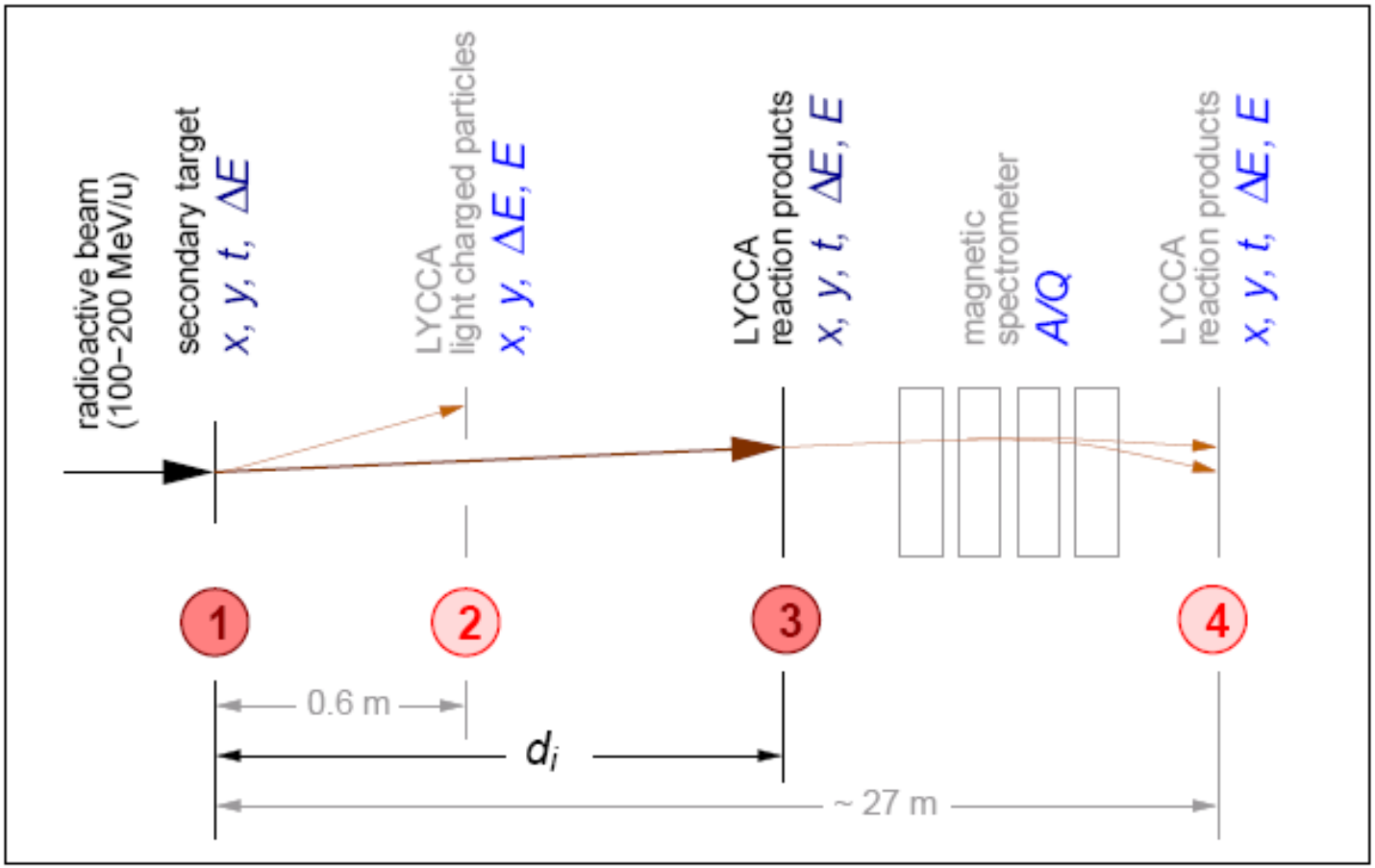
LYCCA Scheme



Slide from Dirk Rudolph

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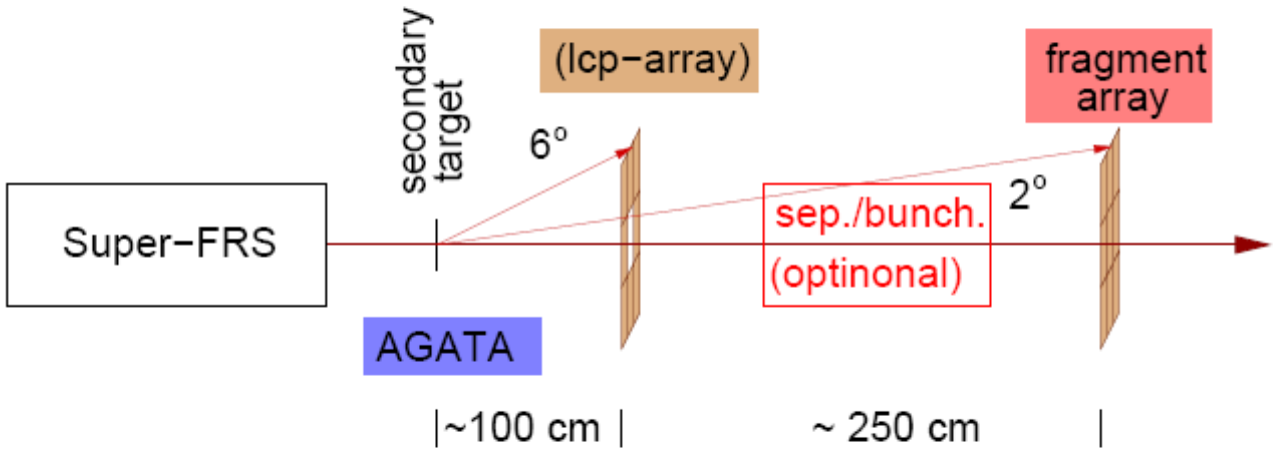
Lund–York–Cologne CAlorimeter (LYCCA)

Fragment identification after the secondary target

High–resolution fragment – gamma (– particle) spectroscopy



3 x 3 modules
hole in the center

5 x 3 mod. (wall)
8 x 2 mod. (f.p.)

50–100 MeV/u range

Distance secondary target – fragment array: ~3.5m

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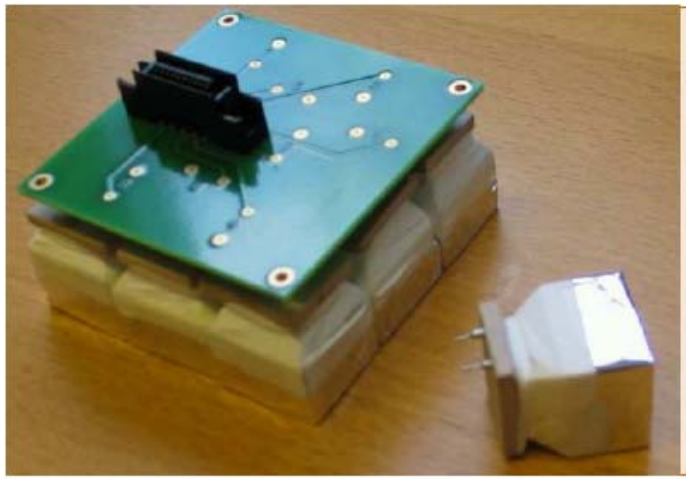
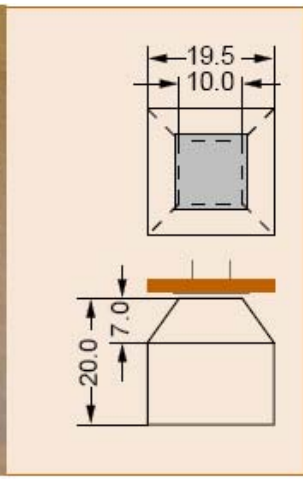
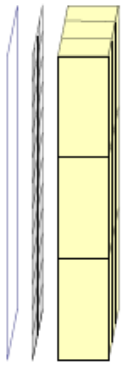
Detectors:





fragments

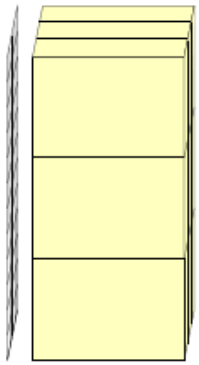
x,y
Δt ΔE E $\}Z,A$



ultra fast plastic or CVC diamond
DSSD
CsI

light charged particles

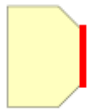
x,y
ΔE E



DSSD
CsI

DSSD: 6cm x 6cm
~0.5 mm
32 x 32 strips

CsI: 2cm x 2cm
~ 10 mm (frg)
~ 30 mm (lcp)



1. CVC diamond: 6cm x 6cm ~0.1−0.2 mm
2. ultra fast plastic: ~1cm strips ~12cm long
3. DSSD signal from one side

Pictures from Dirk Rudolph

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LYCCA Electronics

Electronics channels (as of 15.02.06/15.09.06):

DSSD (*ΔE*):

LCP	512	range 0-10 MeV	use extra batches of
HI	~1000	range 0.1-5.0 GeV	DESPEC Si-ASIC?

CsI (*E*):

LCP	72	range 0.01-1.0 GeV	sampling ADCs
HI	~150	range 1.0-30.0 GeV	type CAEN 1724?

Ultra fast scintillators or CVC diamond (*Δt*):

HI	~32	or	~16

LYCCA-0 at RISING: (new) preamps, mesytec shapers, VME
LYCCA at HISPEC: CsI: re-use the above
Si: AIDA ASICs.

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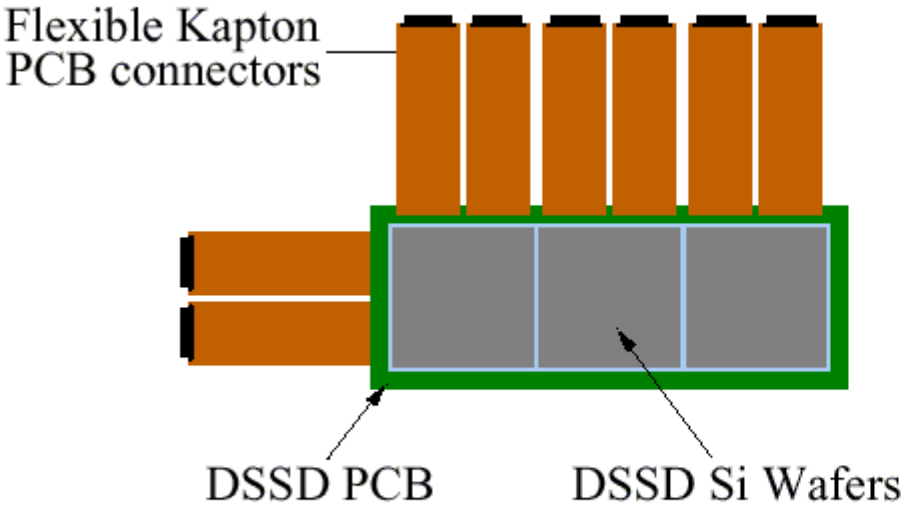
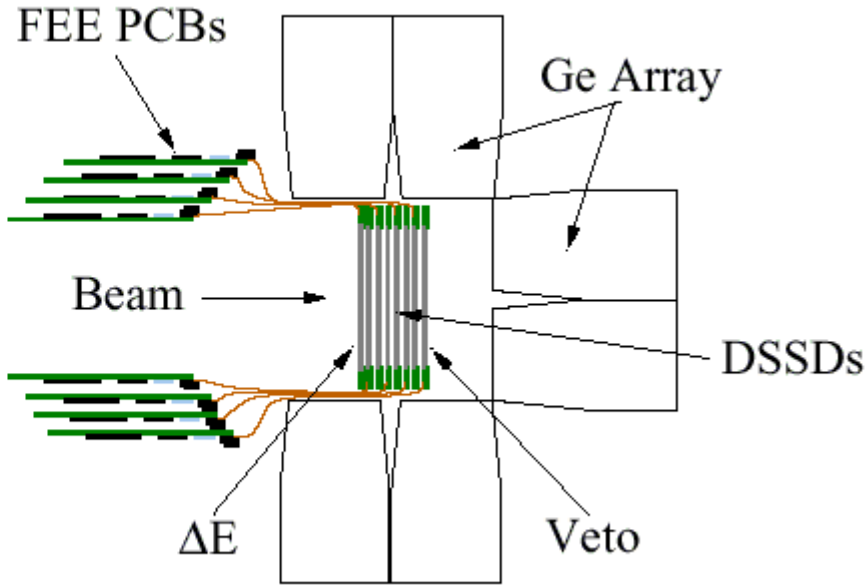
AIDA General Arrangement





Implantation detector for RDT

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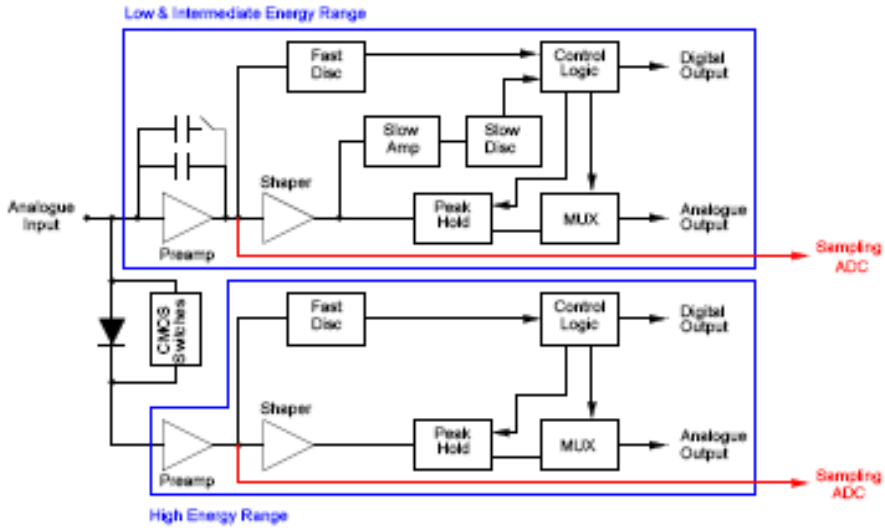

Figure 2: Schematic diagram of the functionality of one ASIC channel

AIDA ASIC:

- 625um pitch
- 8/16 channels
- 2 channels/strip
- Mux'ed analogue ouput
- Direct digital output for external FADC
- 2 ranges: 0-20MeV/1GeV and 0-20GeV

Why do we control ASIC & readout with FPGAs?

- FPGA = Field programmable gate array
- Flexible (reprogrammable in situ to change function or fix bugs)
- Fast (>1Gbyte/sec using multiple output paths)
- Handles control logic and clocks easily
- Handles data transfer easily and fast
- Built in IP for Ethernet (Virtex 4) and PCIe (Virtex 5)
- Reasonable expectation of common development (shared IP) for NUSTAR interfaces to slow control, readout and BUTIS timestamping.

- Design studies are well under way for:
  - Fast recovery ASIC
  - Readout card
- Specification includes:
  - 4096 channels in total (128 or 64 per FEE card)
  - ASIC Ranges 0-20Mev, 0-1GeV, 0-20GeV
  - ASIC threshold 50keV-2MeV on 20MeV range
  - ASIC Recovery from HI implant- few us
  - 200MHz (5ns) Timestamp
  - Readout via Gbit Ethernet (1 per 64 or 128 channels)
  - Data rate (if we read traces from FADC) is approx 1.5 to 3 Mbytes/sec max; 45-90kB/sec/128 channel card

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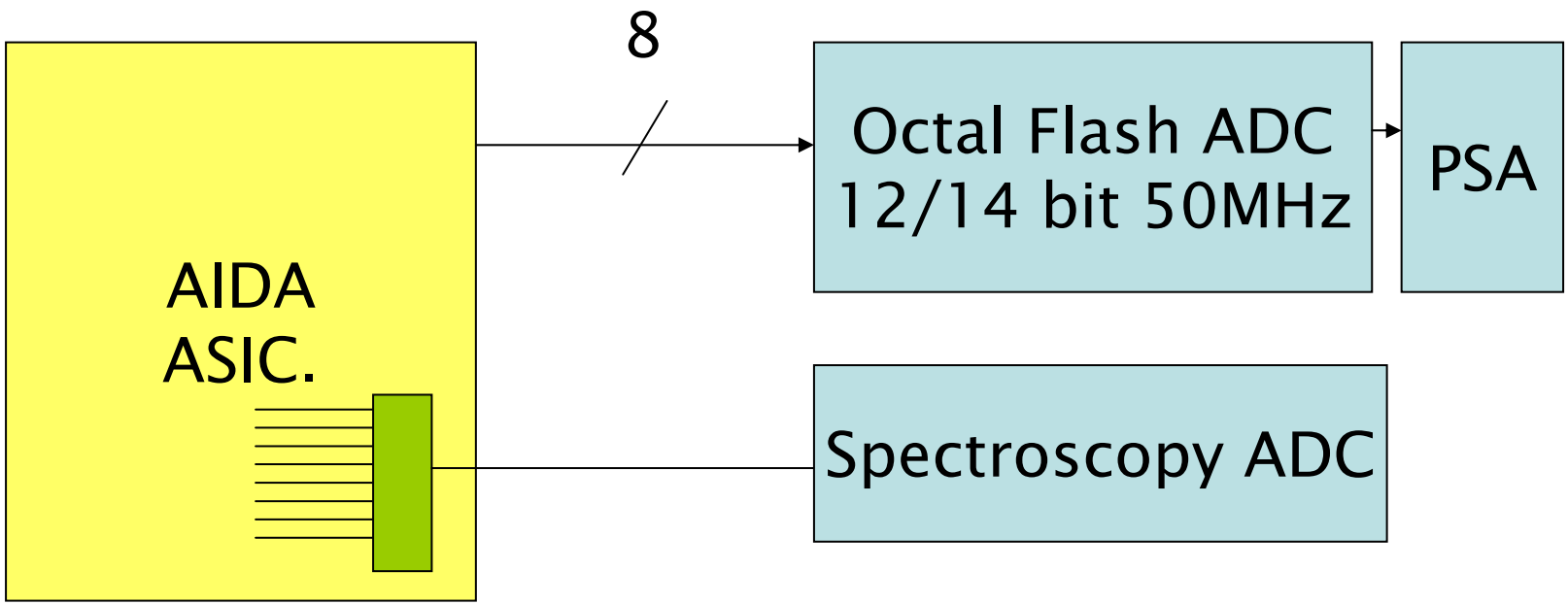
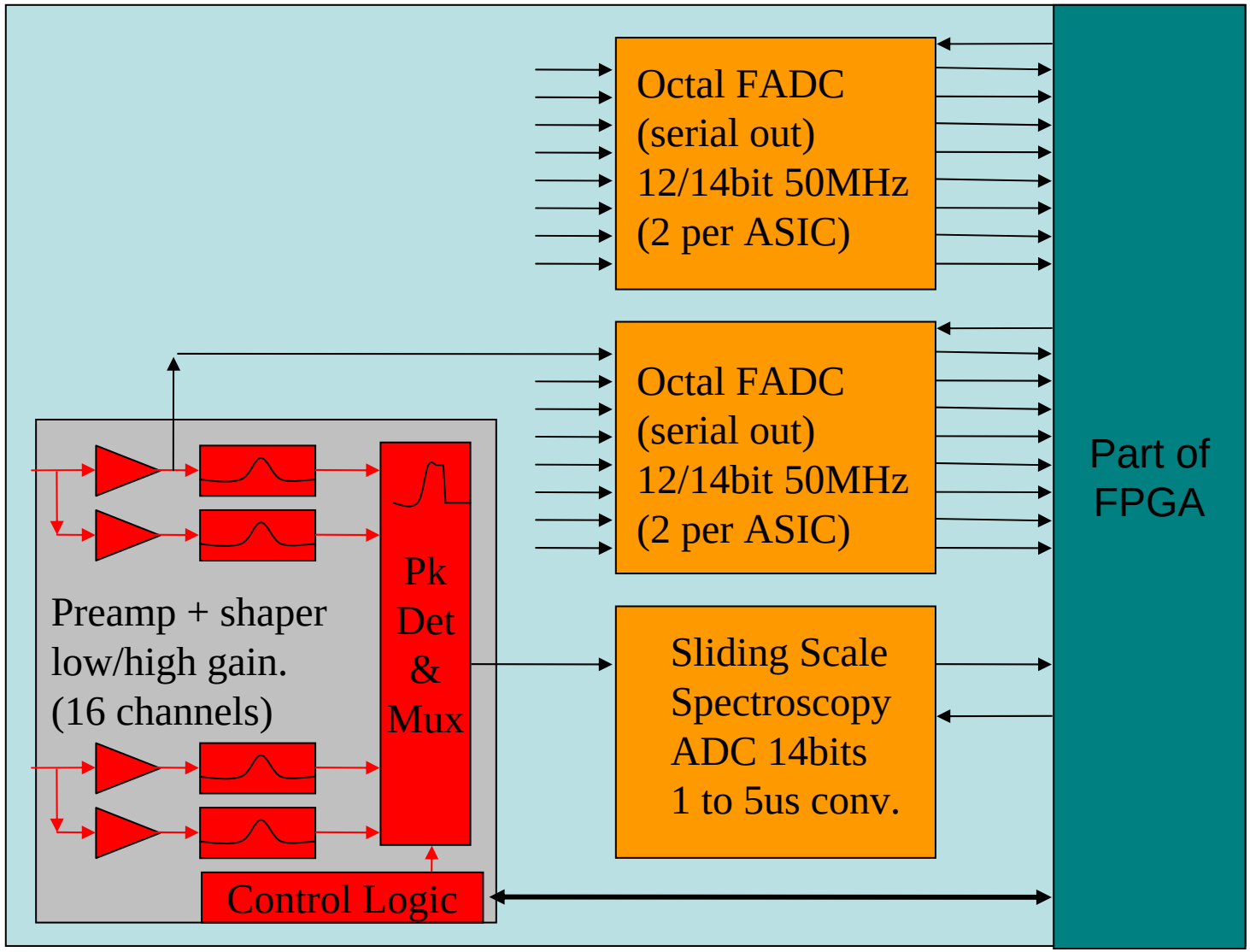
AIDA ASIC readout paths.




Octal FADC
(serial out)
12/14bit 50MHz
(2 per ASIC)
Octal FADC
(serial out)
12/14bit 50MHz
(2 per ASIC)
Part of
FPGA
Preamp + shaper
low/high gain.
(16 channels)
Pk
Det
&
Mux
Sliding Scale
Spectroscopy
ADC 14bits
1 to 5us conv.
Control Logic

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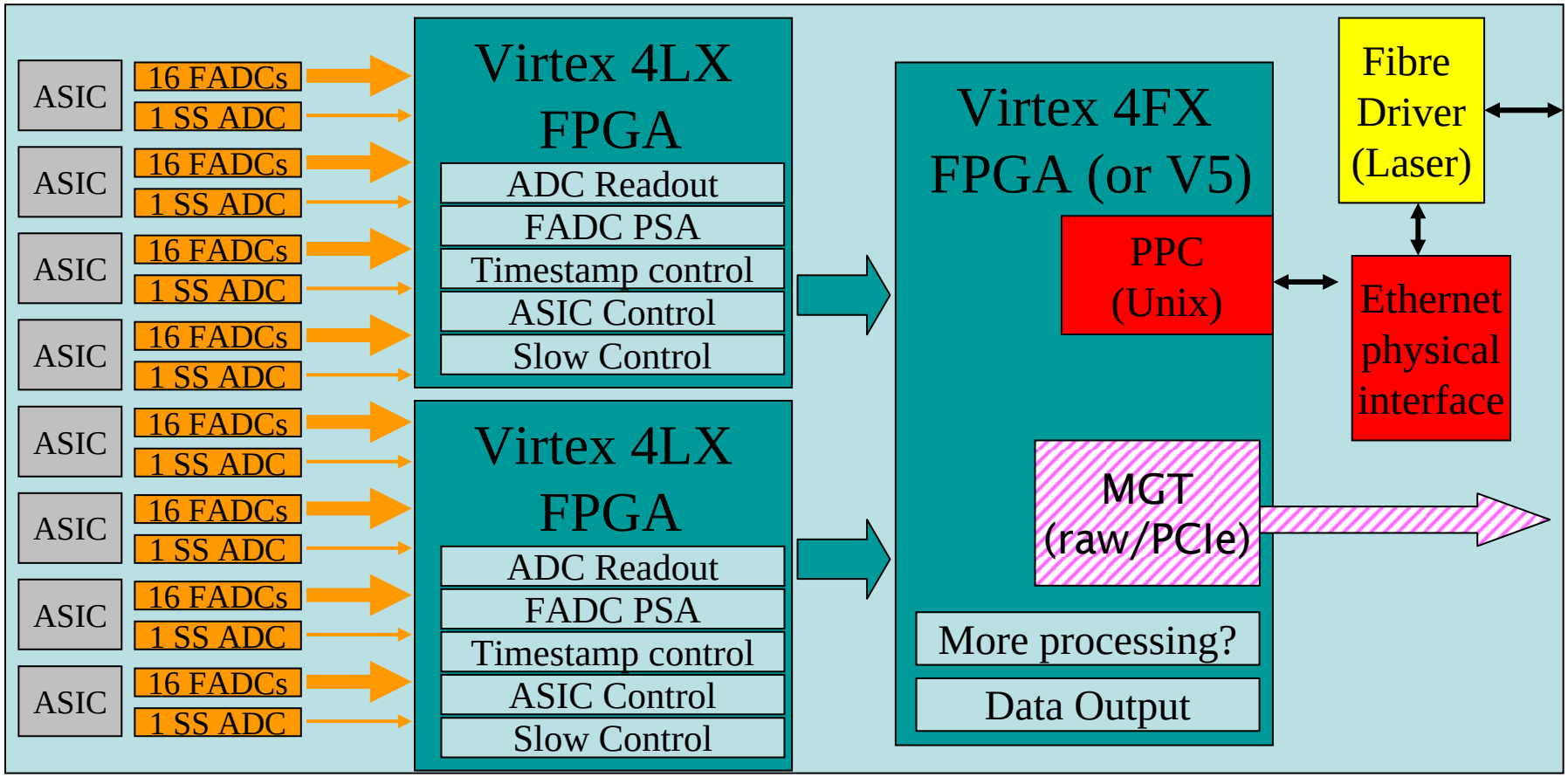
16 ch ASIC

16 FADCs (12/14 bit) 1 Sliding Scale ADC (14bit) per ASIC

128 (64?) detector signals in; 1 data fibre out (max 50Mbytes/sec) or multiple MGTs with PCIe or point-point 200Mbytes/sec



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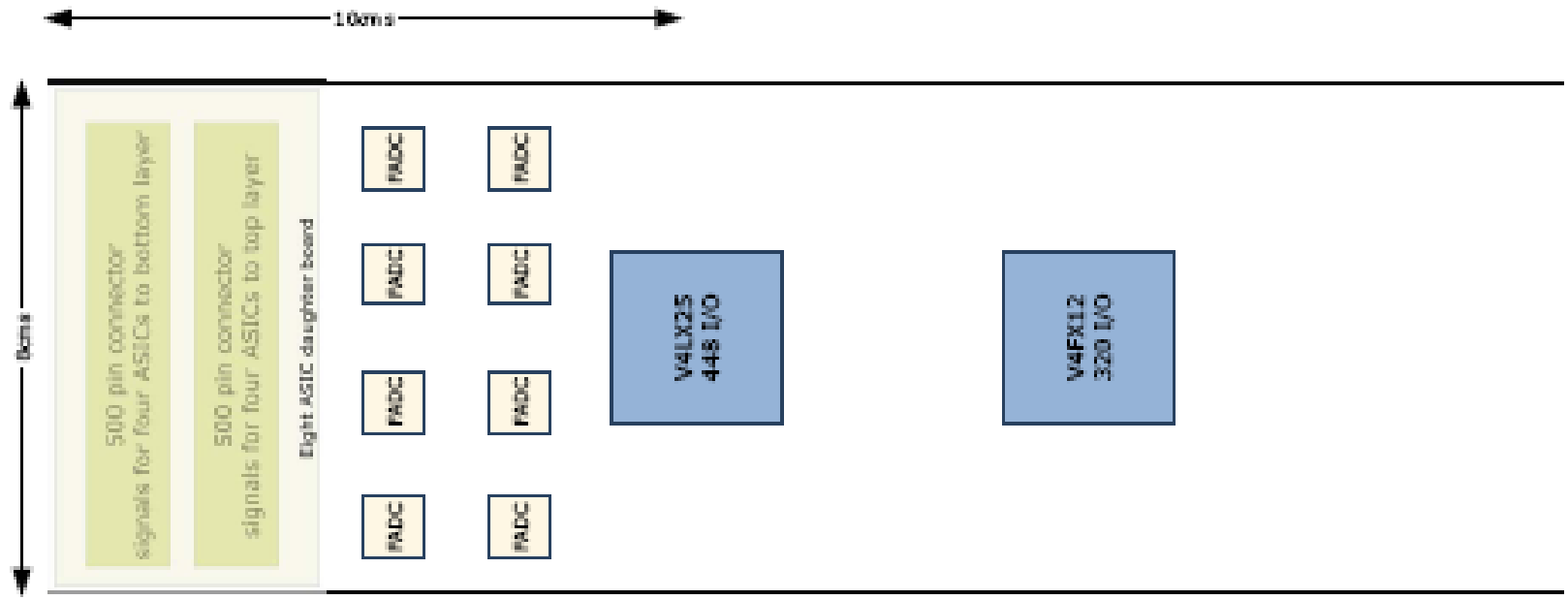
Proposed Physical layout of AIDA FEE card



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The 3 NUSTAR Docking Stations

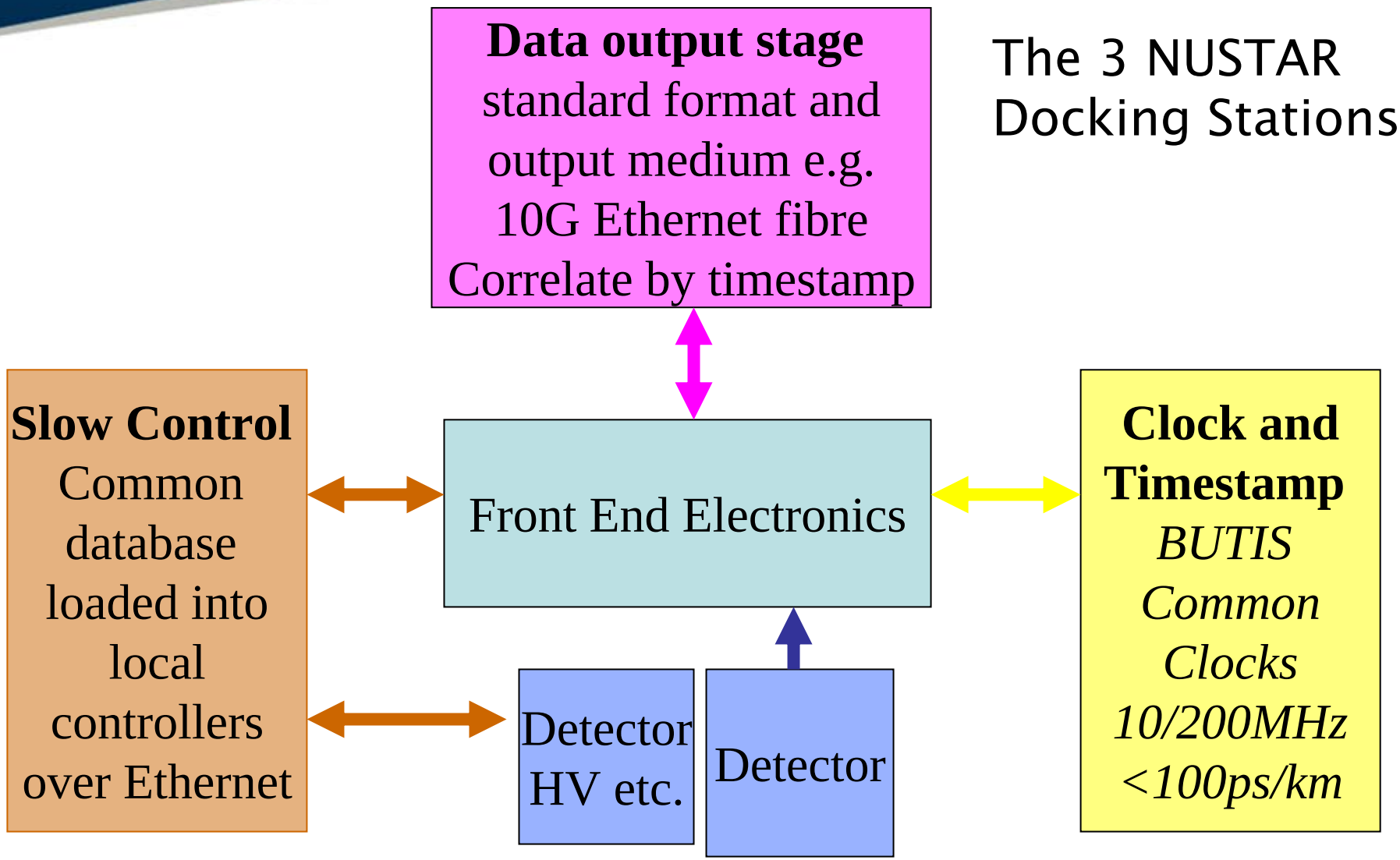

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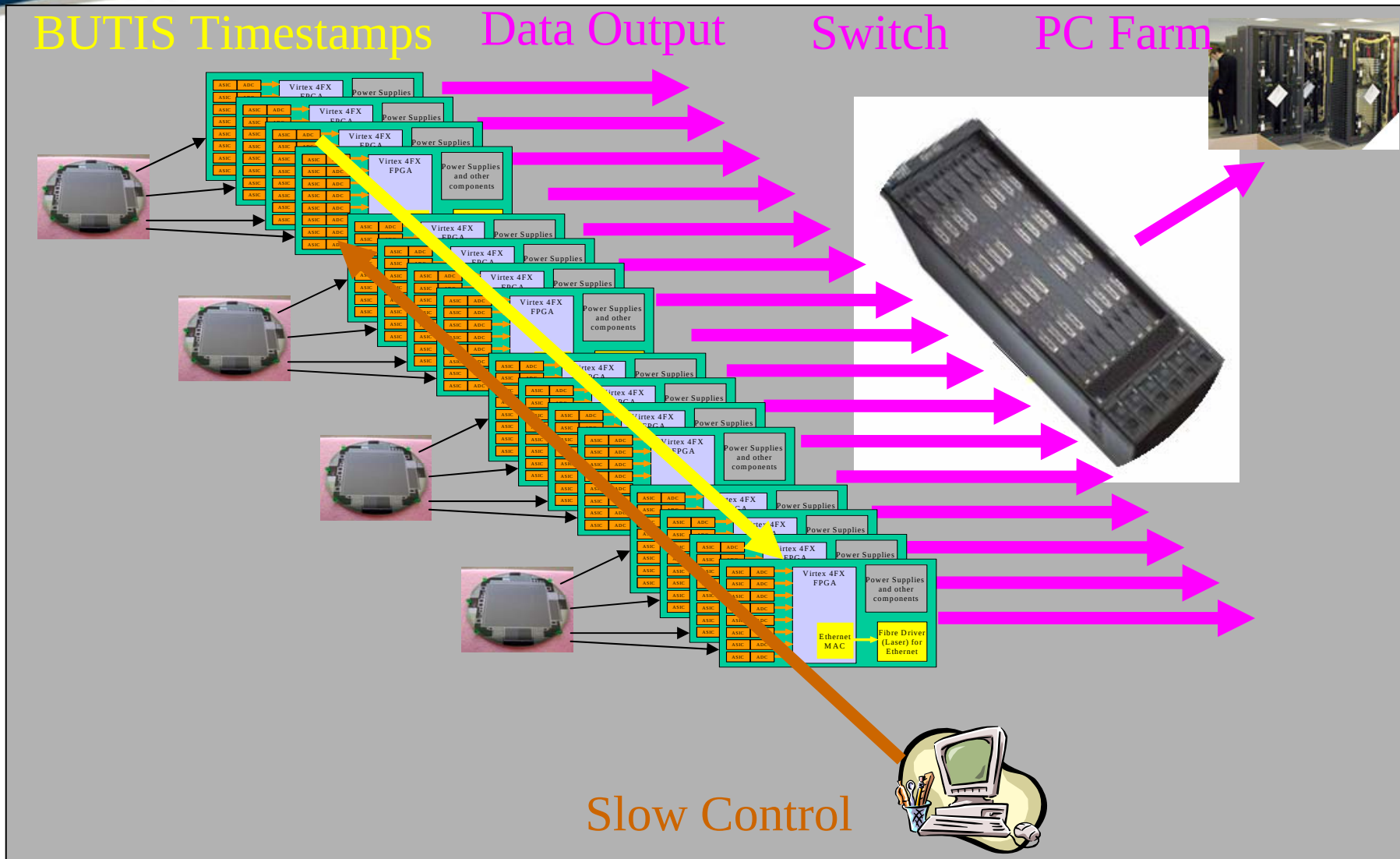
Diagram of half of AIDA system



AIDA (and LYCCA DSSD) FEE status

- Specification finalised (then revised Mar 07!)
- Detailed design starts this year (2007)
- Prototype tests (ASIC and readout) mid 2008
- DAQ using Gbit Ethernet from Virtex 4FX being developed for other projects too.
- Timestamp with BUTIS- least well defined area
- Expect to profit from sharing IP with other Hi/DeSpec and NUSTAR EDAQ for common interfaces.