AIDA detailed design

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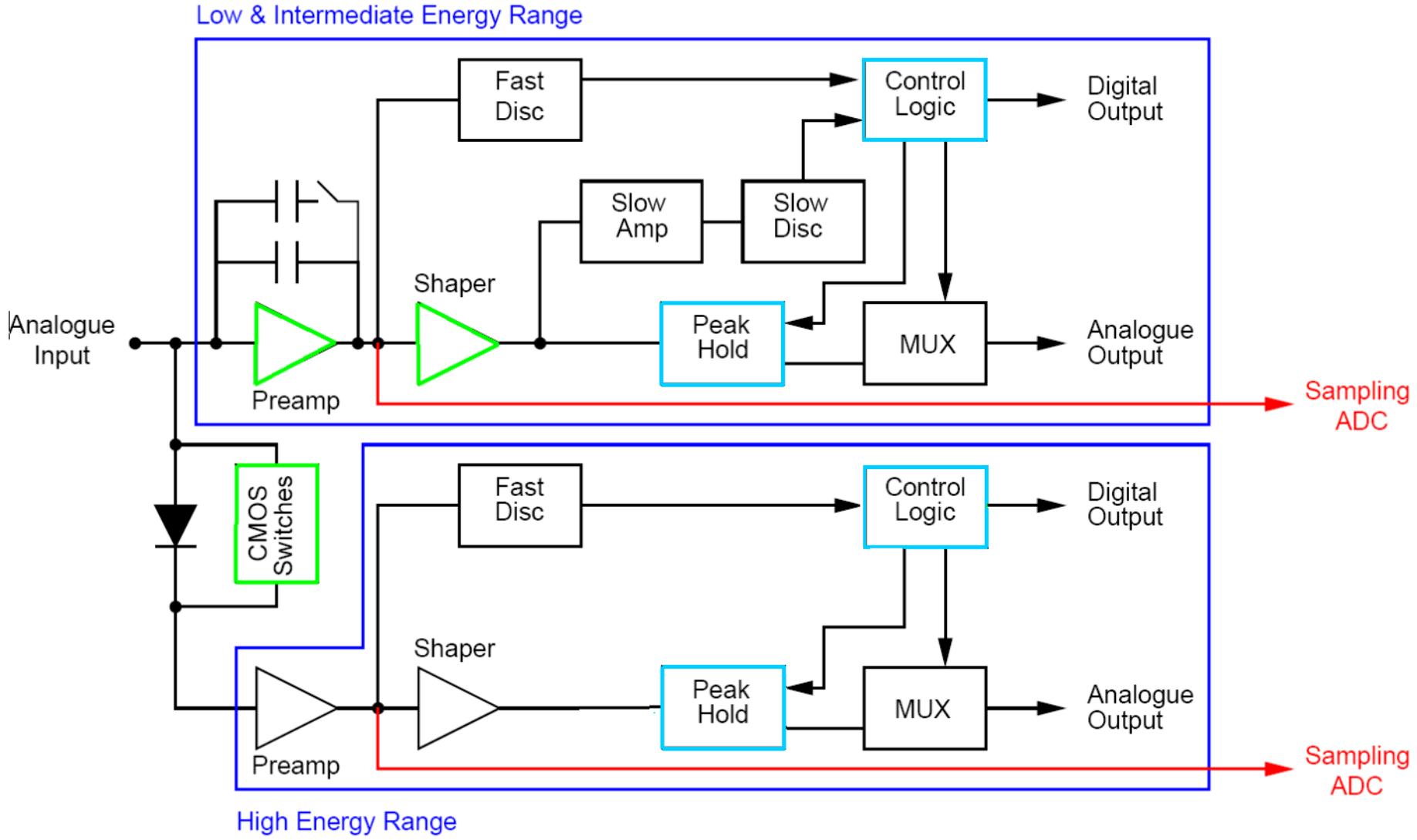

Low & Intermediate Energy Range
Fast Disc
Control Logic
Digital Output
Slow Amp
Slow Disc
Shaper
Analogue Input
Peak Hold
MUX
Analogue Output
Preamp
Sampling ADC
CMOS Switches
Fast Disc
Control Logic
Digital Output
Shaper
Peak Hold
MUX
Analogue Output
Preamp
Sampling ADC
High Energy Range

XFEL detector review meeting : 8 May, DESY

Detector carrier density identified as a major risk for electronic design (~50pC charge per pulse)

ESRF with XSTRIP read-out

- 20ps bunch, 2.82ns repetition rate, 1e9 photons/s per channel
- Average of 2.82 photons per bunch, 9400 e/h pairs per bunch
- 1e5 holes per channel in detector volume (~30ns hole drift time)
- Hole concentration **p~8e9 /cm^3**

XFEL

- 100fs bunch, 200ns separation (x 500), 100ms repetition
- 1e5 photons per channel per bunch, 5e8 per second
- 3e8 e/h pairs per 100fs (for 12keV X-rays)
- Hole concentration **p~3e12 /cm^3**

Silicon detector has N_D ~1e12 /cm^3

ESRF: p<<N_D, carriers have no effect on detector field

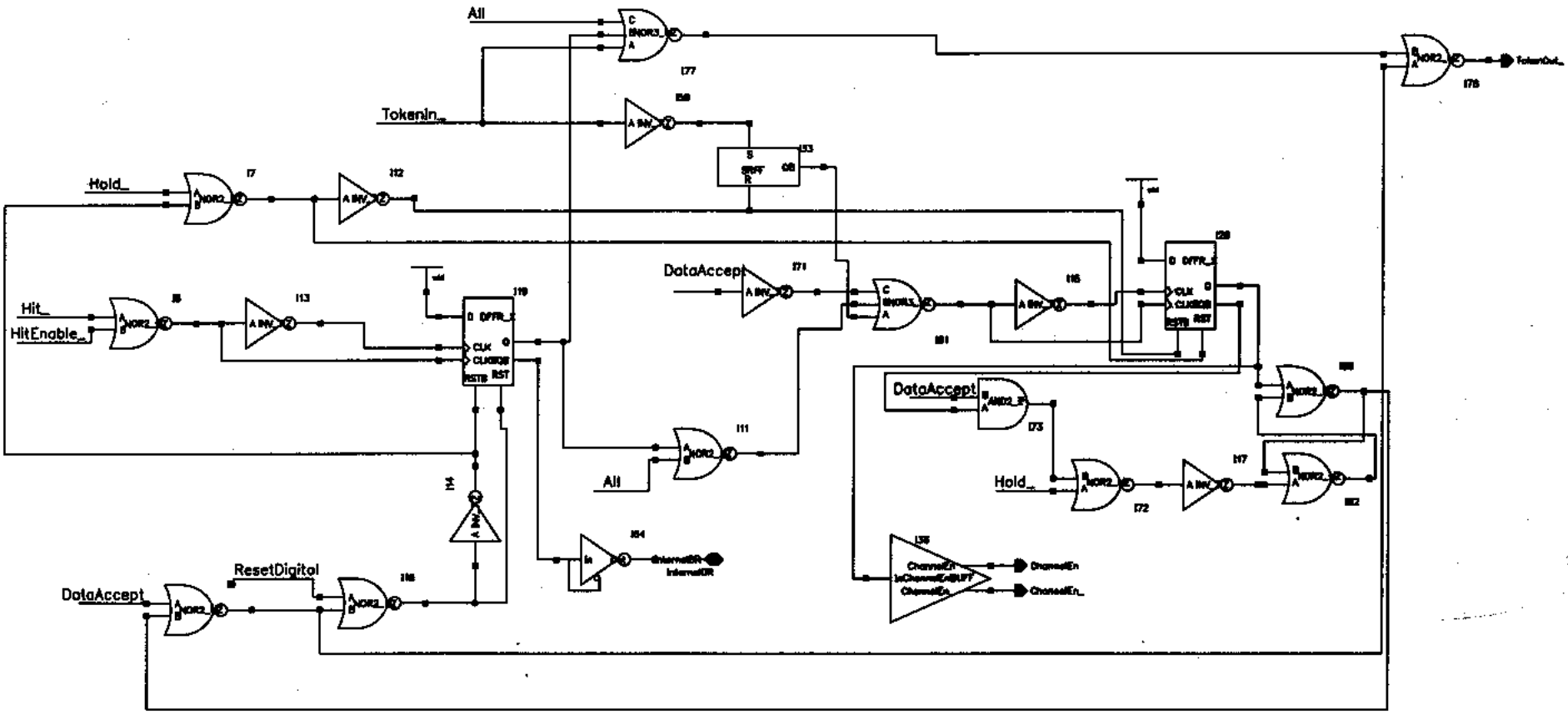
XFEL: p>>N_D, carriers can influence field:

risk of charge shielding effects, with recombination

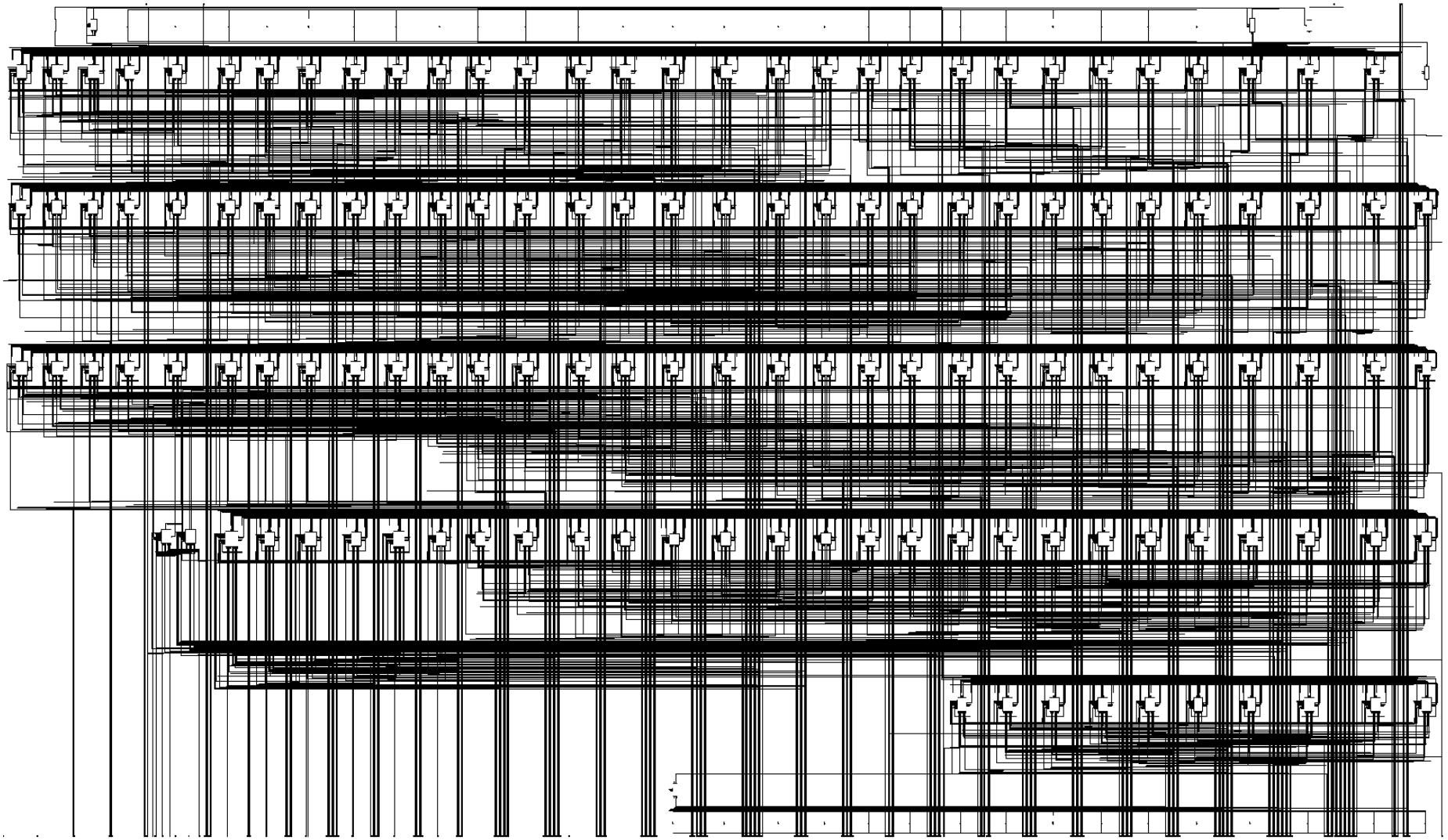
Detailed design issues:

- re-use of existing circuit blocks, optimised for linearity
- analogue behavioural models (faster for top level simulation)
- high-level digital models (Verilog), with synthesis of schematics
- semi-custom digital layout

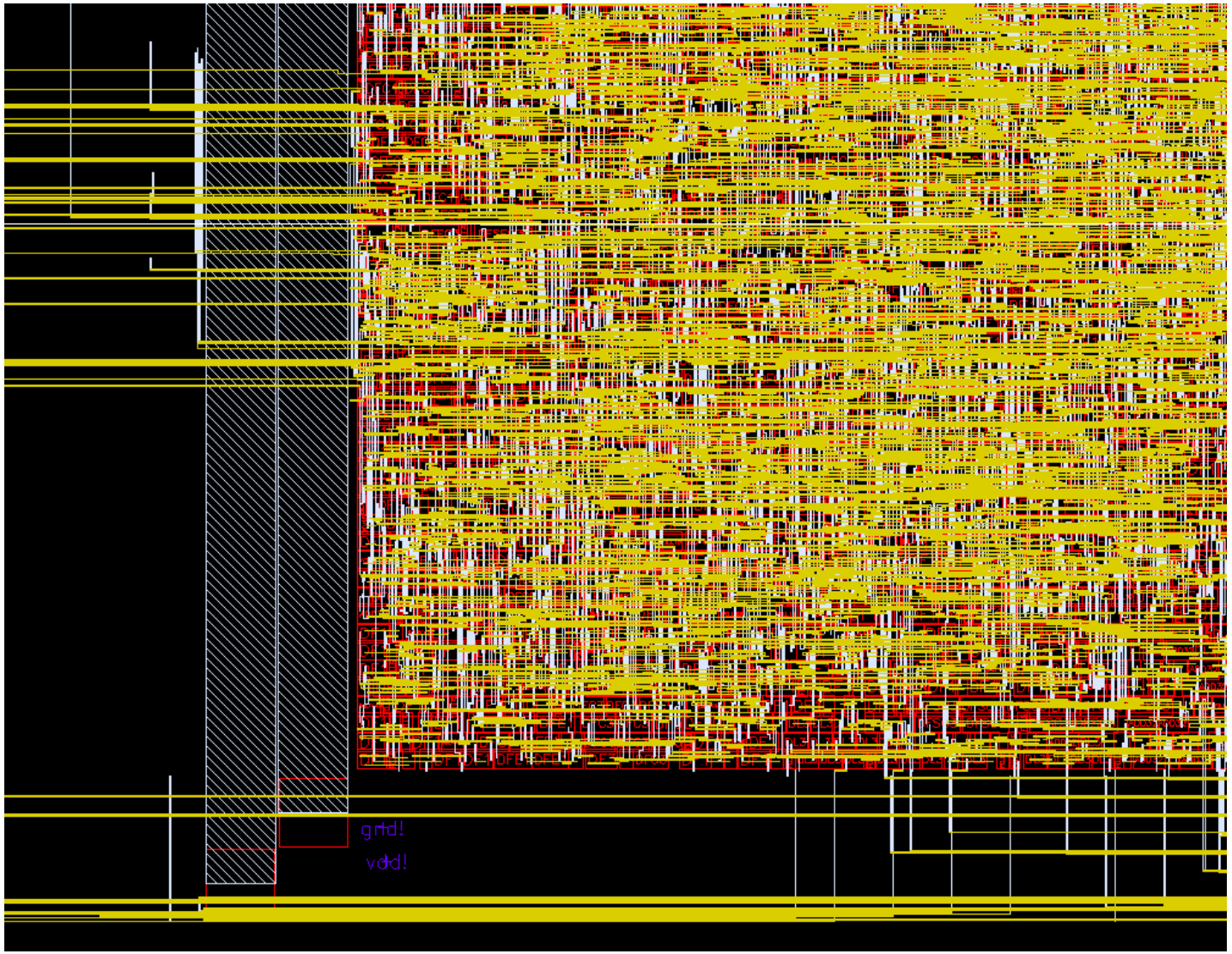
Digital design: sparse read-out (1997)



Digital design: sparse read-out (2007)

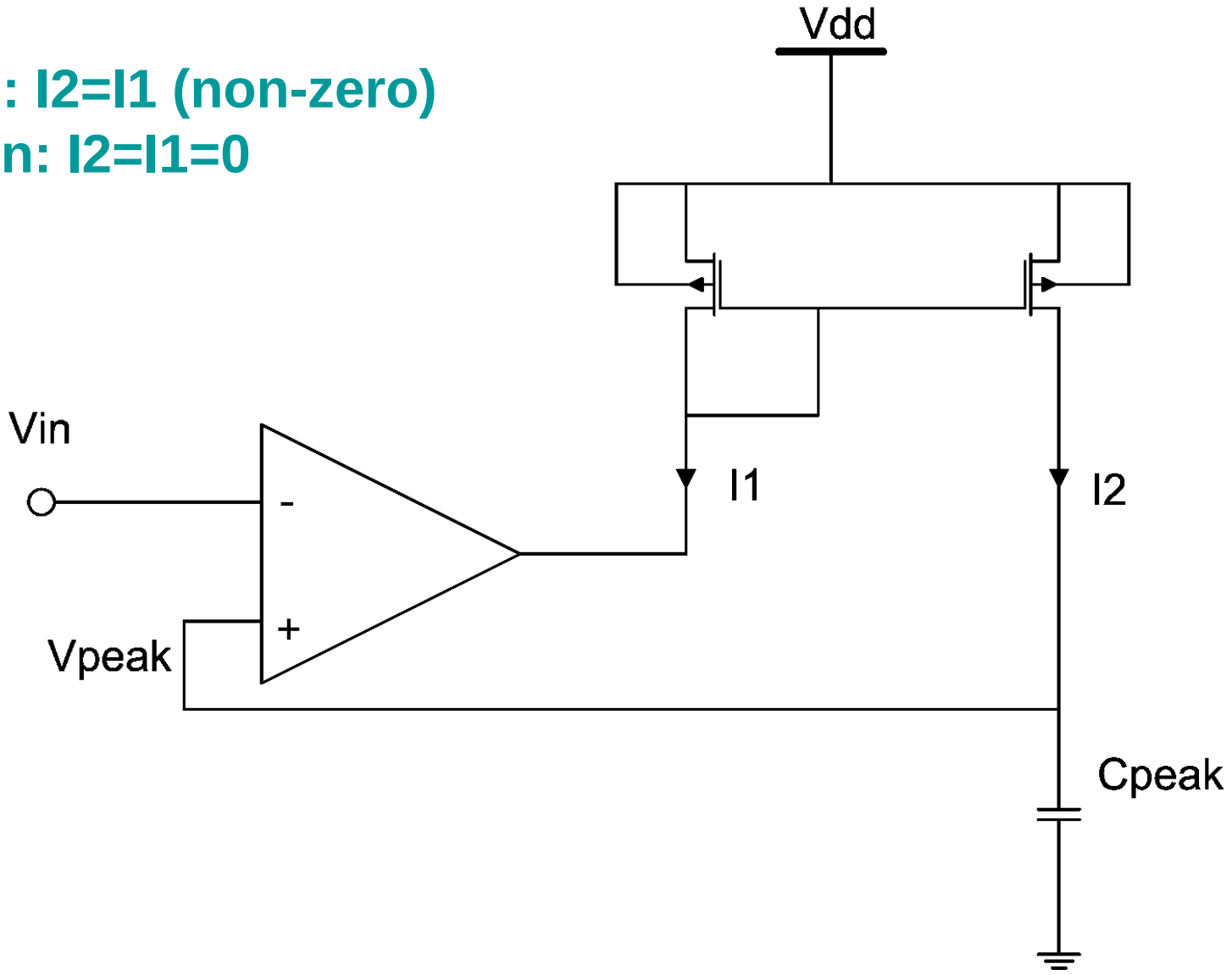


Digital design: automatic layout

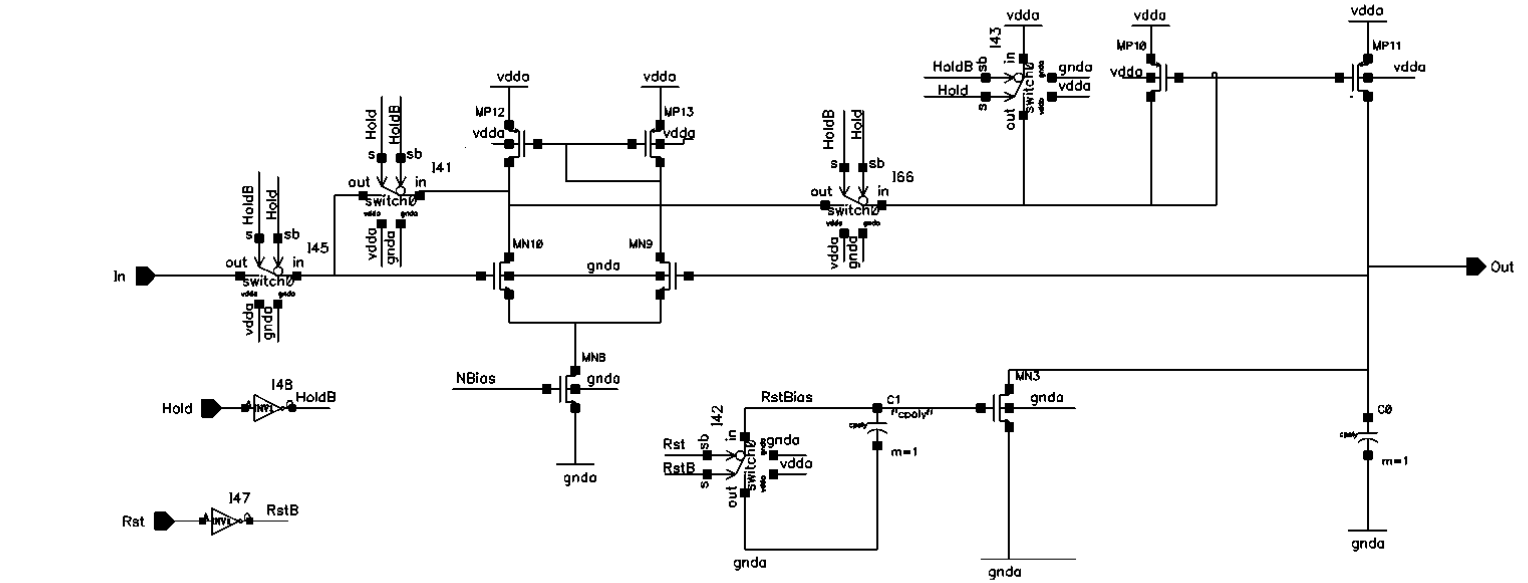


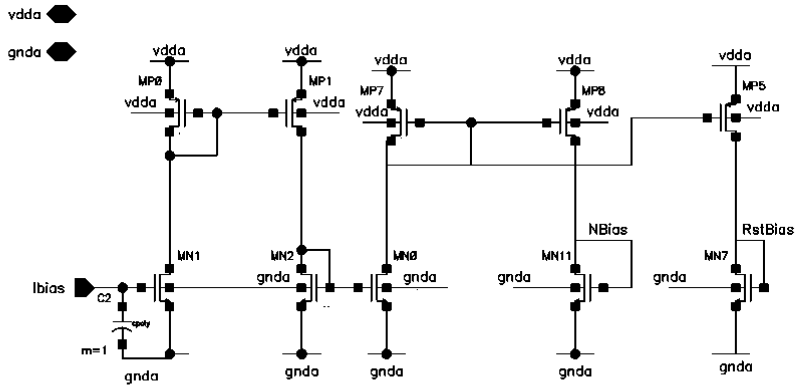
Peak hold circuit

Vpeak<Vin: I2=I1 (non-zero)
Vpeak>=Vin: I2=I1=0



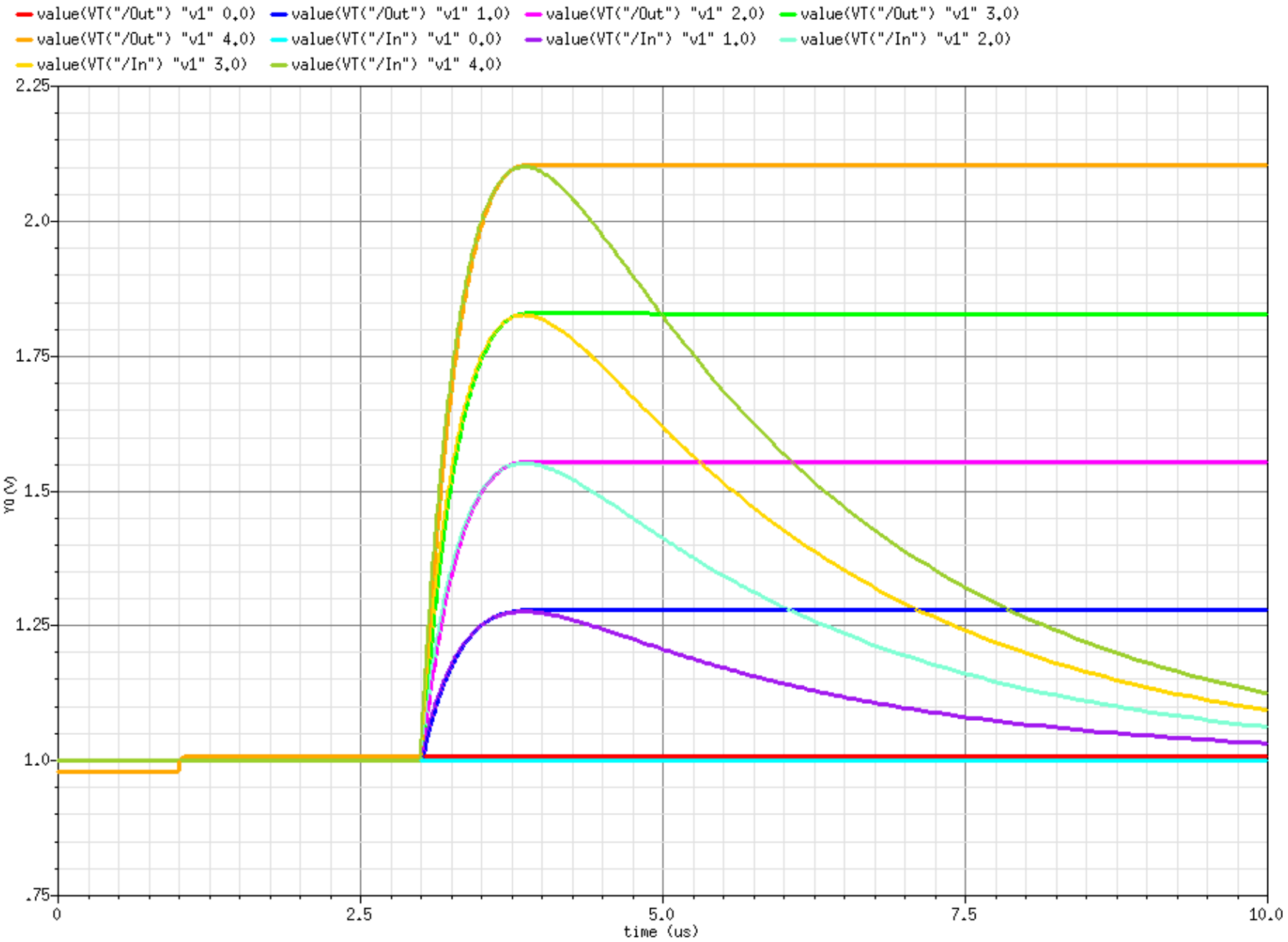
Peak hold circuit - full version



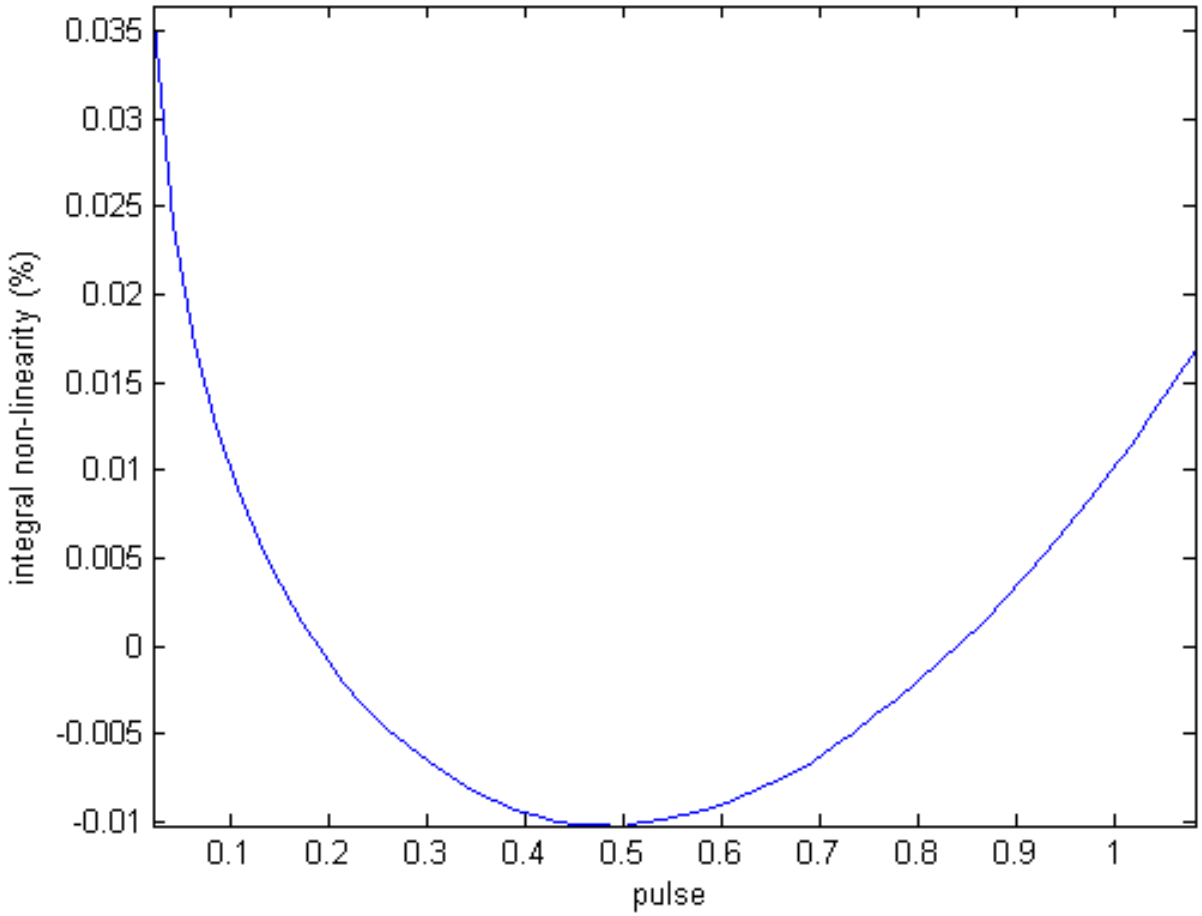


STFC Technology	ASIC Design Group
Project	AIDA
Library Name	AIDA_sim
Block Name	aida1_peakHold1
Last QA Review	
Last Changed	May 11 16:08:14 2007

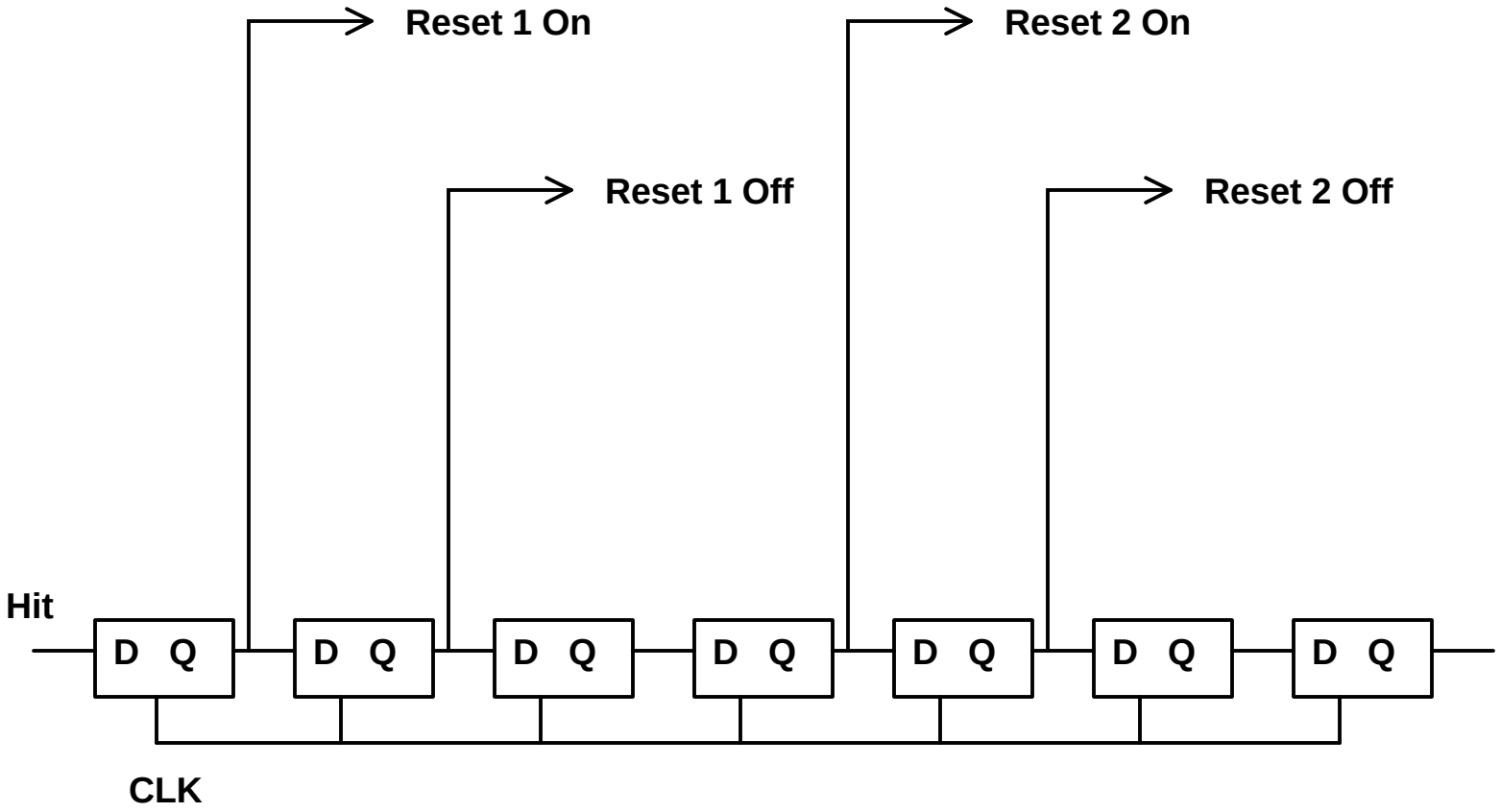
Peak hold simulation



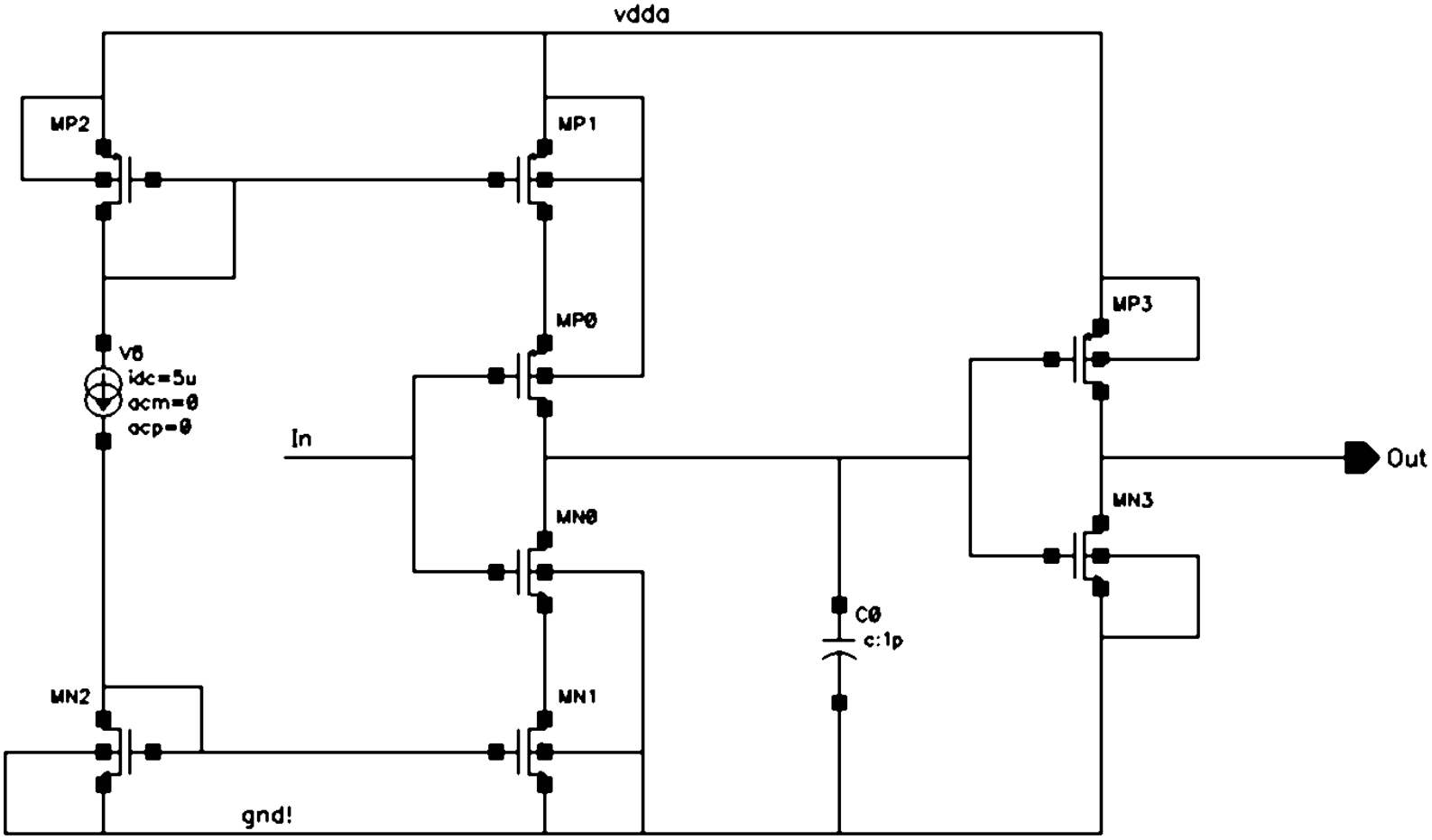
Peak hold linearity



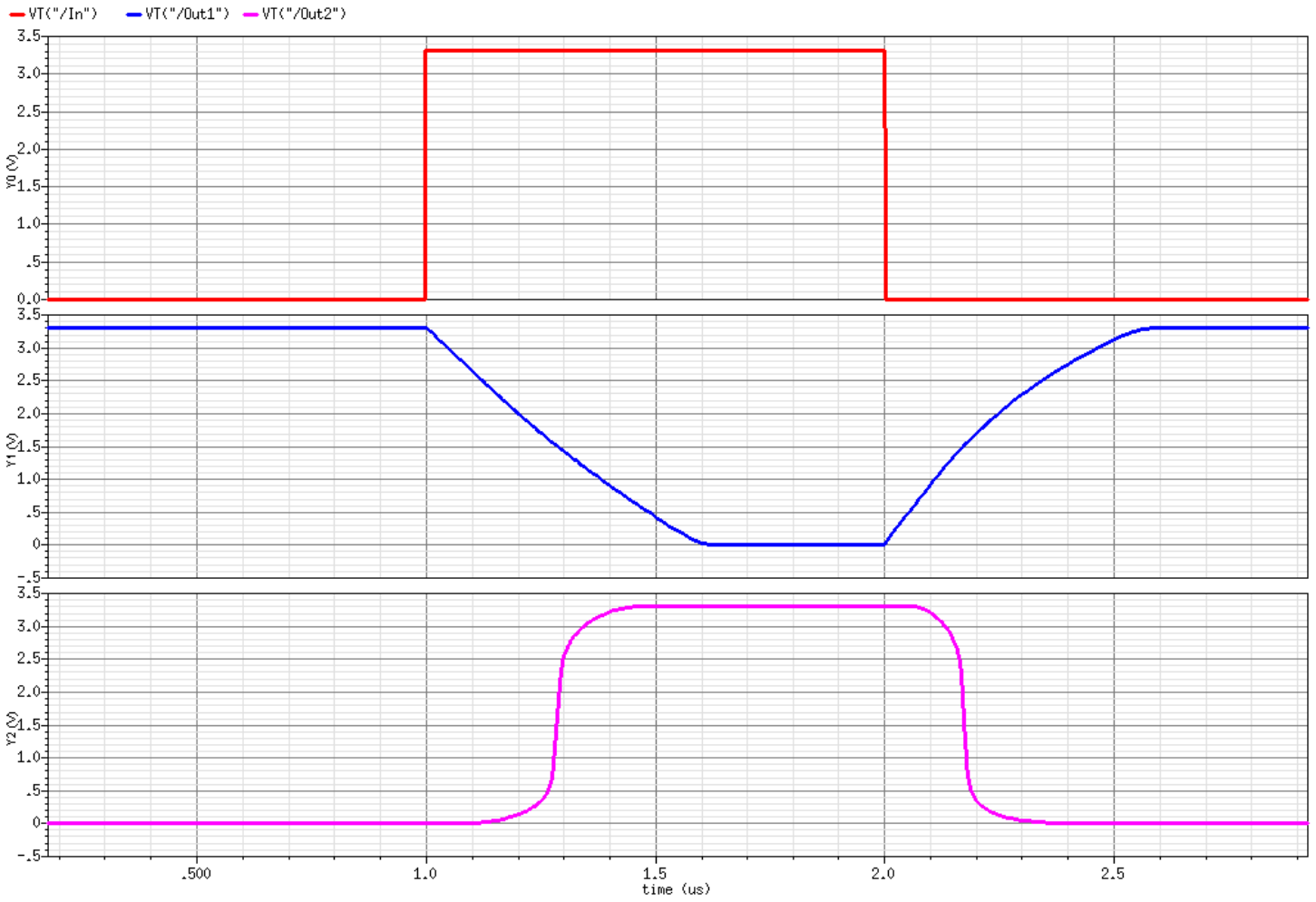
Digital delay 1: Shift register



Digital delay 2: Current limited inverter



Digital delay 2: Current limited inverter



Conclusions:

- Detector simulation important (XFEL)
- Linearity maintained with peak-hold
- Two options for reset sequencing (digital or analogue)
- Two options for digital design (traditional approach or synthesis)