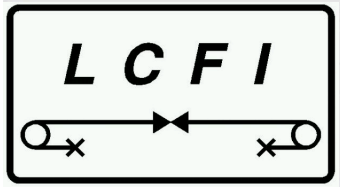


Heavy Flavour Identification at the ILC

Experimental Particle Physics Seminar

University of Edinburgh

26th January 2006

Joel Goldstein

CCLRC Rutherford Appleton Laboratory

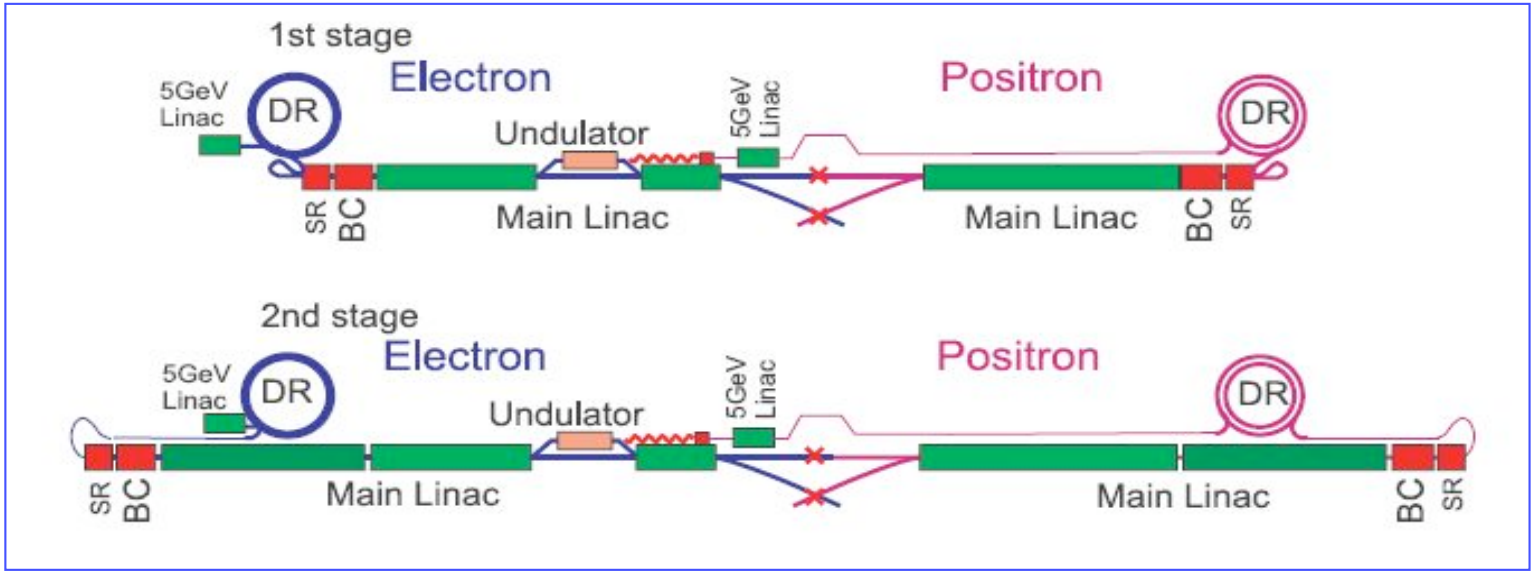
Outline

1. Introduction to the ILC and Heavy Flavour ID
2. *LCFI* Research Programme:
   - I. Simulation and Physics
   - II. Mechanical Development
   - III. Sensor Development
3. Summary

The International Linear Collider

500-1000 GeV e^+e^- collider

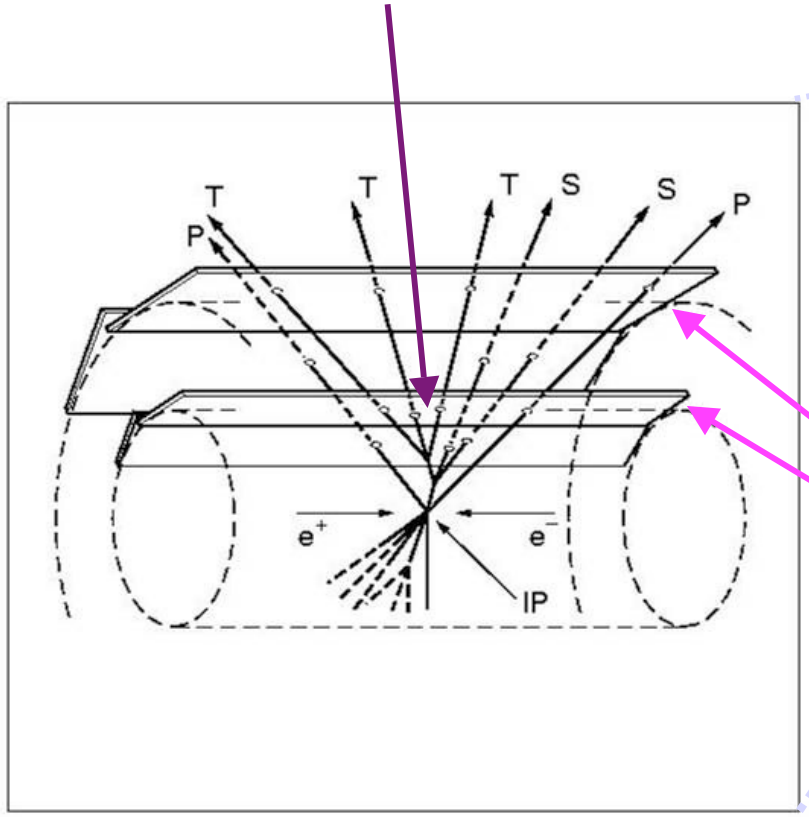
- Superconducting RF
- Start in ~2015

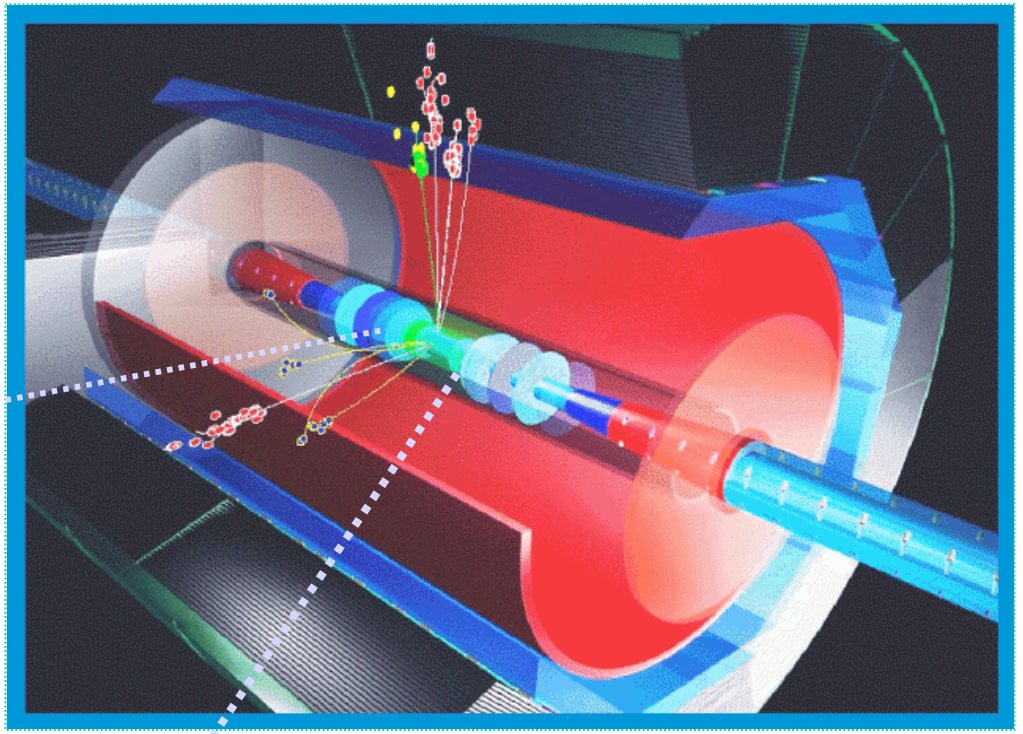


- Complimentary to LHC:
  - Precision measurements
  - Searches
- Many physics channels require excellent *heavy flavour ID*
  - *Higgs, SUSY, Top....*

Heavy Flavour Identification

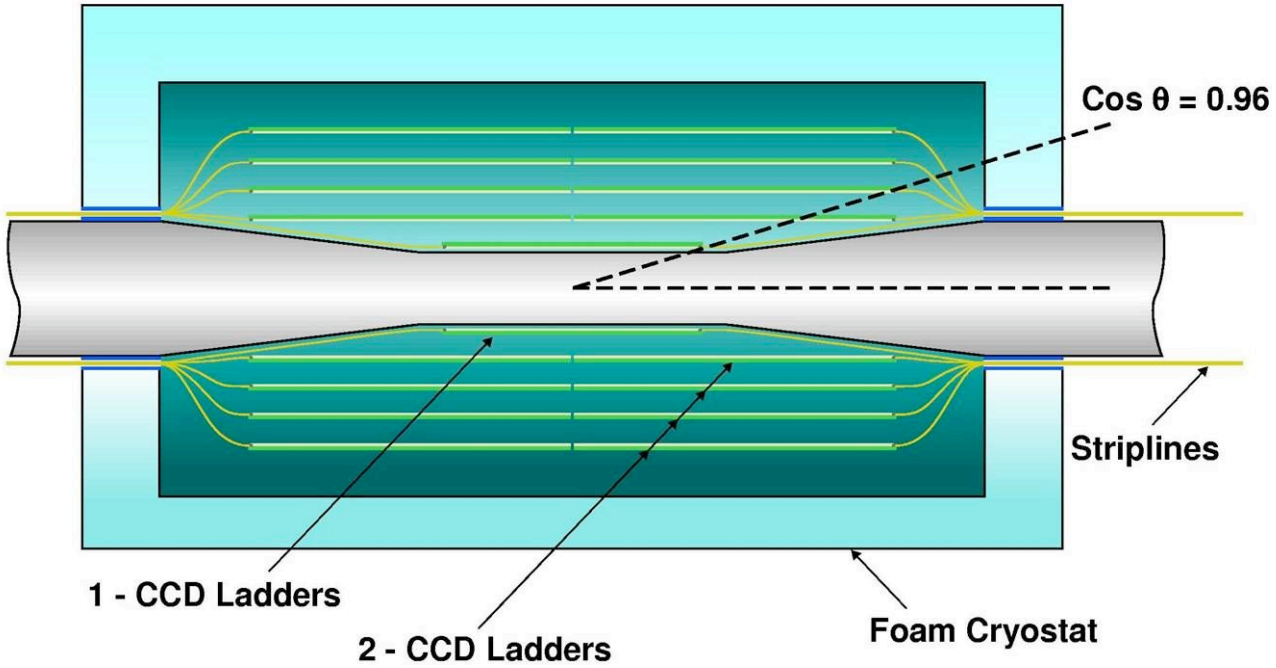
Heavy flavour particles with lifetime ~1 ps (τ, *b* and *c*) travel a few mm then decay.





Precision silicon detectors can reconstruct decay vertices.

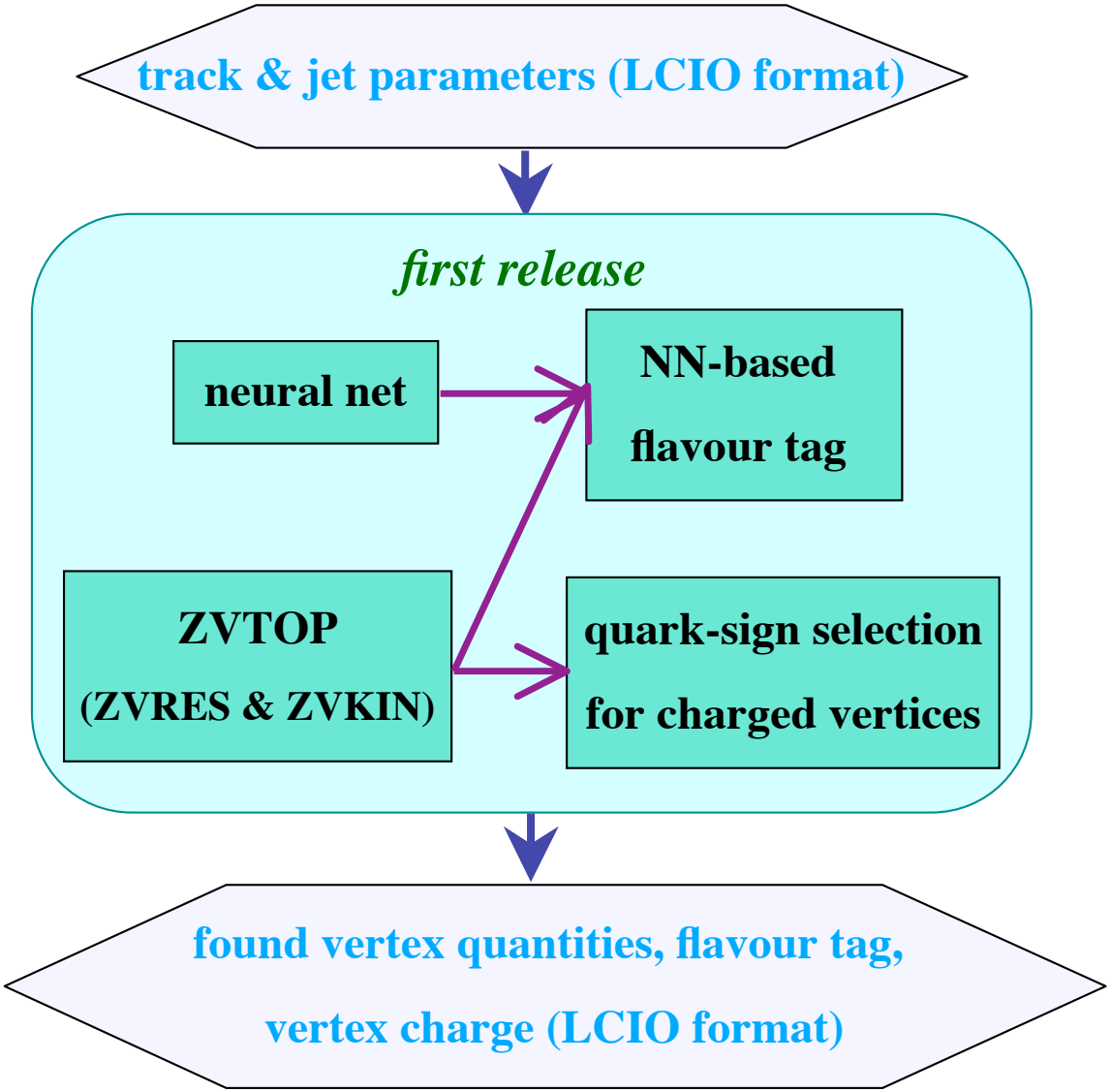
Baseline Vertex Detector



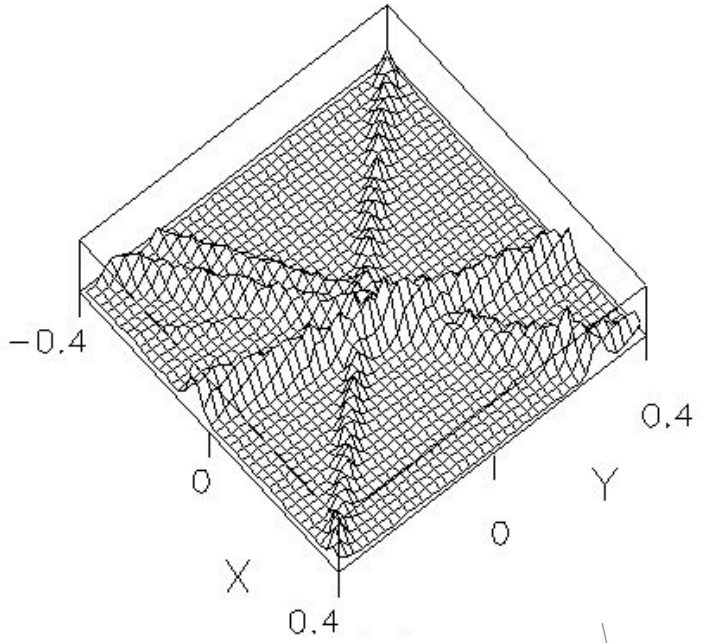
- 800 Mchannels of 20×20 μm pixels in 5 layers
- Optimisation:
  - Inner radius (1.5 cm?)
  - Readout time (50 μs?)
  - Layer thickness (0.1% X_0?)

Simulation and Physics

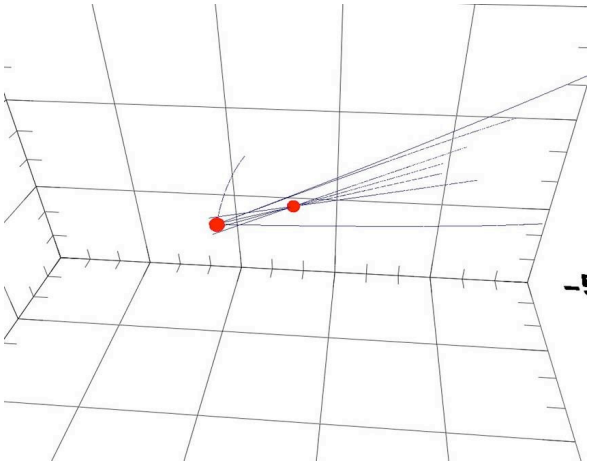
1. Optimise detector design
   - Need reliable tracking
   - Been using Fortran/SGV
2. Develop vertex tools
   - Work within common framework
   - Writing C++ package
3. Physics analysis

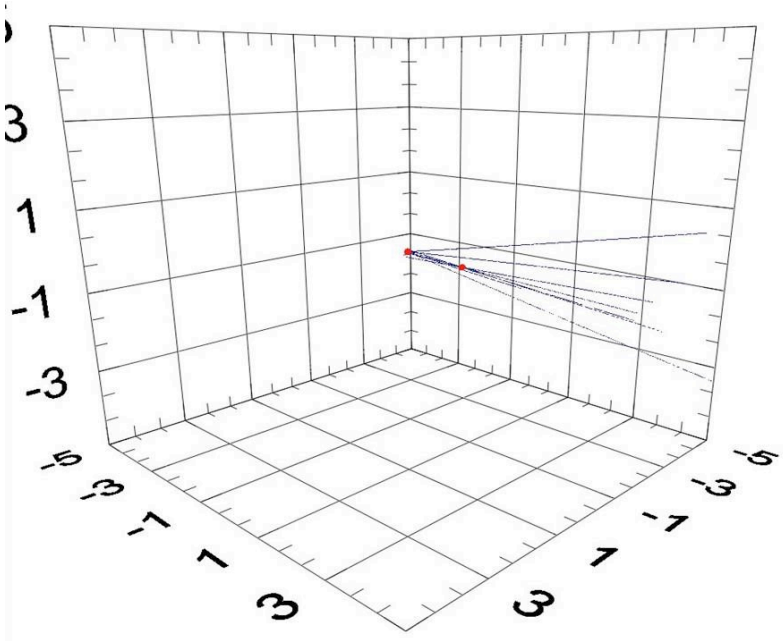


ZVTOP



- **Topological vertex finder**
  - **Developed at SLD**
  - **Being ported to C++** ***(JAVA at SLAC)***
- **Used as basis for flavour tag**



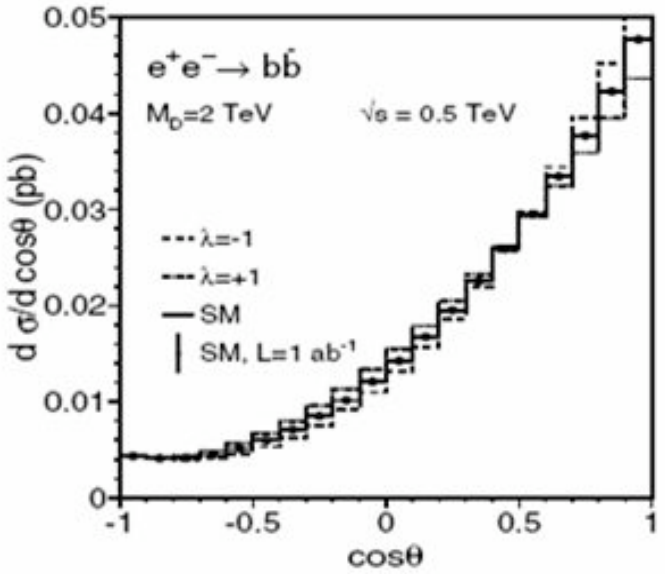


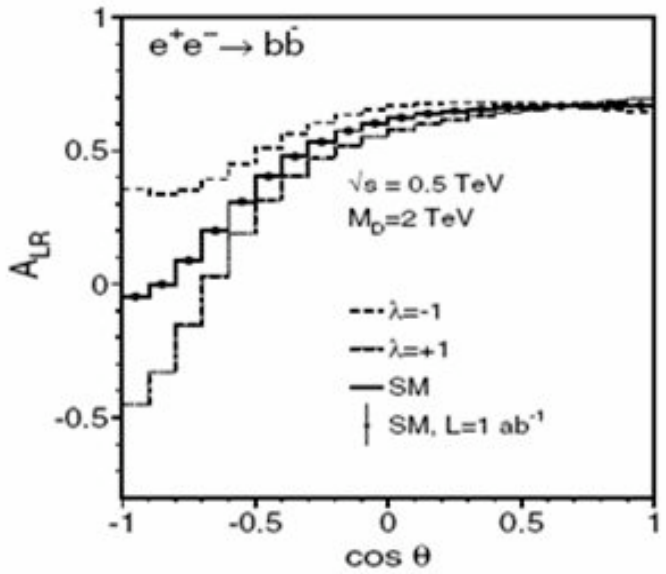
Vertex Charge

Do more than identify *b*, *c* quarks…

1. **Find vertices with ZVTOP**
2. **Attach candidate tracks**
3. **Measure charge**

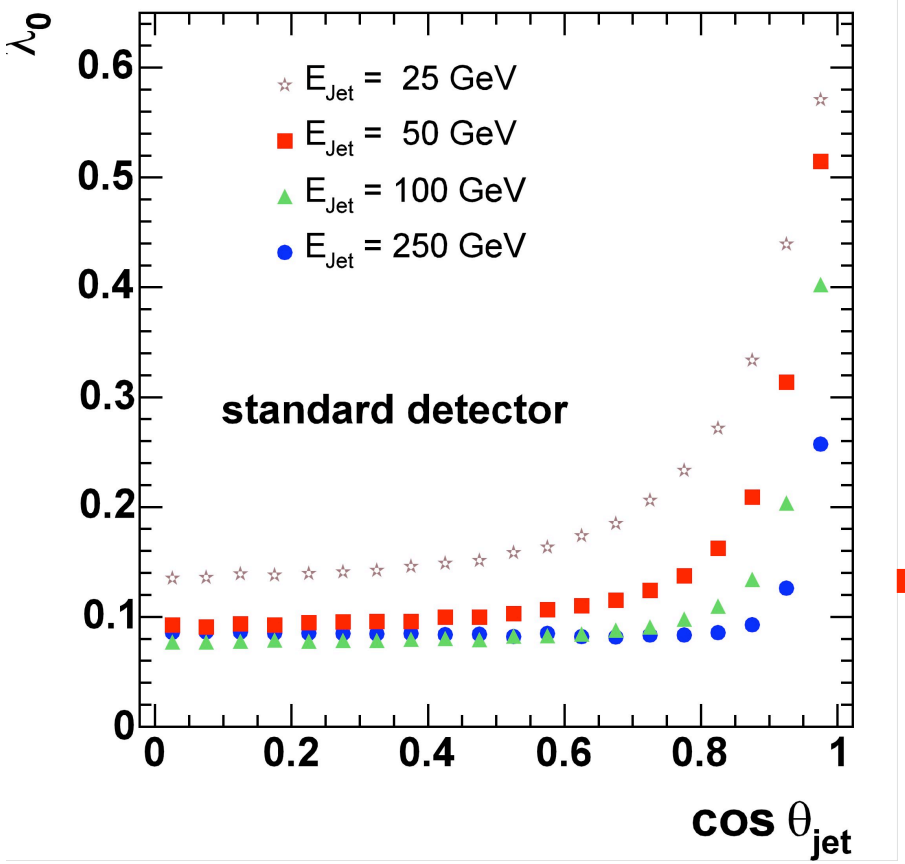
Can tell quark from antiquark!





e.g. LED scenarios

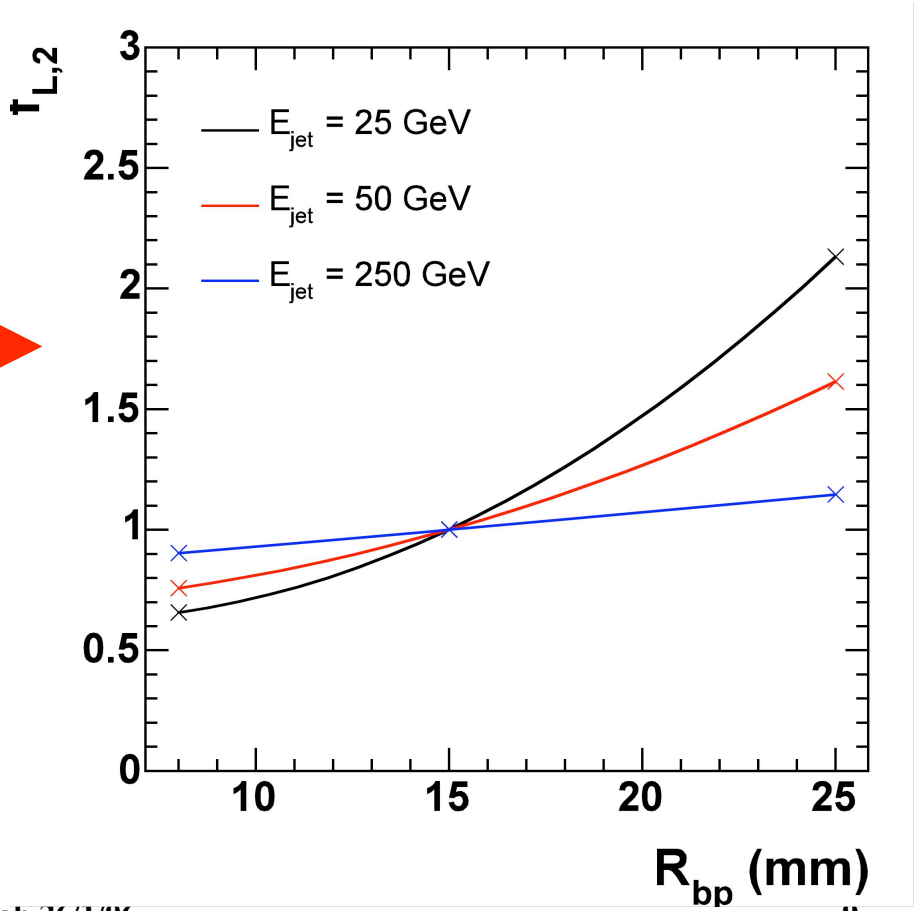
Vertex Charge in Physics



Neutral *B* Leakage Rates

Luminosity factor for two jets

- Quantify effect of beam pipe radius



LCFI Mechanical Studies

1. Thin Ladder Mechanics

- Materials and designs for $\Delta T \approx 100K$
- Preference for uniform material in tracking volume
- *CCDs routinely thinned to epitaxial layer*

2. Global Design

- Ensure ladder designs practical

3. Cooling

- Gas cooling has always been assumed…

Mechanical Options

Target of 0.1% X_0 per layer

(100μm silicon equivalent)

1. Unsupported Silicon

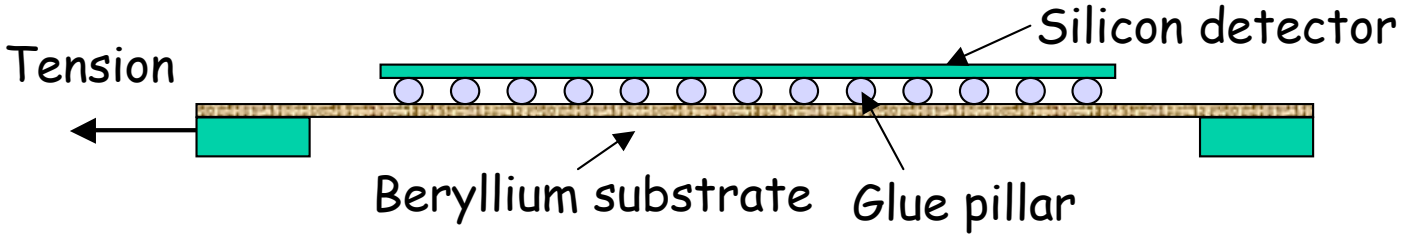
- Longitudinal tensioning provides stiffness
- No lateral stability
- Not believed to be promising

2. Thin Substrates

- Detector thinned to epitaxial layer (20μm)
- Silicon glued to low mass substrate for lateral stability
- Longitudinal stiffness still from tension
- Beryllium has best specific stiffness

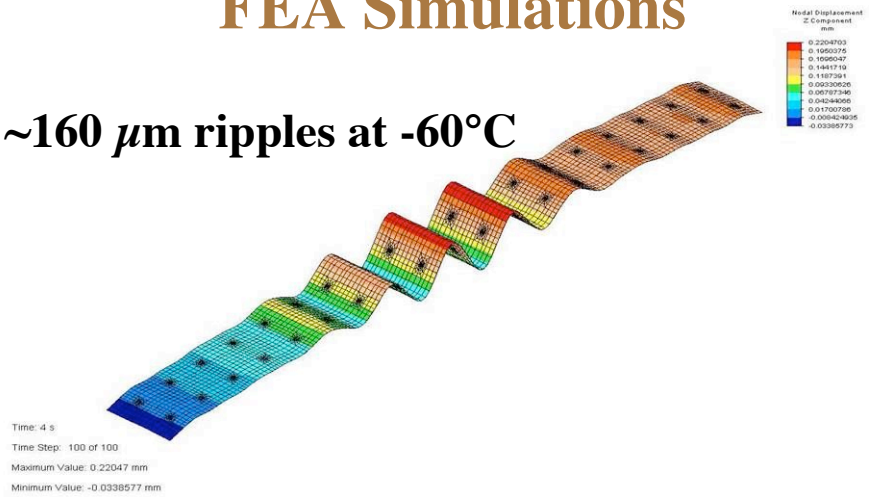
3. Rigid Structures

Mechanical Studies of Be-Si

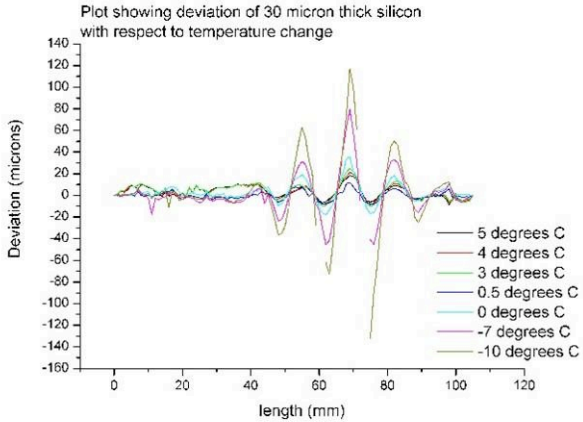


FEA Simulations

~160 μm ripples at -60°C



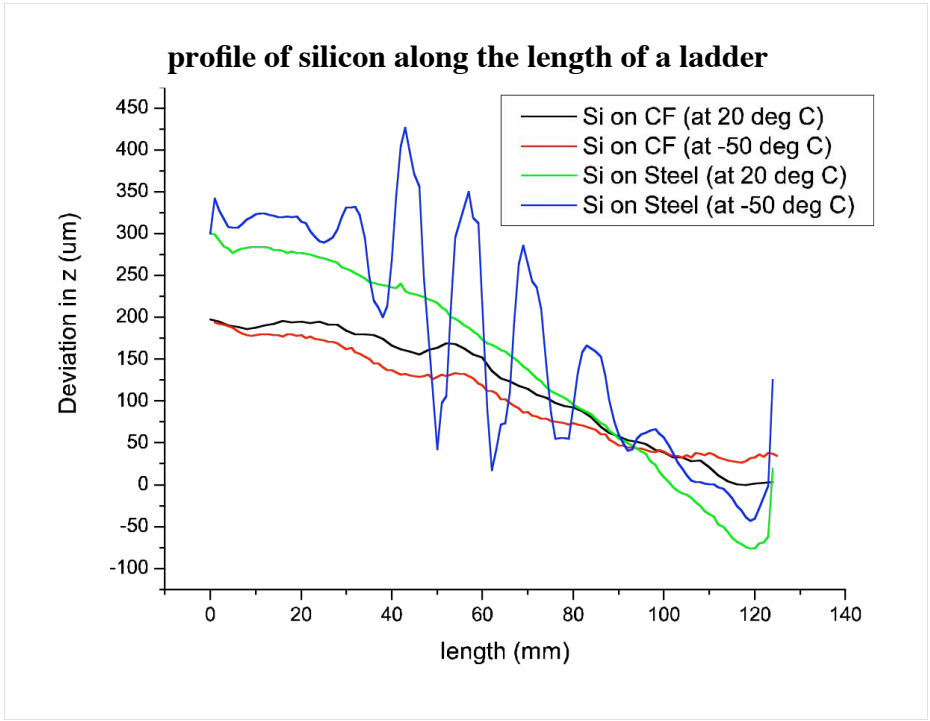
Physical Prototyping



- **Good qualitative agreement**
- **Minimum thickness ~ 0.15% X_0**

Carbon Fibre Substrates

- Carbon fibre has better CTE match than beryllium

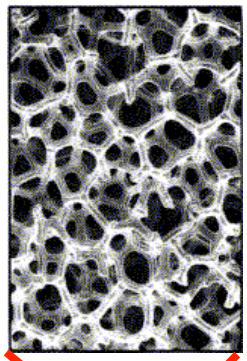


- Prototype ~ 0.09% X_0
  - No rippling down to < 200K
  - Lateral stability insufficient

- Other thin substrates under consideration

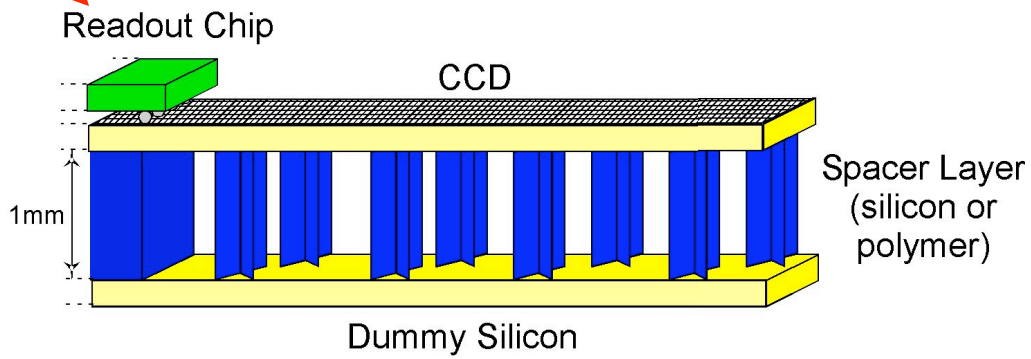
Rigid Structures

Foam: substrate or sandwich core



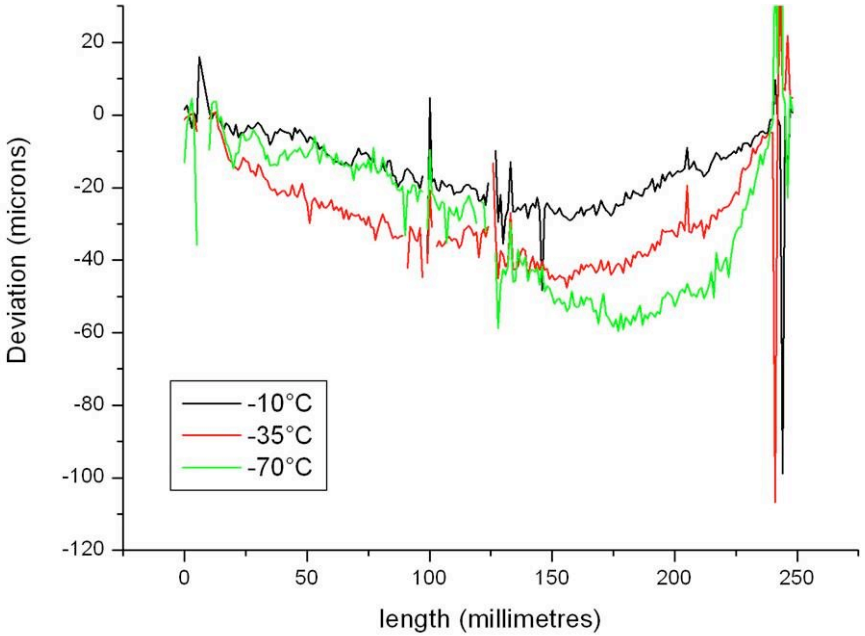
- **Macroscopically uniform**
- **No tensioning needed**

Other approaches exist

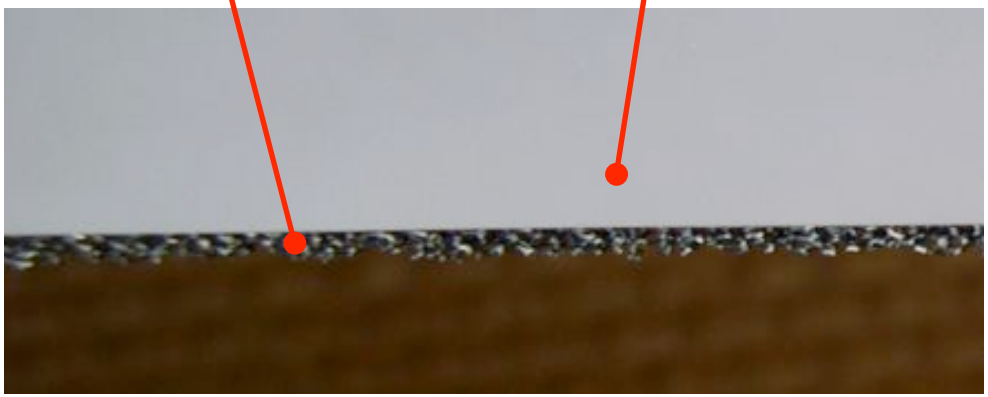


Foam Prototypes

- 8% Silicon Carbide
  - Single-sided
  - 0.14% X0
  - 3-4% believed possible



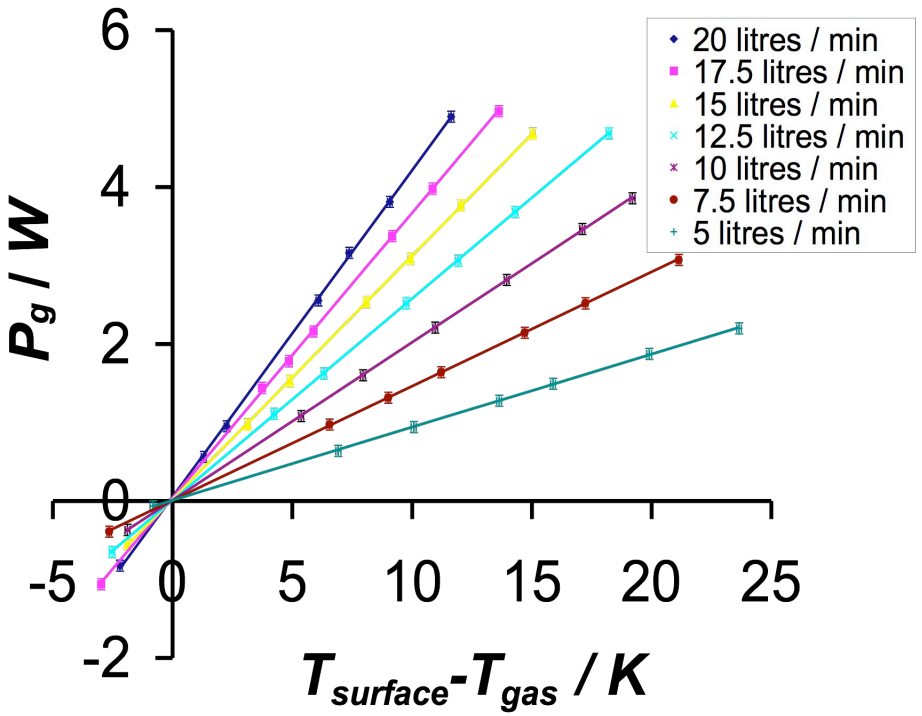
1.5 mm SiC 20 μm silicon

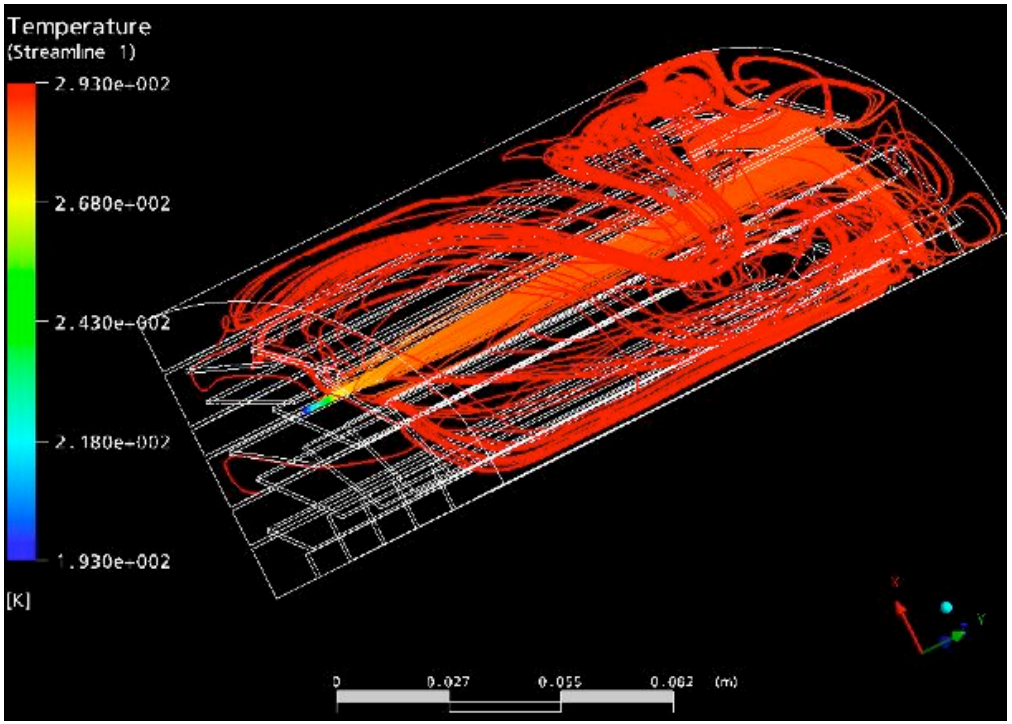


- 3% RVC
  - Sandwich
  - 0.09% X_0

Cooling Studies

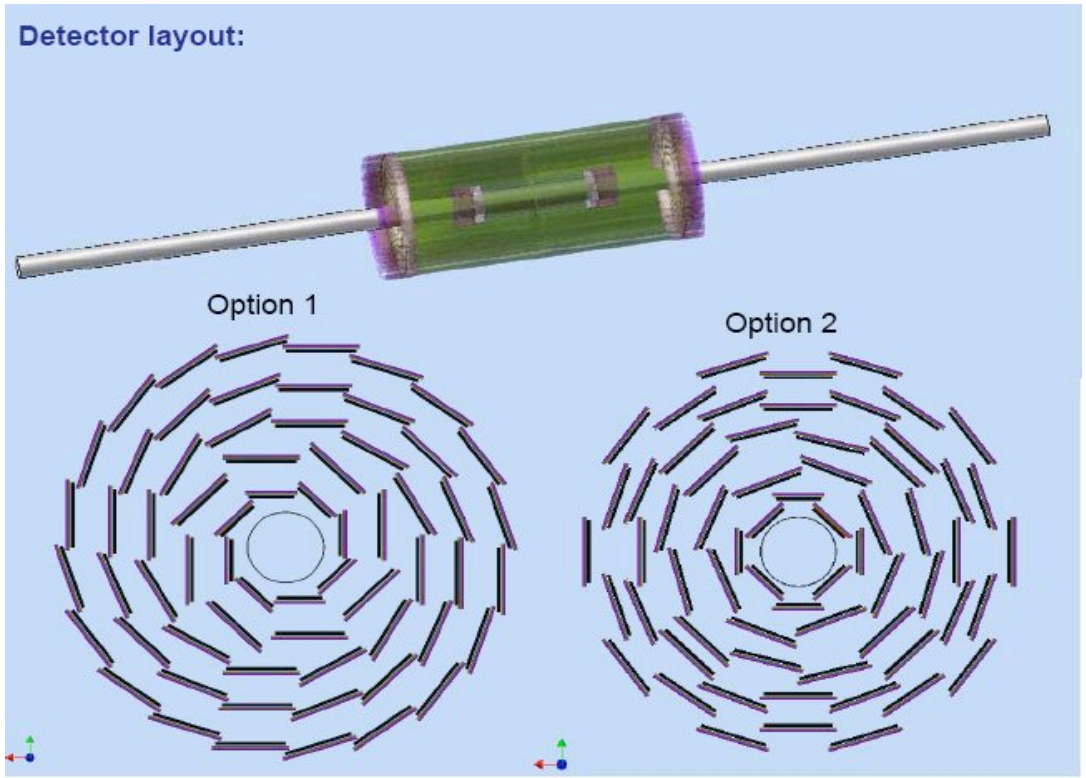
- **Gas cooling test stand**
  - **Cold nitrogen flow**
  - **Model of 1/4 detector**

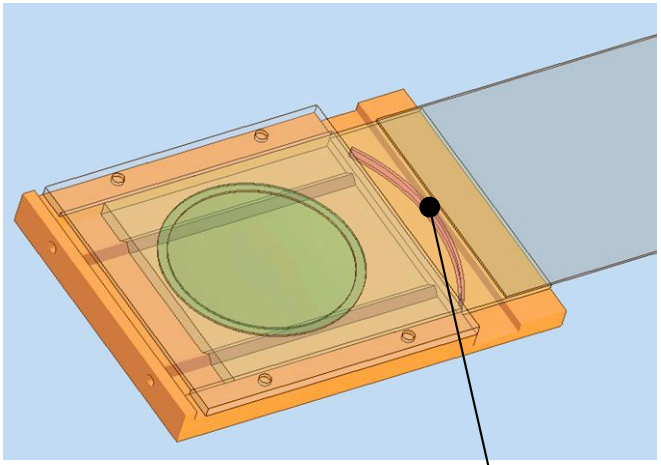




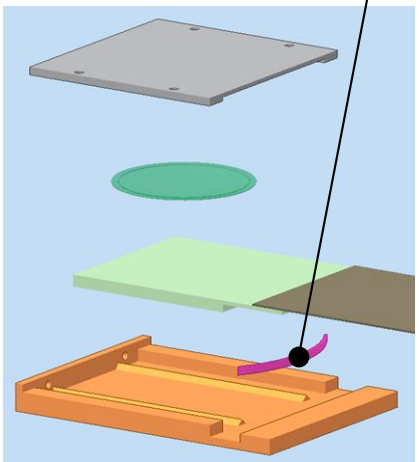
- **Parallel CFD simulation work**

Global Design Work





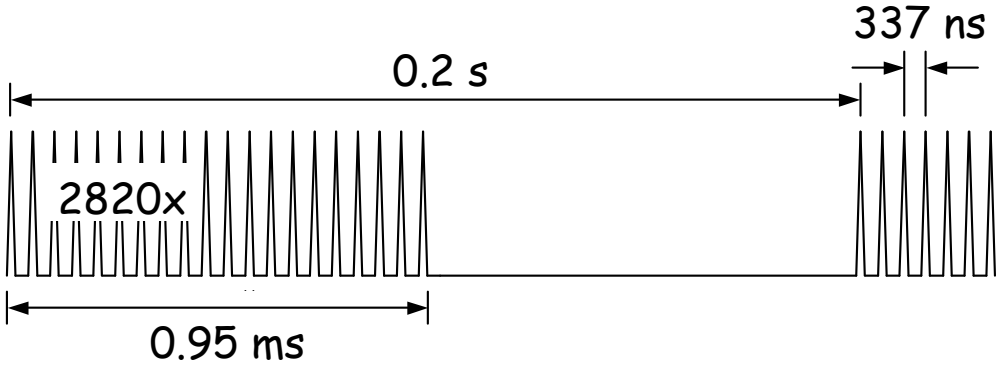
Ladder end with leaf spring



- **Enough detail for ladder design "sanity check"**

Sensors: The Challenge

Beam Time Structure:



What readout speed is needed?

- **Inner layer 1.6 MPixel sensors**
- **Once per bunch = 300ns per frame : *too fast***
- **Once per train ~200 hits/mm^2 : *too slow***
- **10 hits/mm^2 => 50μs per frame: just right**

(Fastest commercial imaging ~ 1 ms/MPixel)

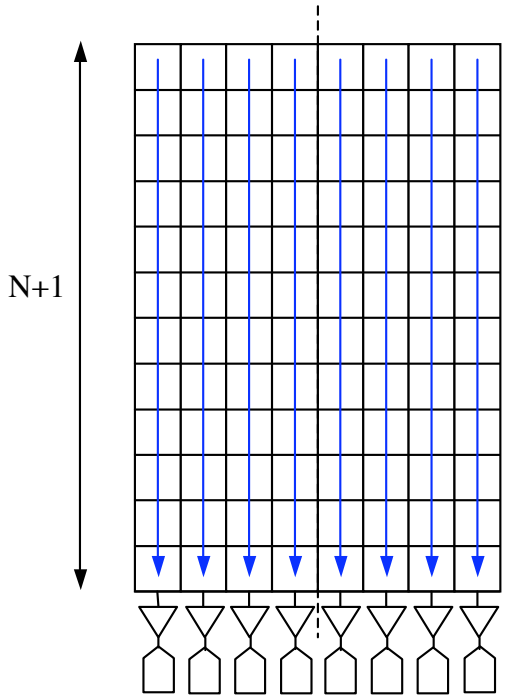
Power dissipation – gas volume cooling

Sensor Research

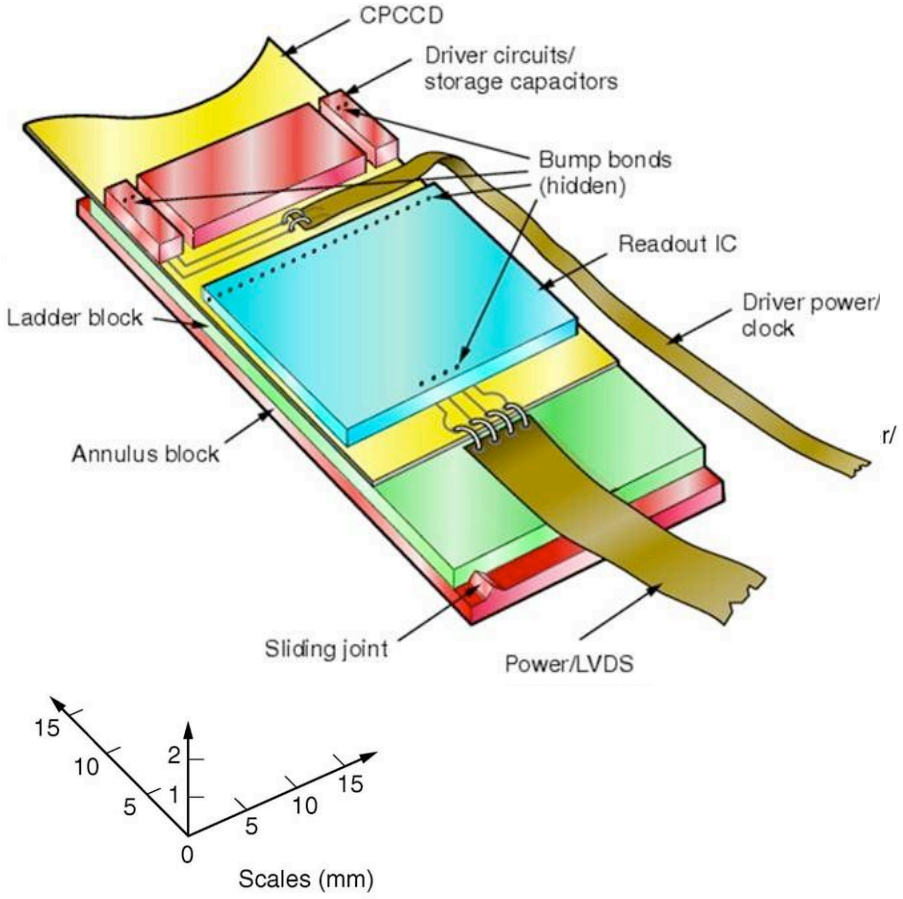
1. **Column Parallel CCDs**
   - Focus so far - building on past experience
   - Readout during bunch train
   - Clock drive major challenge
2. **Image Sensor with In-situ Storage**
   - Increased robustness
   - Reduced driver requirements

Column Parallel CCD

- **Separate amplifier and readout for each column**
- **50 MHz clock rate**

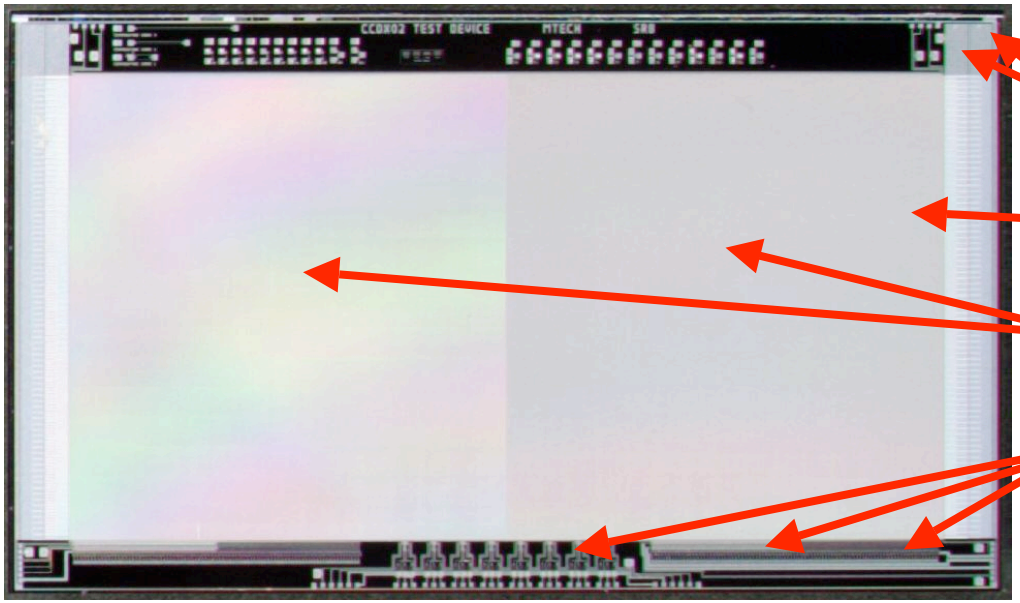


Column Parallel CCD
Readout time = $(N+1)/F_{out}$



- **Clock drive is real challenge**

Prototype CP CCD



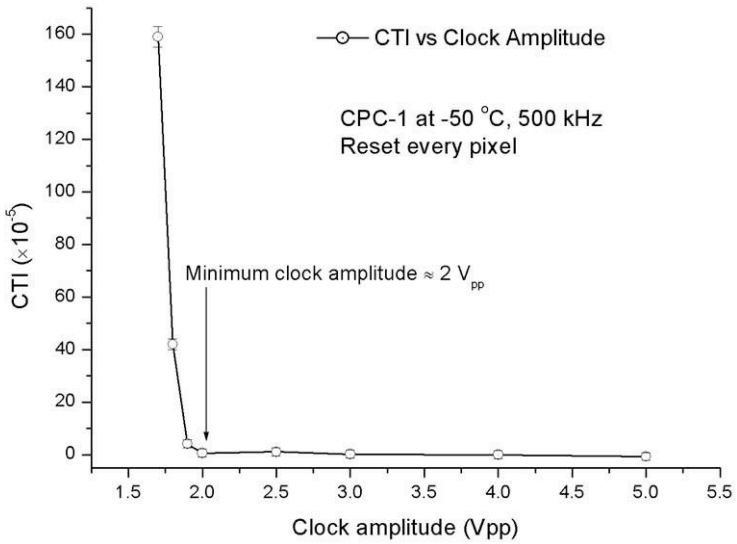
CPC-1 produced by e2v

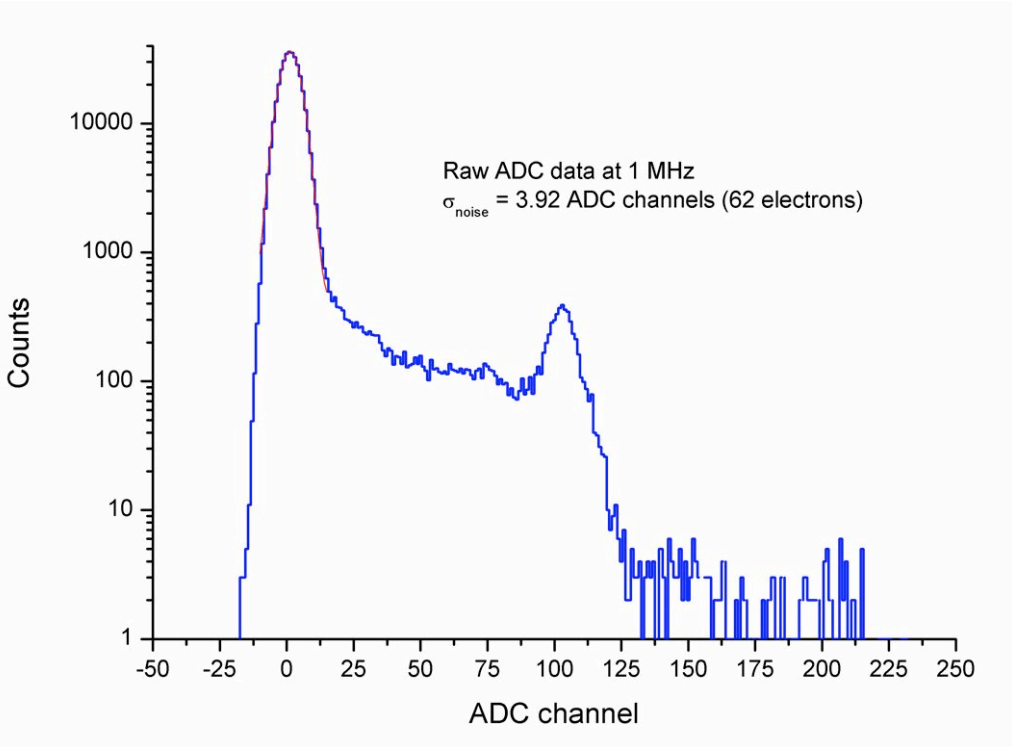
- Two phase operation
- Metal strapping for clock
- 2 different gate shapes
- 3 different types of output
- 2 different implant levels

➢*Clock with highest frequency at lowest voltage*

CPC-1 Results

- **Noise ~ 100 electrons (60 after filter)**
- **Minimum clock ~1.9 V**



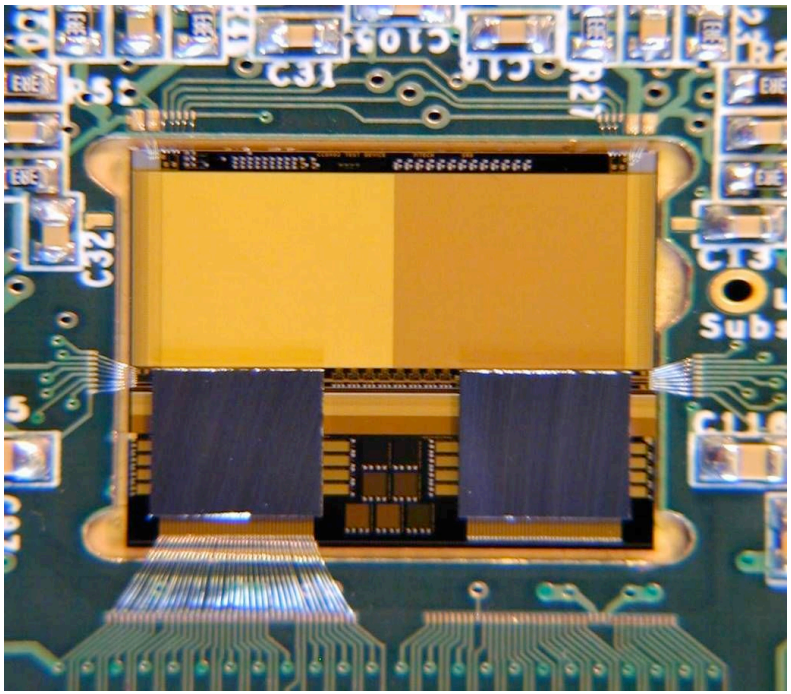


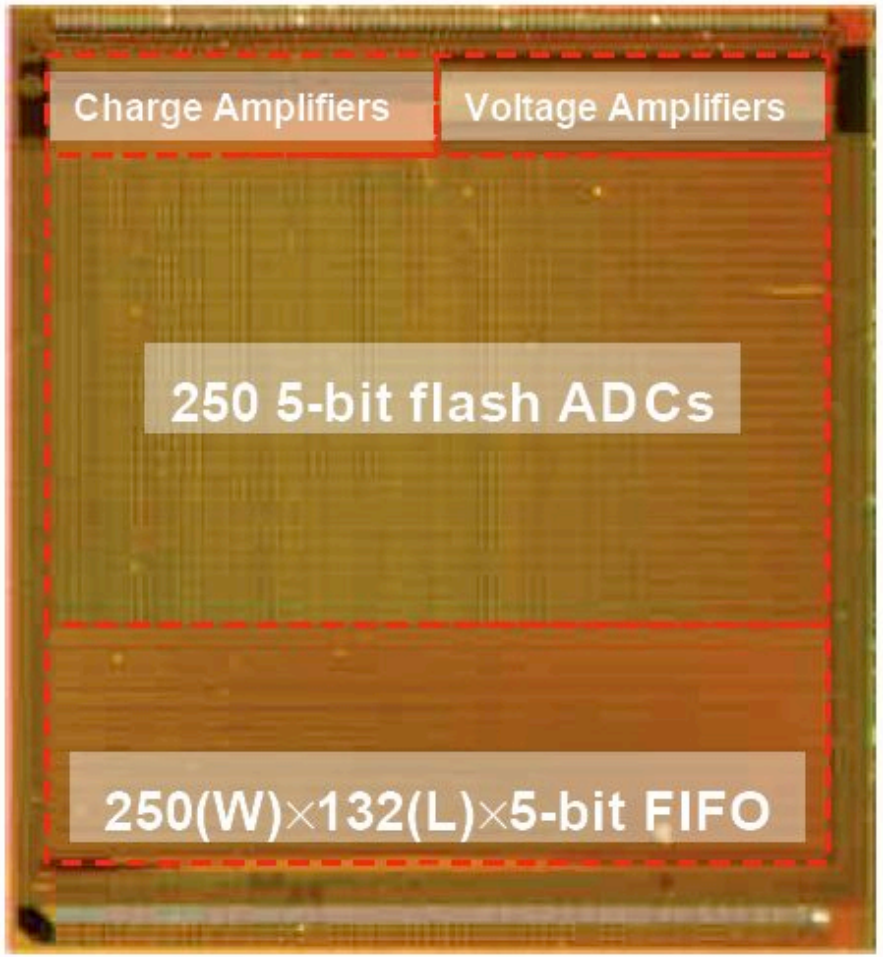
- **Maximum frequency > 25 MHz**
  - **inherent clock asymmetry**

CP Readout ASIC

CPR-1 designed in house

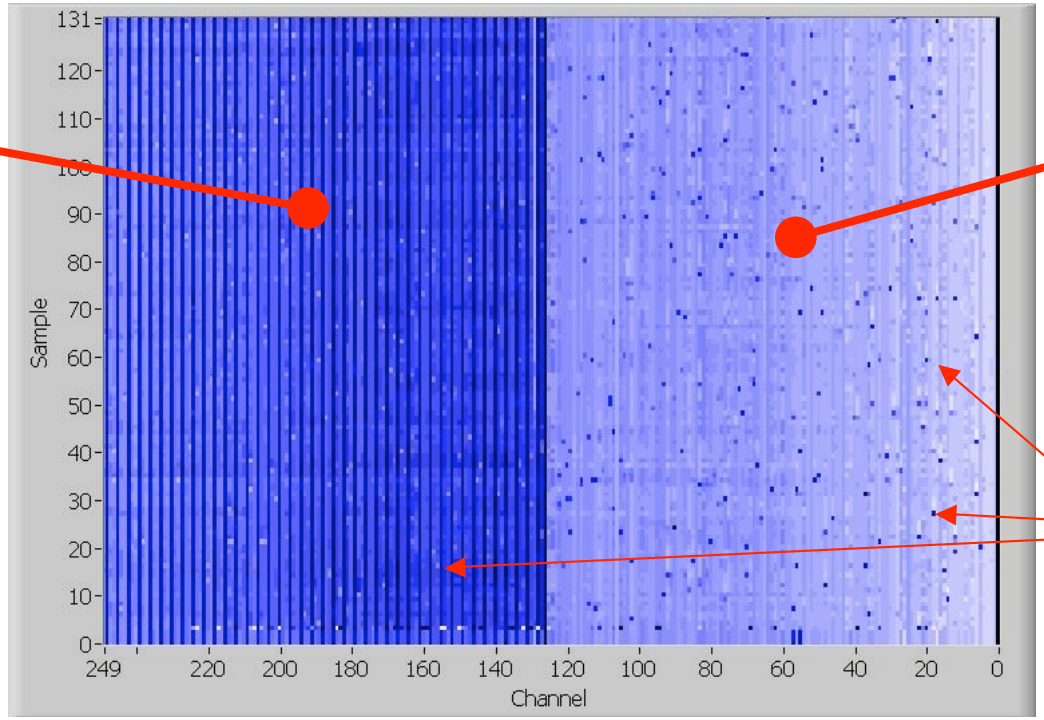
- IBM 0.25 μm process
- Bump bonded to CPC





Testing Results

Charge Amplifiers
(inverting)



Voltage Amplifiers
(non-inverting)

6 keV X-rays

- Charge amplifiers work
- Negligible noise from CPR
- *Column parallel operation demonstrated*

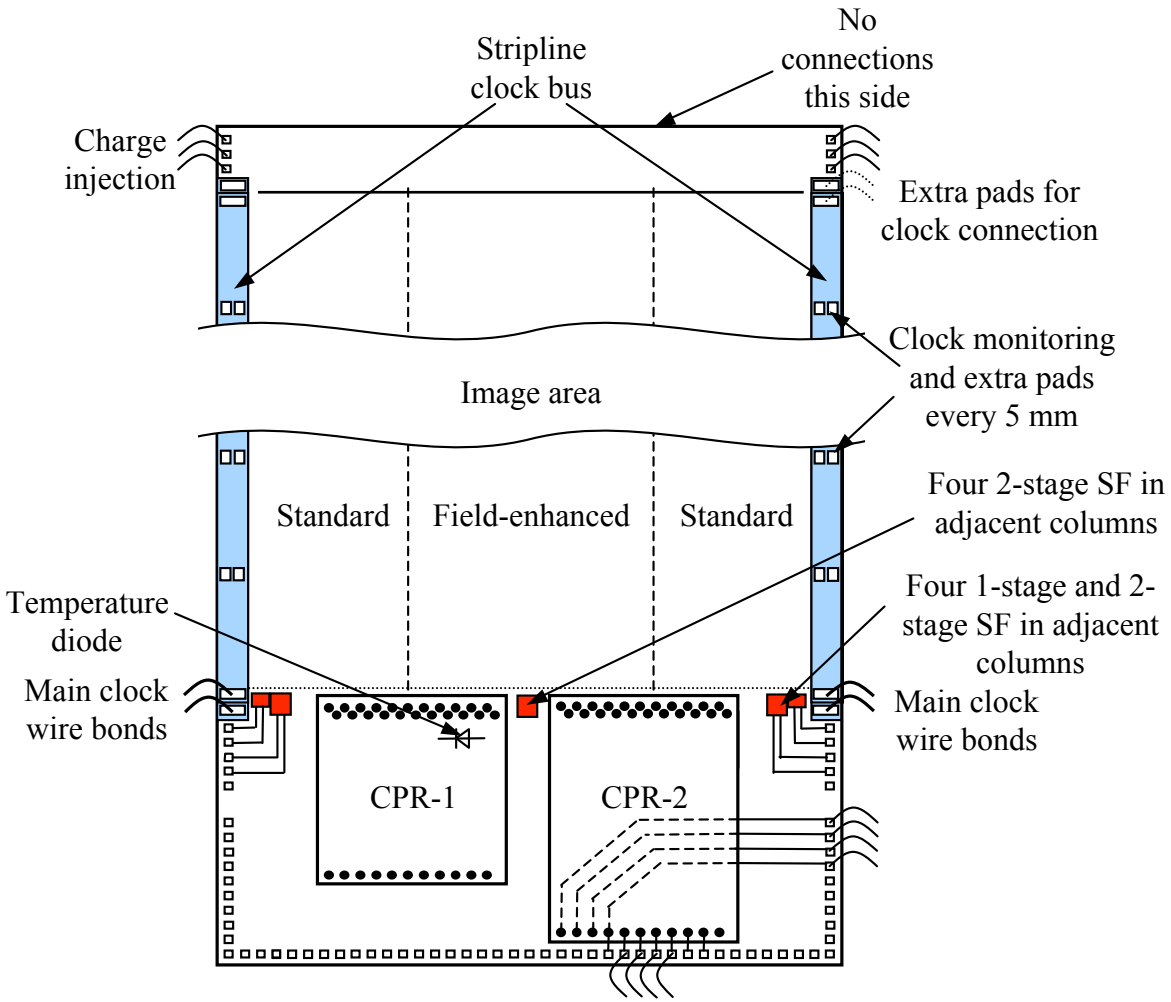
- No signal in ~20% of voltage channels
- Readout chip very sensitive to timing and bias issues
- Gain decrease towards centre of chip

The Second Generation

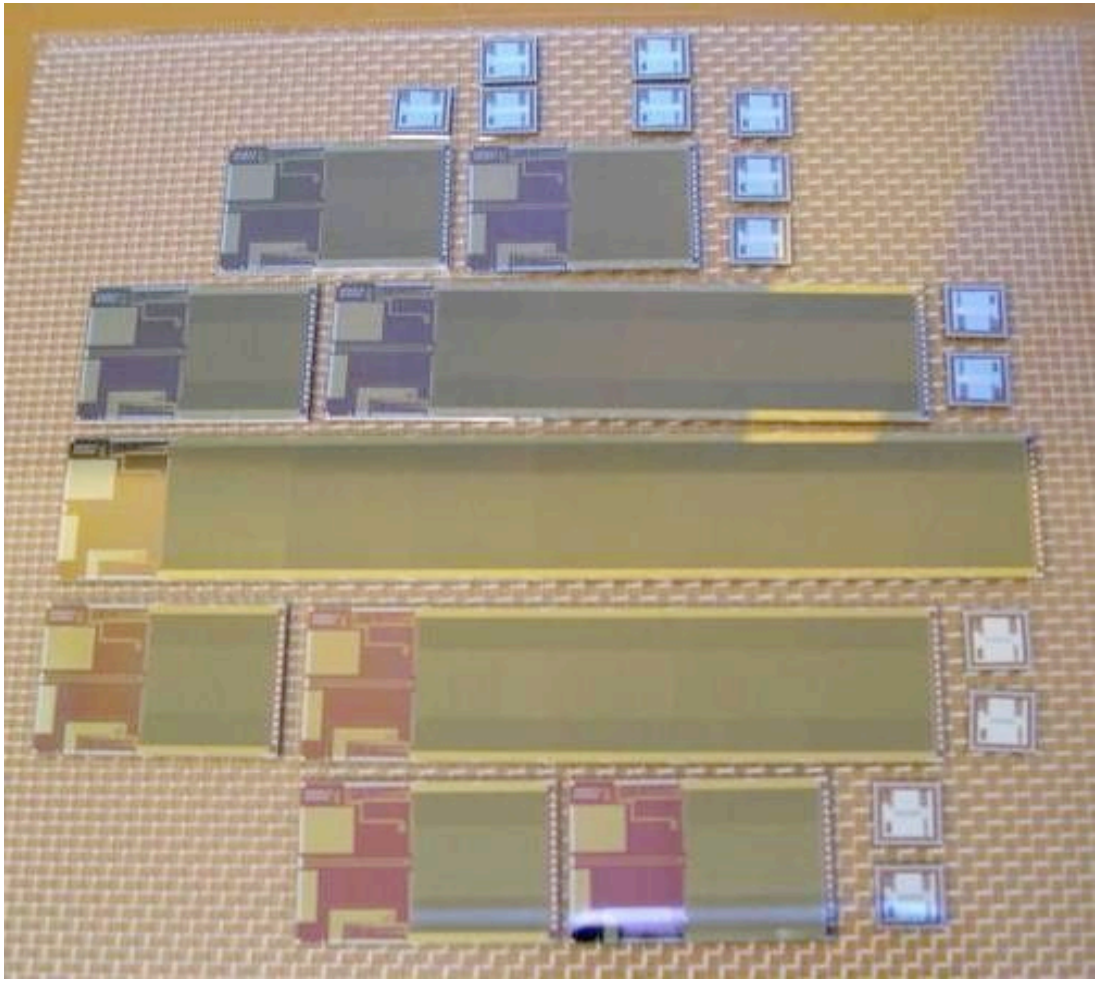
- **CCDs**
  - **Larger and faster prototypes**
  - **Clock drivers**
  - **Radiation effects**
- **ASICs**
  - **More robust**
  - **Cluster finding logic**
- **Hostile RF environment:**
  - **Large EM leakage from ILC bunch train**
  - **Charge-voltage conversion dangerous**
  - ***Store multiple charge samples locally***
  - ***Readout all samples during 200ms dead time***

New CPC

- **Double metal now available from e2v**
- **Symmetric clock design**
- **"Busline-free" option**
  - **Distributed clock planes**
  - **Faster**
  - **More uniform**
- **Compatible with old and new readout chips**

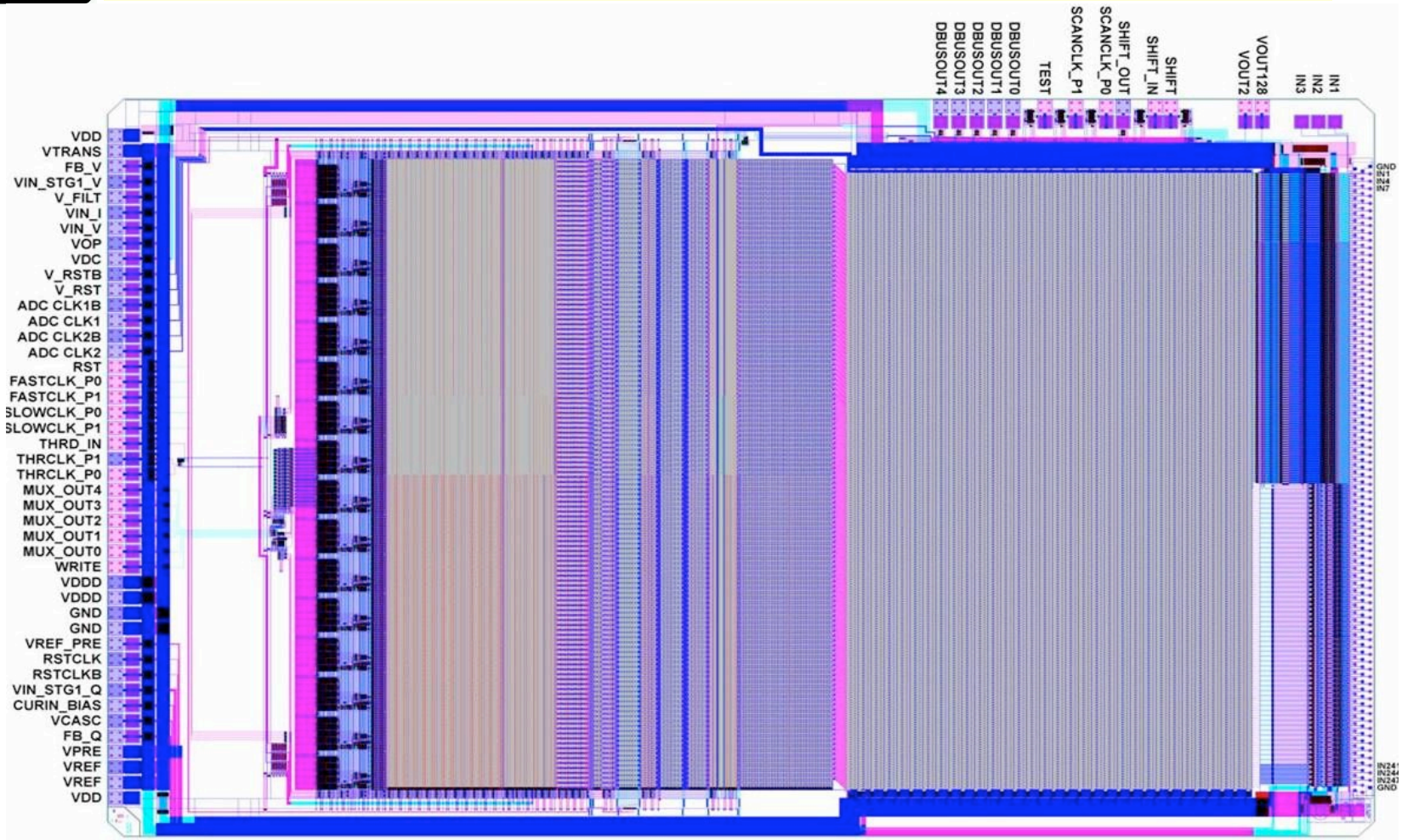


CPC-2 Production



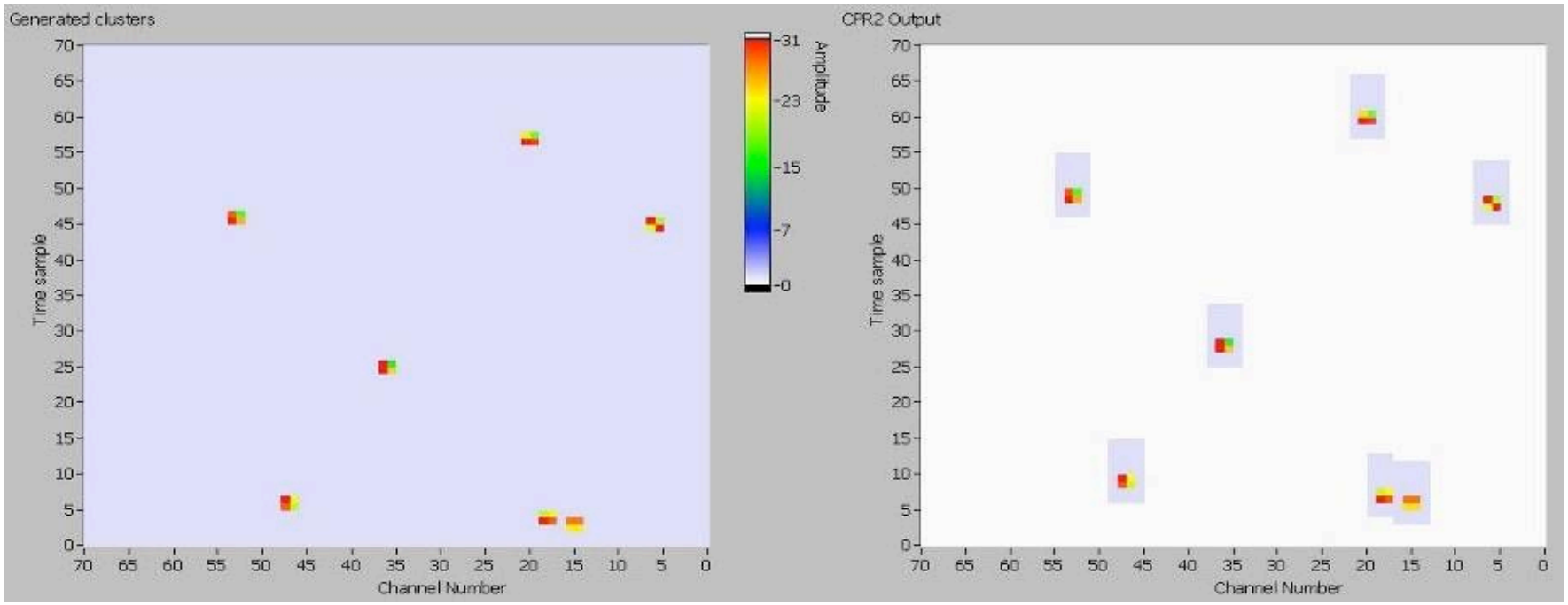
- **Dedicated batch at e2v**
- **3 sizes of CPCCD**
  - *up to 92 mm active length*
- **First devices delivered**
- **Wafers include 16×16 ISIS**

New Readout Chip



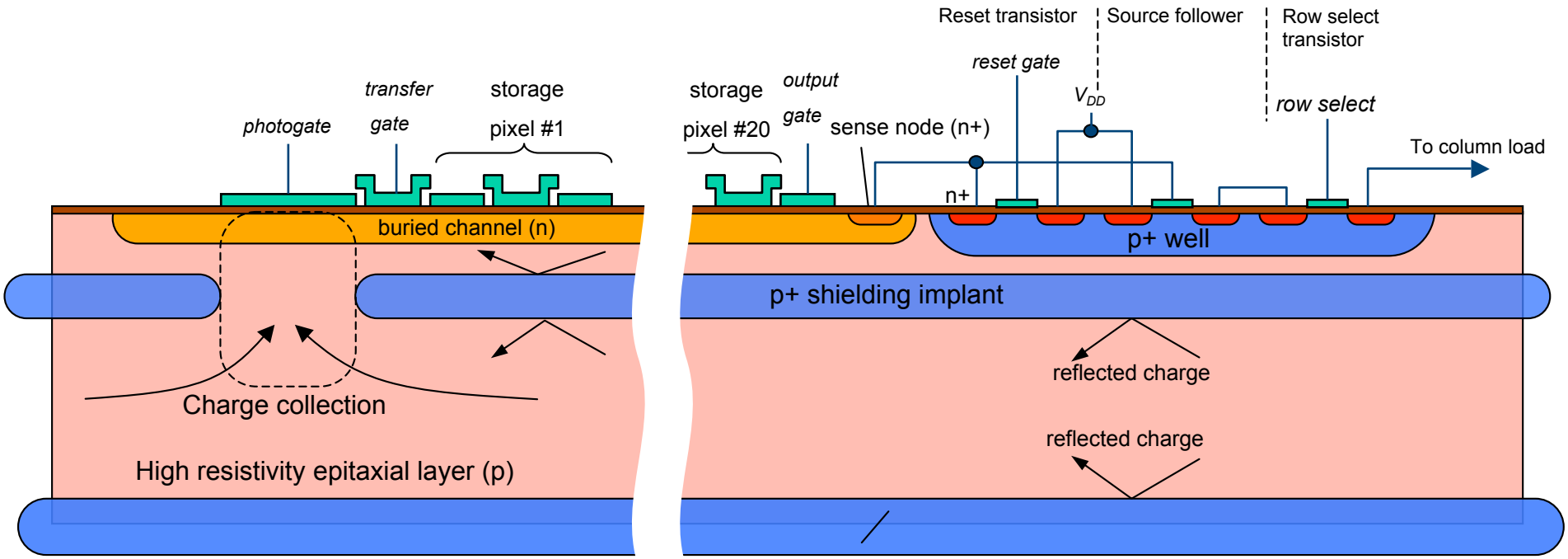
Output | **Sparsification & Multiplexing** | **Cluster Finding** | **Binary Conversion** | **5-bit ADC** | **Preamp Input**

CPR-2 Testing



- **Cluster finding logic and sparse readout**
- **Improved amplifiers and ADCs**
- **Increased robustness**

ISIS Concept



- **Orders of magnitude increased resistance to RF**
- **Much reduced clocking requirements *(readout ~1MHz)***
- **Combination of CCD and CMOS technology on small pitch**

Ideal burst imager - is it practical for the ILC?

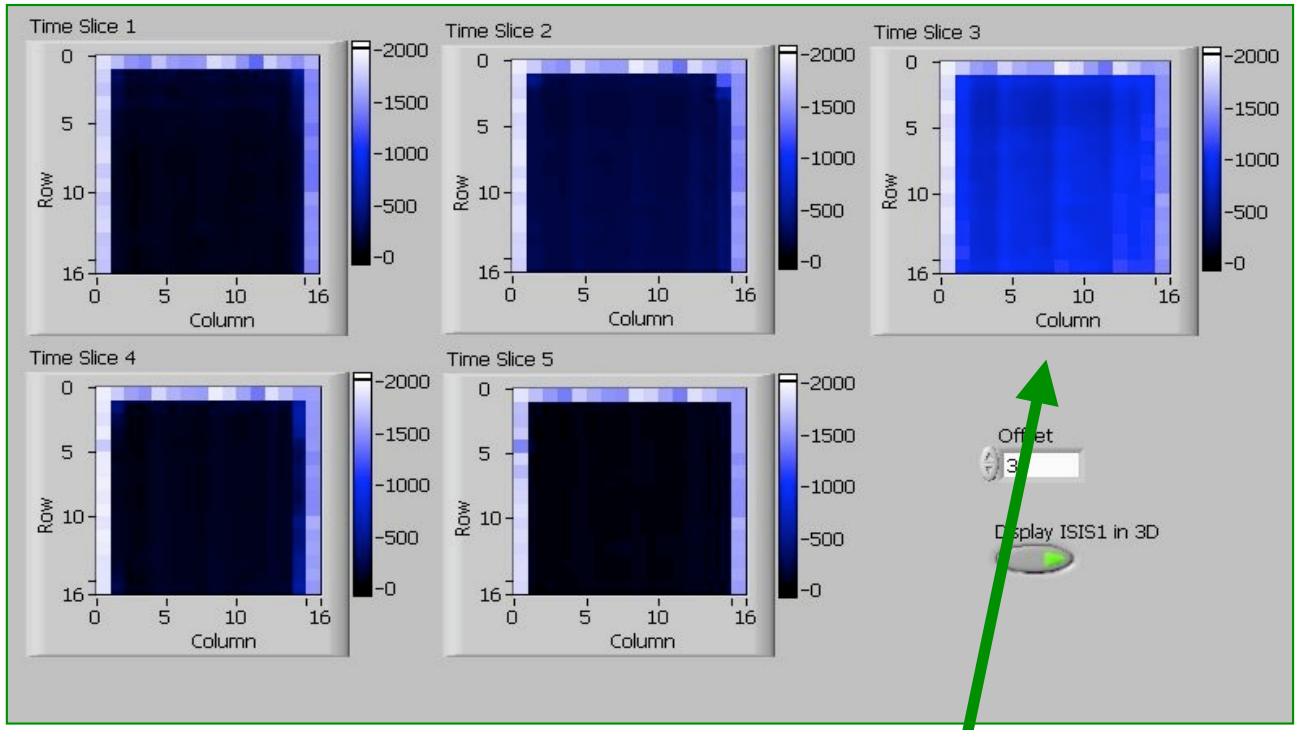
ISIS-1

Photogate 8×8μm²

5 cell CCD Register

Output and reset transistors

- **Proof-of-principle**
  - 16×16 array
  - e2v design rules



LED flash in 3rd cell

Summary

- First generation sensors extensively studied
  - Column parallel CCD principle proven
  - Direct charge output demonstrated
- Starting to text next generation
  - Detector-scale CCDs, sparsification
  - ISIS principle proved
- 0.1% X_0 ladders seem achievable
  - Foams looking promising
- Qualitative detector optimisation
  - Delivering tools to global ILC community

Exciting times ahead!