VME Products

CAEN *Short Form Catalog 2010*

More modules are available in VME64X standard
(see Ordering Information)

The VERSAmodule Eurocard bus is one of the trademarks of CAEN instrumentation catalog.
Widely used both in the industry and in the research communities it offer the combination of several qualities such as reliability, robustness and flexibility.
CAEN VME products are widely used both in test and measurements applications and in small and big data acquisition installations.
In the following pages you will find the huge selection of functions that the CAEN modules offer.

Function	Model	Description	Page	
ADC (Peak Sensing)	**V1785**	*8 Ch Dual Range Multievent Peak Sensing ADC*	49	
ADC (Peak Sensing)	**V785**	*32 Channel Multievent Peak Sensing ADC*	49	
ADC (Peak Sensing)	**V785N**	*16 Channel Multievent Peak Sensing ADC*	49	
ADC (Sampling)	**V1729A**	*4 Channel 14 bit 2 GS/s (300 MHz bandwidth) Switched-Capacitor Digitizer*	50	New
Sequencer	**V551B**	*Sequencer for V550 - V550A C-RAMS*	50	
ADC (C-RAMS)	**V550**	*CAEN Readout for Analog Multiplexed Signals (10 bit)*	50	
ADC (C-RAMS)	**V550A**	*CAEN Readout for Analog Multiplexed Signals (12 bit)*	50	
Amplifier (Fast)	**V974**	*4 Channel Variable Gain Fast Amplifier*	51	
Amplifier (Fast)	**V975**	*8 Channel Fast Amplifier*	51	
Attenuator	**V859**	*Dual Attenuator*	51	
Coinc./Logic/Trig. Unit	**V1495**	*General Purpose VME Board*	52	
Scaler	**FW1495SC**	*128 Ch 270 MHz Multievent latching Scaler Firmware*	53	New
Coinc./Logic/Trig. Unit	**V976**	*Quad 4 Fold AND/OR/MAJ, NIM-TTL TTL-NIM Translator, Fan-In Fan-Out*	54	
Controller	**V1718**	*VME-USB2.0 Bridge*	54	
Controller	**V2718**	*VME-PCI Optical Link Bridge*	55	
Discriminator	**V812**	*16 Channel Constant Fraction Discriminator*	55	
Discriminator	**V814**	*16 Channel Low Threshold Discriminator*	56	
Discriminator	**V895**	*16 Channel Leading Edge Discriminator*	56	
Fan In - Fan Out Unit	**V925**	*Quad Linear Fan-In Fan-Out*	57	
I/O Register	**V259**	*16 Bit Strobed Multihit Pattern Unit*	57	
I/O Register	**V977**	*16 Channel Input/Output Register (Status A)*	58	
QDC	**V792**	*32 Channel Multievent QDC*	58	
QDC	**V792N**	*16 Channel Multievent QDC*	58	
QDC	**V862**	*32 Channel Multievent Individual Gate QDC*	59	
QDC	**V965**	*16 Channel Dual Range Multievent QDC*	59	
QDC	**V965A**	*8 Channel Dual Range Multievent QDC*	59	
Scaler	**V560**	*16 Channel Scaler*	60	
Scaler	**V830**	*32 Channel Latching Scaler*	60	
TDC	**V1190A**	*128 Channel Multihit TDC*	61	
TDC	**V1190B**	*64 Channel Multihit TDC*	61	
TDC	**V1290A**	*32 Channel Multihit TDC*	61	
TDC	**V1290N**	*16 Channel Multihit TDC*	61	
TDC	**V775**	*32 Channel Multievent TDC*	62	
TDC	**V775N**	*16 Channel Multievent TDC*	62	
Timing Unit	**V972**	*Delay Unit*	62	
Timing Unit	**V993B**	*Dual Timer*	63	
Translator	**V538A**	*8 Channel NIM-ECL/ECL-NIM Translator*	63	

V1785 8 Ch Dual Range Multievent Peak Sensing ADC

T8

The Mod. V1785 is a 1-unit wide VME 6U module housing 8 Peak Sensing Analog-to-Digital Conversion channels. Each channel is able to detect and convert the peak value of the positive analog signals (with >50 ns risetime) fed to the relevant connectors. Input voltage range is 0 ÷ 4 V. Each channel is processed by two gain stage (x1 and x8) in parallel followed by the ADC stage: a dual input range is then featured: 0 ÷ 4 V (1 mV LSB) and 0 ÷ 500 mV (125 µV LSB); this allows to avoid saturation with big input signals while increasing resolution with small ones.

The only Dual Range Multievent Peak Sensing ADC.
Avoid saturation with big input signals and increase resolution with small ones!

The ADCs use a sliding scale technique in order to reduce the differential non-linearity.
Programmable zero suppression, multievent buffer memory, trigger counter and test features complete the flexibility of the unit.
The module works in A24/A32 mode. The data transfer occurs in D16, D32, BLT32 or MBLT64 mode. The unit supports also the Chained Block Transfer (CBLT32/CBLT64) and the Multicast commands.
The VME interface is VME64 and VME64X standard compliant and features the A24/A32 and MultiCast addressing modes. The data readout occurs either in D32, BLT32, MBLT64 mode, or in daisy chain with 32/64 bit Chained Block Transfers. The module features a fully programmable RORA interrupter.
The board is provided with the P1 and P2 VME connectors and fits into both V430 and standard 6U crates. It also supports the "live insertion", allowing the User to insert (or remove) the board into (or from) the crate without switching it off.

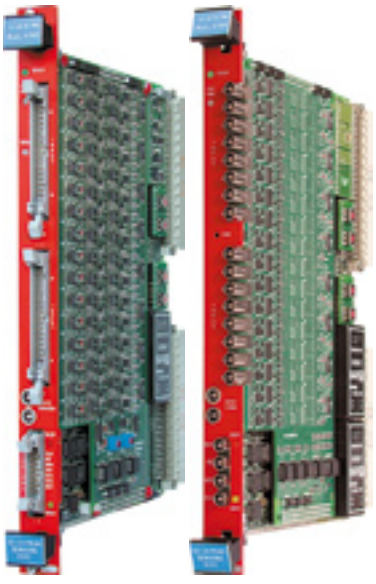
- **Two simultaneous ranges: 0 ÷ 4 V / 0 ÷ 500 mV**
- **12 bit resolution with 15 bit dynamics**
- **125 µV LSB on low range, 1mV LSB on high range**
- **2.8 µs / 8 ch conversion time**
- **600 ns fast clear time**
- **Zero and overflow suppression for each channel**
- **±0.1 % Integral non linearity**
- **±1.5 % Differential non linearity**
- **32 event buffer memory**
- **BLT32/MBLT64/CBLT32/CBLT64 data transfer**
- **Multicast commands**
- **Live insertion**

Ordering Information

Code	Description
WV1785XNCAAA	V1785NC - 8 Ch. Dual Range Multievent Peak Sensing ADC

V785 - V785N 32 / 16 Channel Multievent Peak Sensing ADC

T8



The Mod. V785 is a 1-unit wide VME 6U module housing 32 Peak Sensing Analog-to-Digital Conversion channels. Each channel is able to detect and convert the peak value of the positive analog signals (with >50 ns risetime) fed to the relevant connectors. Input voltage range is 0 ÷ 4 V. The Model V785N houses 16 channels on LEMO 00 connectors and shares most of the other features with the Mod. V785.
The outputs of the PEAK sections are multiplexed and subsequently converted by two fast 12-bit ADCs (V785: 5.7 µs for all channels, V785N: 2.8 µs for all channels). The integral non linearity is ±0.1% of full scale range (FSR), measured from 2% to 97% of FSR; the differential non linearity is ±1.5% of FSR, measured from 3% to 100% of FSR. The ADCs use a sliding scale technique to reduce the differential non-linearity.
Programmable zero suppression, multievent buffer memory, trigger counter and test features complete the flexibility of the unit.
The module works in A24/A32 mode. The data transfer occurs in D16, D32, BLT32 or MBLT64 mode. The unit supports also the Chained Block Transfer (CBLT32/CBLT64) and the Multicast commands.
A 16 ch. flat cable to LEMO input adapter (Mod. A385, see *Accessories* section) is available for the Mod. V785 (one 32 ch. V785 requires two A385 adapters).
The boards support the live insertion that allows inserting or removing them into the crate without switching it off.

- **0 ÷ 4 V input range**
- **Full 12 bit resolution**
- **5.7 µs / 32 ch and 2.8 µs / 16 ch conversion times**
- **600 ns fast clear time**
- **Zero and overflow suppression for each channel**
- **±0.1% integral non linearity**
- **±1.5% differential non linearity**
- **32 event buffer memory**
- **BLT32/MBLT64/CBLT32/CBLT64 data transfer**
- **Multicast commands**
- **Live insertion**

Ordering Information

Code	Description
WV785XACAAAA	V785AC - 32 Channel Peak Sensing ADC (4V, No 12V DCDC, live ins)
WV785XAGAAAA	V785AG - 32 Channel Peak Sensing ADC (8V, No 12V DCDC, live ins)
WV785XNCAAAA	V785NC - 16 Channel Peak Sensing ADC (4V, No 12V DCDC, live ins)
WA385XAAAAAA	A385 - 16 Channel Cable Adapter (Flat to LEMO) for V785, 50cm ±10% cables

V1729A 4 Channel 14 bit 2 GS/s (300 MHz bandwidth) Switched-Capacitor Digitizer

T10

NEW

The V1729A is a 1-unit wide VME 6U board based on the MATACQ (analog matrix) chip developed by a collaboration between the CEA/DAPNIA and the IN2P3/LAL. This board is well suited for acquisition of fast analog signals.
VME interface supports A32/D64, A32/D32, A24/D16 modes; GPIB and USB 2.0 are also featured.

14-bit of resolution
2GS/s of sampling rate
USB2.0 Read out.
The fastest 14 bit digitizer on the market!

The module houses four 14 bit ADC channels with 2GHz sampling frequency and 300MHz bandwidth. The measurement is realized in three phases:

- Acquisition: the analog signal is continuously sampled at the sampling frequency in a circular analog memory. The arrival of a trigger signal starts the stopping phase of the sampling. At the end of this phase, the state of the memory is set: it then contains the last 2560 points sampled (out of which 2520 are valid).
- Digitization and Storage: after a stopping command of the acquisition, the samples stored under analog form in the MATACQ chips are rapidly (650µs) re-read and converted into digital data over 14 bits, then stored in a digital memory buffer. The acquisition is informed vof the end of the conversion phase either by polling an internal register, or by an interrupt.
- Reading: readout rate is close to 1 kHz with a performing A32/D64 system for a full readout of a 4-channel board.

(CEA/DAPNIA & IN2P3/LAL Design)

- **4 channel**
- **14 bit 2 GS/s Switched Capacitor digitizer**
- **2 GS/s max sampling frequency**
- **Full Scale Range: ± 1 V**
- **125 µV LSB**
- **2520 usable sampled points**
- **Five trigger mode operation (on signal, external, auto, auto+normal, internal random) with rising or falling edge detection**
- **USB2.0 interface**
- **GPIB interface**
- **Integral non linearity: ± 0.1%**
- **Differential non linearity: ± 0.005%**

Ordering Information

Code	Description
WV1729AXAAAA	V1729A - 4 Ch. 14 bit 2 GS/s (300 MHz bandwidth) Switched-Capacitor Digitizer

V551B Sequencer for V550 - V550A C-RAMS

T25

The Mod. V551B is a 1-unit wide VME module which can handle data acquired by some of the well known front-end chips (VA, Amplex, Gasplex, etc.). The V551 has been developed to control the signals from/to the Mod. V550 and V550A C-RAMS (CAEN Readout for Analog Multiplexed Signals). A single V551B can control up to 19 C-RAMS modules, enabling the read out of 76608 multiplexed detector channels. The module works in A24/A32 mode, the data transfer occurs in D16 mode. C-RAMS can be programmed via VME to readout groups of up to 2016 detector channels per block; the multiplexing frequency can be set from 100 kHz to 5 MHz with programmable duty cycle.
The module houses a VME RORA interrupter; it is possible to program, via VME, the interrupt generation on the condition that the DRDY signal is asserted, indicating that at least one channel has data to be read out.

- **Control of up to 19 V550 – V550A modules**
- **5 MHz maximum multiplexing frequency**
- **Programmable duty cycle**

Ordering Information

Code	Description
WV551BXBAAAA	V551BB - C-RAMS Sequencer

V550 - V550A CAEN Readout for Analog Multiplexed Signals

T9

The Mod. V550 and V550A CAEN Readout for Analog Multiplexed Signals (C-RAMS) are 1-unit wide VME modules housing 2 independent Analog to Digital Conversion channels, to be used for the readout of analog multiplexed signals coming from some of the well known front-end chips (Amplex, Gasplex, VA, etc.). Each channel of the module accepts positive, negative or differential input signals, amplifies and feeds them to a 10 bit ADC (12 bit for the V550A). The sensitivity (mV/bit) can be selected among 4 different values with relative ratios of 1, 2, 5 and 10. The input signals are sampled by the ADC up to a 5 MHz frequency and their digital value is compared to a threshold for each channel. If the signal is over the channel's threshold, a programmable individual pedestal is subtracted and the result is stored in a 2k x 32 bit FIFO.
The modules work in A24/A32, D32 mode. Block Transfer mode is also available. A positive open-collector signal ("DRDY") allows to obtain a wired-OR Global Data Ready signal. A fast CLEAR signal is also available for a cycle abort. It is also possible to operate the modules in TEST mode (VME selectable) by simulating some input patterns.
The Mod. V550 and V550A can be controlled by the CAEN Mod. V551B C-RAMS Sequencer.

- **2 independent ADC blocks**
- **Four ranges: 0.15, 0.30, 0.75 and 1.50 V**
- **Resolution: 12 bit (V550A) or 10 bit (V550)**
- **5 MHz maximum sampling rate**
- **Designed for multiplexed signals**
- **Up to 2016 detector channels per block**
- **Programmable zero suppression and pedestal subtraction**
- **Controlled by the V551B Sequencer**

Ordering Information

Code	Description
WV550XBAAAAA	V550B - CAEN Readout for Analog Multiplex. Signals (10 bit)
WV550AXBAAAA	V550AB - CAEN Readout for Analog Multiplex. Signals (12 bit)

V974 4 Channel Variable Gain Fast Amplifier

T11

The Mod. V974 is a 4 channel fast rise time amplifier housed in a 1-unit VME module; each channel features a voltage gain adjustable from 1 to 10 in x1 steps. Channels are non-inverting and bipolar: they amplify both positive and negative signals. Input bandwitdth is 170 MHz for signals up to 50 mVpp and decreases for larger ones (up to 100 MHz @ 400 mVpp). Gain setting is performed independently for each channel via four rotary handles. Channels can be cascaded in order to obtain larger gain values. Each channel is provided with three LEMO 00 connectors, one for the input and two bridged for the output. The board features a ±2 V output dynamics. 4 screw-trimmers (one per channel) allow the offset calibration which operates over a ±25 mV range. The features include an output short circuit protection.

- **Input bandwidth up to 170 MHz**
- **x10 adjustable gain with x1 steps**
- **50 Ohm input impedance**
- **±2 V output dynamics**
- **Drives 50 Ohm loads**
- **Cascadeable channels**
- **Rise/fall time <3 ns with a 25 mV unipolar input amplitude**
- **I/O delay <3 ns**

Ordering Information

Code	Description
WV974XBAAAAA	V974B - 4 Channel Variable Gain Fast Amplifier

V975 8 Channel Fast Amplifier

T11

The Mod. V975 is an 8 channel fast rise time amplifier housed in a 1-unit VME module; each channel features a fixed voltage gain of 10. Channels are bipolar, non-inverting and can be cascaded in order to obtain larger gain values. Input bandwitdth is 250 MHz for signals up to 50 mVpp and decreases for larger ones (up to 110 MHz @ 400 mVpp). Each channel is provided with three LEMO 00 connectors, one for the input and two bridged for the output. The board features a ±2 V output dynamics. Screw-trimmers (one per channel) allow the offset calibration which operates over a ±25 mV range. The features include an output short circuit protection.

- **Input bandwidth up to 250 MHz**
- **x10 fixed gain**
- **50 Ohm input impedance**
- **±2 V output dynamics**
- **Drives 50 Ohm loads**
- **Cascadeable channels**
- **Rise/fall time <1.5 ns with a 25 mV unipolar input amplitude**
- **I/O delay <3 ns**

Ordering Information

Code	Description
WV975XBAAAAA	V975B - 8 Channel Fixed Gain Fast Amplifier

V859 Dual Attenuator

T13

The Model V859 is a passive dual section attenuator housed in a 1-unit VME module; the module does not require any power supply since it is made up of resistive cells. Attenuation ranges from 0 to 44.5 dB for each section (0.5 dB steps). The two sections can be cascaded in order to obtain a single section featuring a 0÷89 dB (0.5 dB step) attenuation.
Each section is provided with two LEMO 00 connectors, one for the input (50 Ohm impedance) and one for the output, and seven toggle switches for attenuation setting; an additional switch, allows to cascade the two sections.

- **Attenuation adjustable from 0 to 44.5 dB**
- **Cascadeable sections**
- **Input bandwidth larger than 300 MHz**
- **100 mW maximum input power**
- **No power supply required**

Ordering Information

Code	Description
WV859XAAAAAA	V859 - Dual Attenuator (0 to 44.5 dB)

V1495 General Purpose VME Board

T15 • T19 • T21 • T28

The Mod. V1495 is a VME 6U board, 1U wide, suitable for various digital Gate/Trigger/Translator/Buffer/Test applications, which can be directly customised by the User, and whose management is handled by two FPGA. The first one is the FPGA "Bridge", used for the VME interface and for the connection between the VME and the 2nd FPGA (FPGA "User") through a proprietary local bus. The FPGA "Bridge" manages also the programming via VME of the FPGA "User".

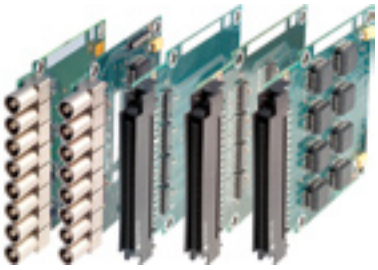
The re-configuration of your system made easy!
All the power of the FPGA.
All the flexibility of swappable IOs.

The FPGA "User" (Cyclone EP1C20) manages the front panel I/O channels and is substantially an empty FPGA. It is available to be programmed by the User according to the desired logic function. The I/O channel digital interface is composed by four sections placed on the motherboard. The cannel Interface can be freely expanded or modified by the user by adding or exchanging up to three independent mezzanine boards, choosing between the five available types:

- A395A 32 LVDS/ECL/PECL input channels
- A395B 32 LVDS output channels
- A395C 32 ECL output channels
- A395D 8 NIM/TTL input/output channels
- A395E 8 Analog output channels 16 bit resolution

Therefore, the Mod. V1495 can achieve a maximum number of 194 I/O channels.
A Mounting Option is necessary in order to install three A395C on the V1495 (see Ordering Options).
The FPGA "User" can be programmed "on the fly" via VME, without any external hardware tools, without disconnecting the board from the set up, and without resetting it or turning the crate off. A flash memory on the board stores the programming file, which can be loaded to the FPGA "User" at any moment. Four (independent, digital, programmable, asynchronous, chainable) timers, are available for Gate/Trigger applications.
The unit is supported by a free "FPGA demo firmware", but custom applications can be developed as well.
The Mod. V1495 has been developed in the framework of the european project EURITRACK, which belongs to the Sixth Framework Programme (FP6).

- **User customisable FPGA Unit (with preloaded demo code)**
- **LVDS/ECL/PECL inputs (differential)**
- **64 inputs, expandable to 162 (with 32 outputs)**
- **32 outputs, expandable to 130 (with 64 inputs)**
- **I/O delay smaller than 15 ns (in Buffer Mode)**
- **Programmable 3-color LED**
- **Libraries (C and LabView) and Software tools for Windows and Linux**



Ordering Information

Code	Description	
WV1495XAAAAA	V1495 - General Purpose VME Board	
WA395XAAAAAA	A395A - 32 LVDS/ECL/PECL input channels interface for V1495	
WA395XBAAAAA	A395B - 32 LVDS output channels interface for V1495	
WA395XCAAAAA	A395C - 32 ECL output channels interface for V1495	
WA395XDAAAAA	A395D - 8 NIM/TTL input/output channels interface for V1495	
WA395XEAAAAA	A395E - 8 channel 16Bit ±5V DAC for V1495	NEW
WA967XAAAAAA	A967 - 32 Channel Cable Adapter (1x32 to 2x16) for V767, V862, V1190, VX1190, V1495	
WPERS0149501	V1495 Customization - 3 A395C Mounting Option	
WFW1495SCXAA	FW1495SC - 128 Channels Latching Scaler for V1495	NEW

Piggyback Boards	A395A	A395B	A395C	A395D	A395E NEW
No. of channels	32	32	32	8	8
Channel type	Digital Input	Digital Input	Digital Input	Digital I/O selectable	Analog output
Description	Differential LVDS/ECL/PECL	Differential LVDS	Differential ECL	NIM/TTL	16 bit resolution Output range: ± 5V @10 kΩ RL ± 4V @200Ω RL
Note	single ended TTL optional	LVDS 100Ω RI	ECL	NIM/TTL selectable 50Ω Rt	DAC board equipped with V1495 Firmware and VHDL source for custom development
Bandwidth	200MHz	250MHz	300MHz	250MHz	Tbd
Front panel connector	3M P50E-068-P1-SR1 type (34+34) pins	3M P50E-068-P1-SR1 type, (34+34) pins	3M P50E-068-P1-SR1 type, (34+34) pins	LEMO 00	LEMO 00

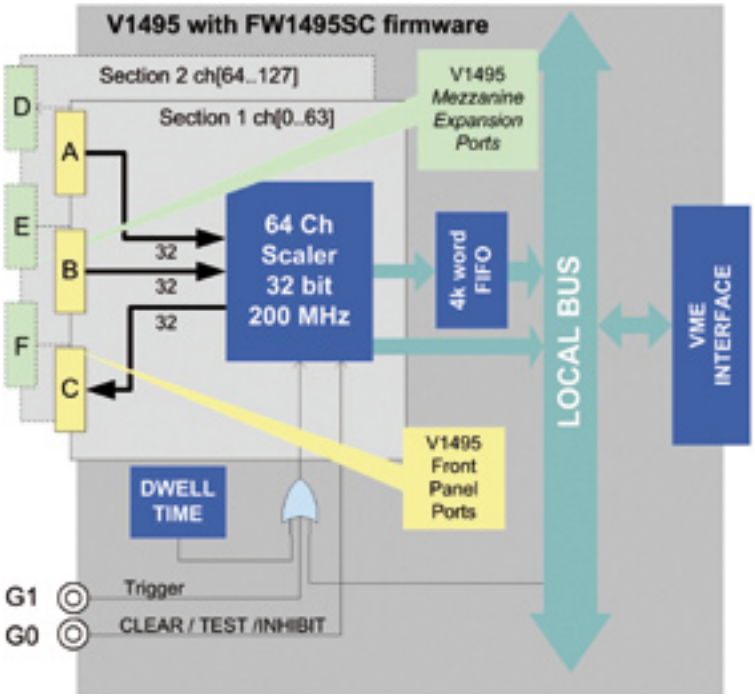
FW1495SC 128 Ch 270 MHz Multievent Latching Scaler Firmware

T24

NEW

FW1495SC is a FPGA firmware for CAEN V1495 model that allows to use the Mod. V1495 as a multievent latching scaler housing up to 128 independent counting channels. Each channel has 32 bit counting depth and accepts LVDS/ECL/PECL and NIM/TTL (max 16 channels) inputs; the maximum input frequency is 270 MHz. The board has a FIFO memory that stores the values of the counter, latched "On the fly" at the trigger arrival, while the counting goes on.
The Trigger signal can be provided by an external NIM/TTL signal or by a VME request. It is also possible to generate a periodical Trigger signal by means of an internal programmable timer.

The counters can be also read out "On the fly" real time via VME. A programmable General Input signal (NIM /TTL) can be programmed as CLEAR, TEST or VETO (in common for all channels).



- **Up to 128 Channel Latching Scaler**
- **270 MHz counting frequency**
- **32 bit channel depth**
- **Multichannel scaler operation with programmable dwell time from 1 µsec to ~ 1 hour**
- **4 k x 32 bit multievent buffer memory**
- **Trigger time tag**
- **VME Block Transfer support**

Ordering Information

Code	Description
WFW1495SCXAA	FW1495SC - 128 Channels Latching Scaler for V1495

V976 Quad 4 Fold AND/OR/MAJ, NIM-TTL TTL-NIM Translator, Fan-In Fan-Out

T15 • T19 • T28

The Mod. V976 is a 1-unit VME module housing four 4-input Coincidence Fan in/Fan out and NIM – TTL / TTL – NIM adapter sections. Each section features 4 inputs and 4 outputs on LEMO 00 connectors and can operate as a 4 channel level translator or as AND/OR gate. It is possible to use two or four sections together to obtain an 8 or 16 input majority
The logic functions can be selected via front-panel and internal switches. Some extra functions, such as a 1 to 12 Fan Out, can be performed by cascading properly the module's sections.
The module accepts NIM and TTL inputs; the output can be programmed to provide NIM or TTL levels, either direct or inverted.

- **Four independent sections with four channels each**
- **TTL and NIM inputs automatically detected**
- **NIM/TTL selectable output level**
- **AND, OR, Majority function with selectable number of inputs**
- **Logic Fan In / Fan Out**
- **Direct or inverted output**

Ordering Information

Code	Description
WV976XBAAAAA	V976B - Quad 4 Fold AND/OR/MAJ, NIM-TTL TTL-NIM Level Translator and Fan-In Fan-Out

V1718 VME-USB 2.0 Bridge

T16

The Mod. V1718 is a 1-unit wide 6U VME master module which can be operated from the USB port of a standard PC; the board can perform all the cycles foreseen by the VME64 (except those intended for 3U boards). The board can operate as VME System Controller (normally when plugged in the slot 1) acting as Bus Arbiter in Multimaster systems.
The VME bus activity can be monitored in detail, both locally (through a LED display) and remotely. The front panel includes also 5 TTL/NIM programmable outputs on LEMO 00 connectors (default assignment is: DS0/1, AS, DTACK, BERR and LOCATION MONITOR) and two programmable TTL/NIM inputs (on LEMO 00 connectors). The I/Os can be programmed via USB in order to implement functions like Timer, Counter, Pulse generator, I/O register, etc.
The V1718 – PC interface is USB 2.0 compliant, USB data transfer takes place through the High Speed Bulk Transaction protocol; the sustained data rate on the USB is up to 30 MByte/s in BLT Read cycles. Thanks to the 128KB memory buffer, the activity on the VME bus is not slowed down by the transfer rate on the USB port.
The Module is provided with drivers which support the use with the most common PC platforms (Windows 2000/XP, Vista, Linux); libraries and useful example programs in C/C++, Visual Basic and LabView are provided as well. Firmware upgrade is possible via USB.

- **No boot required, ready at power ON**
- **Up to 30 MByte/s sustained data transfer rate**
- **VME Master (arbiter or requester)**
- **VME Slave (register and test RAM access)**
- **Cycles: R/W, RMW, BLT, MBLT, IACK, ADO, ADOH**
- **Addressing: A16, A24, A32, CR/CSR, LCK**
- **Data width: D8, D16, D32, D64**
- **System Controller capabilities**
- **Interrupt handler**
- **Front panel Dataway Display (available also from PC and VME)**
- **5 outputs and 2 inputs, NIM or TTL, fully programmable**
- **Libraries, Demos (C and LabView) and Software tools for Windows and Linux**

Ordering Information

Code	Description
WV1718XAAAAA	V1718 - VME-USB 2.0 Bridge
WVX1718XAAAA	VX1718 - VME-USB 2.0 Bridge

V2718 VME-PCI Optical Link Bridge

T16

The Mod. V2718 is a 1-unit wide 6U VME master module, which can be controlled by a standard PC equipped with PCI or PCIe CAEN Controller cards (Models. A2818 and A3818).

Daisy-chain your systems by CAEN controllers!! PCI and PCI-Express options combined with the speed of the optical link.

The connection between the V2718 and the A2818 takes place through an optical fiber cable (AY2705, AY2720, AI2705, AI2720). Multi crate sessions can be easily performed, since up to eight daisy chained (via optical fiber cables) V2718 can be controlled by one A2818/A3818, thus building a CONet (Chainable Optical Network).

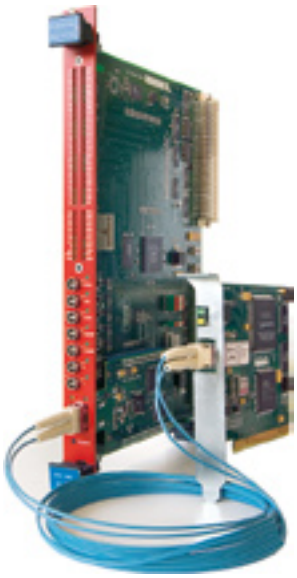
The V2718 can perform all the cycles foreseen by the VME64 (except those intended for 3U boards). The board can operate as VME System Controller (normally when plugged in the slot 1) acting as Bus Arbiter in Multimaster systems.

The VME bus activity can be monitored in detail, both locally (through a LED display) and remotely. The front panel includes also 5 TTL/NIM programmable outputs on LEMO 00 connectors (default assignment is: DS0/1, AS, DTACK, BERR and LOCATION MONITOR) and two programmable TTL/NIM inputs (on LEMO 00 connectors). The I/Os can be programmed in order to implement functions like Timer, Counter, Pulse generator, I/O register, etc.

The sustained data transfer rate is up to 70 MByte/s. Thanks to the 128KB memory buffer, the activity on the VME bus is not slowed down by the transfer rate on the CONet when several V2718s share the same network.

The Module is provided with drivers which support the use with the most common PC platforms (Windows 2000/XP, Vista, Linux); libraries and useful example programs in C/C++, Visual Basic and LabView are provided as well. Future firmware upgrade is possible via PCI/PCIe.

- **No boot required, ready at power ON**
- **Daisy chain capability**
- **PCI 32bit / 33MHz**
- **Up to 70 MByte/s sustained data transfer rate**
- **VME Master (arbiter or requester)**
- **VME Slave (register and test RAM access)**
- **Cycles: R/W, RMW, BLT, MBLT, IACK, ADO, ADOH**
- **Addressing: A16, A24, A32, CR/CSR, LCK**
- **Data width: D8, D16, D32, D64**
- **System Controller capabilities**
- **Interrupt handler**
- **Front panel Dataway Display (available also from PC and VME)**
- **5 outputs and 2 inputs, NIM or TTL, fully programmable**
- **Libraries, Demos (C and LabView) and Software tools for Windows and Linux**



Ordering Information

Code	Description	
WA2818XAAAAA	A2818 - PCI Optical Link Controller	
WK2718XAAAAA	V2718KIT - VME-PCI Bridge (V2718) + PCI Optical Link (A2818) + Optical Fibre 5m duplex (AY2705)	
WV2718XAAAAA	V2718 - VME-PCI Bridge	
WKX2718XAAAA	VX2718KIT - VME-PCI Bridge (VX2718) + PCI Optical Link (A2818) + Optical Fibre 5m duplex (AY2705)	
WVX2718XAAAA	VX2718 - VME-PCI Bridge	
WAY2705XAAAA	AY2705 - Optical Fibre 5 m. duplex	
WAY2720XAAAA	AY2720 - Optical Fibre 20 m. duplex	
WAI2703XAAAA	AI2703 - Optical Fibre 30 cm. simplex	
WAI2705XAAAA	AI2705 - Optical Fibre 5 m. simplex	
WAI2720XAAAA	AI2720 - Optical Fibre 20 m. simplex	
WA3818AXAAAA	A3818 - PCIe 1 Optical Link Controller	✹
WA3818BXAAAA	A3818 - PCIe 2 Optical Link Controller	✹
WA3818CXAAAA	A3818 - PCIe 4 Optical Link Controller	✹

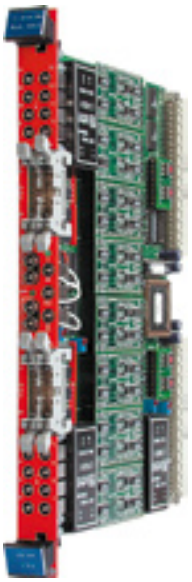
V812 16 Channel Constant Fraction Discriminator

T18

The Mod. V812 is a 1-unit wide VME module housing a 16 channel constant fraction discriminator. The module accepts 16 negative inputs and generates precise ECL pulses when the input signals exceeds a given threshold: constant fraction technique allows to precisely determine the timing of the discrimination. The pulse forming stage of the discriminator produces an output pulse whose width is adjustable in a range from 15 ns to 250 ns via VME. Moreover, in order to protect against multiple pulsing, it is possible to program via VME a dead time, from 150 ns to 2 µs, during which the discriminator is inhibited from retriggering. The discriminator thresholds are individually settable via VME in a range from -1 mV to -255 mV (1 mV step) through an 8-bit DAC. Each channel can be turned on or off via VME by using a mask register. A Current Sum output generates a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load). A MAJORITY output provides a NIM signal if the number of input channels over threshold exceeds the MAJORITY programmed value. Several V812 boards can be connected in a daisy chain via the Current Sum output: in this case, by switching the majority logic to External, it is possible to obtain a Majority signal when the number of active channels in the chained modules exceeds a global Majority level. The logic OR of discriminator outputs is available on a front panel NIM signal.

Need a precise discrimination timing? Programmable output width? OR, Current Sum and MAJORITY outputs? This is your unit!

- **Thresholds individually programmable via VME**
- **Constant fraction for precise discrimination timing**
- **ECL outputs with fan-out of two**
- **Programmable output width**
- **Global VETO and TEST inputs**
- **Mask register for individual channel enable/disable**
- **OR, CURRENT SUM and MAJORITY outputs**



Ordering Information

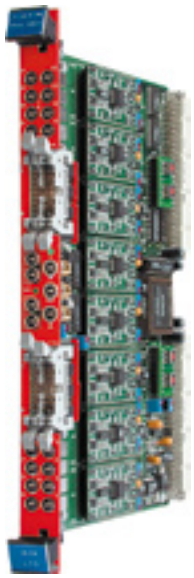
Code	Description
WV812XBAAAAA	V812B - 16 Channel Constant Fraction Discriminator

V814 16 Channel Low Threshold Discriminator

T18

The Mod. V814 is a 1-unit wide VME module housing a 16 channel low threshold discriminator. The module accepts 16 negative (positive on request) inputs and produces 16 differential ECL outputs with a fan-out of two on four front panel flat cable connectors. Maximum input frequency is 60 MHz. The pulse forming stage of the discriminator produces an output pulse whose width is adjustable in a range from 6 to 95 ns via VME. The discriminator thresholds are individually settable in a range from -1 mV to -255 mV (1 mV step), via VME through an 8-bit DAC; a positive input version (Model V814 P), with the thresholds settable in the 1 mV to 255 mV range, is also available. Each channel can be turned on or off via VME by using a mask register. A Current Sum output generates a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load). A MAJORITY output connector provides a NIM signal if the number of input channels over threshold exceeds the MAJORITY programmed value. Several V814 boards can be connected in a daisy chain via the Current Sum output: in this case, by switching the majority logic to External, it is possible to obtain a Majority signal when the number of active channels in the chained modules exceeds a global Majority level. The logic OR of discriminator outputs is available on a front panel NIM signal.

- **Thresholds individually programmable via VME**
- **ECL outputs with fan-out of two**
- **Non updating operation**
- **Programmable output width**
- **Mask register for individual channel enable/disable**
- **Global VETO and TEST inputs**
- **OR, CURRENT SUM and MAJORITY outputs**
- **High sensitivity with small signals**
- **Negative or Positive input version available**



Ordering Information

Code	Description
WV814XBAAAAA	V814B - 16 Channel Low Threshold Discriminator
WV814XPBAAAA	V814PB - 16 Channel Low Threshold Discriminator Positive Inputs

V895 16 Channel Leading Edge Discriminator

T18

The Mod. V895 is a 1-unit wide VME module housing a 16 channel leading edge discriminator. The module accepts 16 negative (positive on request) inputs and produces 16 differential ECL outputs with a fan-out of two on four front panel flat cable connectors. Maximum input frequency is 140 MHz. The pulse forming stage of the discriminator produces an output pulse whose width is adjustable in a range from 5 to 40 ns via VME. Each channel can work both in Updating and Non-Updating mode according to on-board jumpers position. The discriminator thresholds are individually settable in a range from -1 mV to -255 mV (1 mV step), via VME through an 8-bit DAC. The minimum detectable signal is -5 mV. Each channel can be turned on or off via VME by using a mask register. A Current Sum output generates a current proportional to the input multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load). A MAJORITY output connector provides a NIM signal if the number of input channels over threshold exceeds the MAJORITY programmed value. Several V895 boards can be connected in a daisy chain via the Current Sum output: in this case, by switching the majority logic to External, it is possible to obtain a Majority signal when the number of active channels in the chained modules exceeds a global Majority level. The logic OR of discriminator outputs is available on a front panel NIM signal.

- **Thresholds individually programmable via VME**
- **ECL outputs with fan-out of two**
- **Selectable Updating/Non Updating mode**
- **Programmable output width**
- **Global VETO and TEST inputs**
- **Mask register for individual channel enable/disable**
- **OR, CURRENT SUM and MAJORITY outputs**

Ordering Information

Code	Description
WV895XBAAAAA	V895B - 16 Channel Leading Edge Discriminator

V925 Quad Linear Fan In-Fan Out

T19

The Mod. V925 is a 1-unit VME module which houses three 4 In / 4 Out and one 3 In / 3 Out sections; one Discriminator channel is also featured. Each Fan In-Fan Out section produces on all its output connectors, the sum of the signals fed to the inputs, eventually inverted. Fan in/Fan out inputs are bipolar, while the output can be either inverting or non inverting (jumper selectable independently for each section). Both input and output signals are DC coupled.
Maximum input amplitude is ±1.6 V. Moreover each Fan In-Fan Out section features a screwdriver trimmer which allows the DC offset adjustment. The discriminator channel has one DC coupled input (trigger slope leading/trailing is jumper selectable), the threshold is screwdriver adjustable and monitorable via test point; the output is NIM standard, its width is screwdriver adjustable as well. Front panel LEDs allow to monitor all the mode, gain and polarity adjustments performed via internal jumpers.

- **Four independent sections**
- **Bipolar inputs**
- **Three 4 In / 4 Out and one 3 In / 3 Out sections**
- **One Discriminator channel**
- **Inverting or non-inverting mode independently selectable on each section**
- **120 MHz bandwidth**

Ordering Information

Code	Description
WV925XAAAAAA	V925 - Quad Linear Fan In-Fan Out

V259 16 Bit Strobed Multihit Pattern Unit

T21

The Mod. V259 is a 1-unit wide VME 6U module able to store internally a 16 bit input pattern which can be read via the VME bus; the board has 16 inputs; an input coincidence circuit, controlled by a GATE signal, selects the hits which are stored in a Pattern register. If a channel has been already hit during the GATE window, the unit sets the relevant bit in a Multiplicity register.
The unit provides a fast OR signal of the inputs. Input signals can be std. NIM or ECL depending on the purchased version (V259N or V259E). The control signals (GATE, CLEAR, FAST OR) are NIM for both versions.
The unit has an A24, D16 VME interface.
(CEA-IRF SACLAY design)

- **16 input channels ANDed with a GATE signal**
- **Two versions: NIM or ECL inputs**
- **FAST CLEAR input**
- **FAST OR output**
- **Multiple hits register**

Ordering Information

Code	Description
WV259ECLAAAA	V259E - 16 Bit Strobed Multi-Hit Pattern Unit (ECL Level)
WV259NIMAAAA	V259N - 16 Bit Strobed Multi-Hit Pattern Unit (NIM Level)

V977 16 Channel Input/Output Register (Status A)

T21

The Mod. V977 is a 1-unit wide VME module that can work either as 16 channel general purpose I/O Register or as Multihit Pattern Unit; the operating mode is selected via VME and is signalled via front panel LEDs. The module has 16 Inputs/Outputs; an on-board switch allows to select between NIM and TTL output signals, NIM and TTL input signals are both accepted; 2 Leds signal the I/O status of each channel. The module features an additional channel (TEST CHANNEL), which allows to send a test pulse via a front panel pushbutton. Input channels can be individually/globally masked via VME or globally via a front panel GATE input. The channel status can be cleared either via VME or via the front panel common CLEAR input. The channels global OR and /OR outputs are available as front panel signals and can be eventually masked. GATE and CLEAR signals can be either NIM or TTL; OR and /OR can be set at NIM or TTL level in the same way of the output channels. The module houses also a fully programmable VME RORA INTERRUPTER that generates a VME interrupt request when the OR of a selected set of output channels has a TRUE status. Live insertion is supported.

- **NIM and TTL inputs/outputs**
- **Individual channel enabling/disabling**
- **Software Input/Output generation**
- **Fully programmable RORA Interrupter**
- **Pushbutton TEST signal**
- **Satus A capabilities**
- **Live insertion**

Ordering Information

Code	Description
WV977XBAAAAA	V977B - 16 Channel I/O Register (Status A)

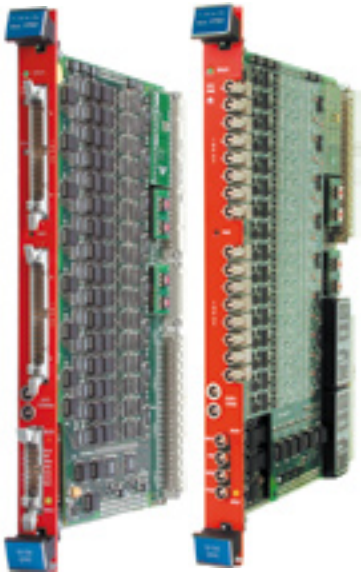
V792 - V792N 32 / 16 Channel Multievent QDC

T23

The Mod. V792 is a 1-unit wide VME 6U module housing 32 Charge-to-Digital Conversion channels with current integrating negative inputs (50Ω impedance). For each channel, the input charge is converted to a voltage level by a QAC (Charge to Amplitude Conversion) section. Input range is 0 ÷ 400 pC. The outputs of the QAC sections are multiplexed and subsequently converted by two fast 12-bit ADCs. The integral non linearity is ±0.1% of Full Scale Range (FSR) measured from 5% to 95% of FSR. The ADCs use a sliding scale technique to improve the differential non-linearity.
The Mod. V792N houses 16 input channels on LEMO 00 connectors and shares most of the other features with the Mod. V792.
The Mod. V792/V792N offers a 32 event buffer memory, A24/A32 addressing mode, D16, D32, BLT32/MBLT64 and CBLT32/CBLT64 data transfer mode. Multicast commands are also supported. A 16 ch. decoupling board Mod. A992 (see Accessories section) is available for the Mod. V792 to avoid ground loops and signal reflections when long flat cable (110Ω) connections to the 50Ω inputs are used (one V792 requires two A992 boards). A 16 channel flat cable to LEMO input adapter, Mod. A392 (see Accessories section) is also available for the Mod. V792 (one V792 requires two A392 boards).
The board has a special circuitry that allows it to be removed from and inserted in a powered crate without switching the crate off.

Sliding scale technique implemented to improve the differential non linearity
A great seller for the Charge-to-Digital conversion.

- **0 ÷ 400 pC input range**
- **Full 12bit resolution**
- **100 fC LSB**
- **5.7 µs / 32 ch and 2.8 µs / 16 ch conversion times**
- **600 ns fast clear time**
- **Zero and overflow suppression for each channel**
- **±0.1% integral non linearity**
- **±1.5% differential non linearity**
- **32 event buffer memory**
- **BLT32/MBLT64/CBLT32/CBLT64 data transfer**
- **Multicast commands**
- **Live insertion**
- **Libraries (C and LabView) and Software tools for Windows and Linux**



Ordering Information

Code	Description
WV792XACAAAA	V792AC - 32 Channel Multievent QDC (No 12V DCDC, live ins)
WV792XNCAAAA	V792NC - 16 Channel Multievent QDC (No 12V DCDC, live ins)

V862 32 Channel Multievent Individual Gate QDC

T23

The Mod. V862 is a 1-unit wide VME 6U module housing 32 Charge-to-Digital Conversion channels with current integrating negative inputs. Each channel has an independent gate input (GATE I) logically ANDed with a COMMON GATE input; the input charge on the I-th channel is converted to a voltage level by a QAC (Charge to Amplitude Conversion) section when both the GATE I and COMMON GATE signals are active. Input range is 0 ÷ 400 pC. The integral non linearity is ±0.1% of full scale range (FSR), measured from 2% to 97% of FSR; the differential non linearity is ±1.5% of FSR, measured from 3% to 100% of FSR. The ADCs use a sliding scale technique to reduce the differential non-linearity.
The outputs of the QAC sections are multiplexed and subsequently converted by two fast 12-bit ADCs (5.7 µs for 32 channels). The Mod. V862 offers a 32 event buffer memory; programmable zero suppression and trigger counter complete the features of the unit. The module works in A24/A32 mode. The data transfer occurs in D16, D32, BLT32, MBLT64 or CBLT32/CBLT64 mode. The unit also supports the Multicast commands.
The board supports live insertion.

Our well known QDC inproved with the individual gate per channel.

- **Individual Gate input per channel**
- **0 ÷ 400 pC input range**
- **Full 12-bit resolution**
- **100 fC LSB**
- **5.7 µs / 32 ch conversion time**
- **32 event buffer memory**
- **600 ns fast clear time**
- **Zero and overflow suppression for each channel**
- **±0.1% integral non linearity**
- **±1.5% differential non linearity**
- **BLT32/MBLT64/CBLT32/CBLT64 data transfer**
- **Multicast commands**
- **Live insertion**
- **Libraries (C and LabView) and Software tools for Windows and Linux**

Ordering Information

Code	Description
WV862XACAAAA	V862AC - 32 Channel Multievent QDC With Individual Gate (live insertion)
WA967XAAAAAA	A967 - 32 Channel Cable Adapter (1x32 to 2x16) for V767, V862, V1190, VX1190, V1495

V965 - V965A 16/8 Channel Dual Range Multievent QDC

T23

The board is a 1-unit wide VME 6U module that houses 16 (V965) or 8 (V965A) Charge-to-Digital Conversion channels with current integrating negative inputs (50 Ohm impedance).
For each channel, the input charge is converted to a voltage level by a QAC (Charge to Amplitude Conversion) section. Each QAC output is then converted by two ADCs in parallel; one ADC is preceded by a x1 gain stage, the other by a gain of about 9x stage. A dual input range is then featured: 0 ÷ 900 pC (200 fC LSB) and 0 ÷ 100 pC (25 fC LSB); this allows to avoid saturation with big charge pulses while increasing resolution with small ones.
The outputs of the QAC sections are multiplexed and subsequently converted by two fast 12-bit ADCs. The ADCs use a sliding scale technique to improve the differential non-linearity. Programmable zero suppression, multi-event buffer memory, trigger counter and test features complete the flexibility of the unit.
The module works in A24/A32 addressing mode; the data transfer occurs in D16/D32/BLT32/MBLT64. The module also supports the chained block transfer (CBLT32/CBLT64) and the multicast commands.
The board supports live insertion.

Avoid saturation with big input signals and increase resolution with small ones with the CAEN Dual Range Charge ADC!

- **Two simultaneous ranges: 0 ÷ 900 pC / 0÷100 pC**
- **12 bit resolution with 15 bit dynamics**
- **25 fC LSB on low range, 200 fC LSB on high range**
- **2.8 µs / 8 ch conversion time**
- **600 ns fast clear time**
- **Zero and overflow suppression for each channel**
- **±0.1 % Integral non linearity**
- **±1.5 % Differential non linearity**
- **32 event buffer memory**
- **BLT32/MBLT64/CBLT32/CBLT64 data transfer**
- **Multicast commands**
- **Live insertion**
- **Libraries, Demos (C and LabView) and Software tools for Windows and Linux**

Ordering Information

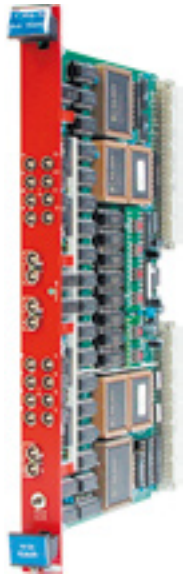
Code	Description
WV965XBAAAAA	V965 - 16 Channel Dual Range Multievent QDC (No 12V DCDC, live ins)
WV965AXBAAAA	V965A - 8 Channel Dual Range Multievent QDC (No 12V DCDC, live ins)

V560 16 Channel Scaler

T24

The Mod. V560 is a single width VME module which houses 16 independent 32 bit counting channels at the maximum input frequency of 100 MHz.
Each channel can be software enabled to generate an interrupt signal when the counter is full. The interrupt level and the correlated vector can be set and read via std. VME write and read cycles. Each channel can be cascaded with the following one through internal jumpers to produce a 64 bit counting depth. The status of the internal jumpers can be read via std. VME read cycles.
All the channels can be cleared via the relevant VME command and via the front panel pushbutton. The unit has a standard A24/A32, D32 VME interface.

- **NIM input**
- **32 bit deep counting channels**
- **100 MHz counting frequency**
- **Cascadeable couples of channels**
- **Clear, Veto and Test NIM inputs**



Ordering Information

Code	Description
WV560NBAAAAA	V560AN - 16 Channel 32 Bit Scaler NIM

V830 32 Channel Latching Scaler

T24

The model V830 is a 1-unit wide VME 6U Multievent Latching Scaler, housing 32 independent counting channels.
Each channel has 32 bit counting depth and accepts either ECL or LVDS inputs, depending on the purchased version; the maximum input frequency is 250 Mhz. The counters' values can be read on the fly from VME without interfering on data acquisition process.

"Read on the fly" up to the least significant bit. A real 250MHz 32bit latching scaler.

The model V830 is equipped with a 32 k x 32 bit multievent buffer memory which may be used to store and readout accumulated data during subsequent counting.
The Trigger signal can be provided by an external NIM/ECL signal or by a VME request. It is also possible to generate a periodical Trigger signal by means of an internal programmable timer.
The module features VETO and CLEAR ECL inputs and a TEST NIM input (in common for all channels).
The model V830 works in A24/A32 mode and data transfer occurs in D32, BLT32 or MBLT64 mode. The unit also supports the Chained Block Transfer (CBLT32/CBLT64) and the Multicast commands.
The board supports live insertion.

- **Available with either ECL or LVDS inputs**
- **250 MHz counting frequency**
- **32 bit channel depth**
- **Multichannel scaler operation with programmable dwell time from 1.2 µs to 1700 s**
- **BLT32/MBLT64/CBLT32/CBLT64 data transfer**
- **Multicast commands**
- **32 k x 32 bit multievent buffer memory**
- **Live insertion**

Ordering Information

Code	Description
WV830XACAAAA	V830AC - 32 Channel 32 Bit Scaler 250 MHz (With FIFO) ECL inputs
WV830LXCAAAA	V830LC - 32 Channel 32 Bit Scaler 250 MHz (With FIFO) LVDS inputs

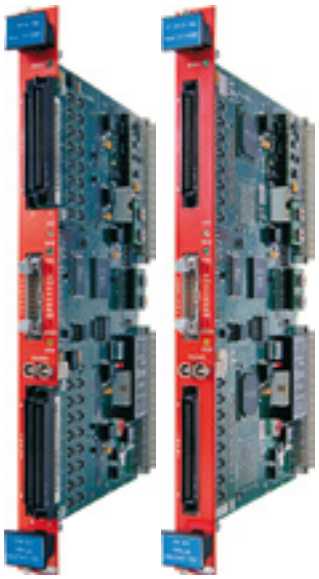
V1190A - V1190B 128/64 Channel Multihit TDC

T26

The board is a 1-unit wide VME 6U module that houses 128 (V1190A) or 64 (V1190B) independent Multi Hit/Multi Event Time to Digital Conversion channels. The unit features High Performance TDC chips, developed by CERN. LSB can be set at 100 ps (19 bit resolution, 52 µs FSR), 200 ps (19 bit, 104 µs FSR) or 800 ps (17 bit, 104 µs FSR). The channels can be enabled for the detection of hits rising/falling edges or for their width measurement (both the edges' timing, and the hit width can be measured with the selected resolution). For each channel there is a digital adjustment for the zero-ing of any offsets. The data acquisition can be programmed in "EVENTS" ("TRIGGER MATCHING MODE", with a programmable time window) or in "CONTINUOUS STORAGE MODE". Both ECL and LVDS input signals are supported.
The VME interface allows the module to work in A24 and A32 addressing modes. The board houses a 32 k x 32 bit deep Output Buffer, that can be readout via VME in a completely independent way from the acquisition itself. The internal registers are available in D16 mode only, while the Output Buffer is accessible in D32, BLT32 or MBLT64. The module supports also the Chained Block Transfer mechanism and the Multicast commands. The board supports live insertion.

Performant and cost effective.
128 acquisition channels with 3 different sub nanoseconds timing resolution squeezed in a 1U VME module

- 3 programmable ranges: 100 ps LSB (19 bit resolution), 200 ps LSB (19 bit) and 800 ps LSB (17 bit)
- ECL/LVDS inputs automatically detected
- 5 ns Double Hit Resolution
- Leading and Trailing Edge detection
- Trigger Matching and Continuous Storage acquisition modes
- 32 k x 32 bit output buffer
- BLT32/MBLT64/CBLT32/CBLT64 cycles supported
- Multicast commands
- Live insertion
- Libraries, Demos (C and LabView) and Software tools for Windows and Linux



Ordering Information

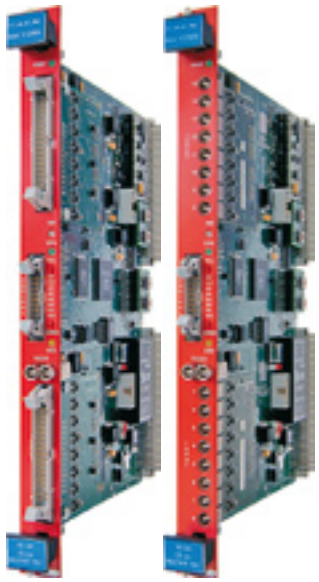
Code	Description
WV1190AEXAAA	V1190A - 128 Ch Multievent Multihit TDC 100-200-800 psec ECL/LVDS
WV1190BEXAAA	V1190B - 64 Ch Multievent Multihit TDC 100-200-800 psec ECL/LVDS
WA967XAAAAAA	A967 - 32 Channel Cable Adapter (1x32 to 2x16) for V767, V862, V1190, VX1190, V1495
WVX1190AEXAA	VX1190A - 128 Ch. Multievent Multihit TDC 100-200-800 psec ECL/LVDS (no JAUX)
WVX1190BEXAA	VX1190B - 64 Ch. Multievent Multihit TDC 100-200-800 psec ECL/LVDS (no JAUX)

V1290A - V1290N 32/16 Channel Multihit TDC

T26

The Mod. V1290A is a 1-unit wide VME 6U module that houses 32 independent Multi Hit/Multi Event Time to Digital Conversion channels. The unit houses 4 High Performance TDC chips, developed by CERN. LSB is 25 ps (21 bit resolution, 52 µs FSR). The module accepts both ECL and LVDS inputs.
The Mod. V1290N houses 16 independent Multi Hit/Multi Event Time to Digital Conversion channels. It houses 2 High Performance TDC chips and shares most of its features with the V1290A. The V1290N module accepts NIM inputs.
The channels can be enabled for the detection of hits rising/falling edges. For each channel there is a digital adjustment for the zero-ing of any offsets. The data acquisition can be programmed in "EVENTS" ("TRIGGER MATCHING MODE", with a programmable time window) or in "CONTINUOUS STORAGE MODE".
The VME interface allows the module to work in A24 and A32 addressing modes. The board houses a 32 k x 32 bit deep Output Buffer, that can be readout via VME in a completely independent way from the acquisition itself. The internal registers are available in D16 mode only, while the Output Buffer is accessible in D32, BLT32 or MBLT64. The module supports also the Chained Block Transfer mechanism and the Multicast commands. The board has a special circuitry that allows it to be removed from and inserted in a powered crate without switching the crate off.

- 25 ps LSB
- 21 bit resolution
- 52 µs full scale range
- 5 ns Double Hit Resolution
- Leading and Trailing Edge detection
- Trigger Matching and Continuous Storage acquisition modes
- 32 k x 32 bit output buffer
- BLT32/MBLT64/CBLT32/CBLT64 cycles supported
- Multicast commands
- Live Insertion
- Libraries, Demos (C and LabView) and Software tools for Windows and Linux



Ordering Information

Code	Description
WV1290AEXAAA	V1290A - 32 Ch Multievent Multihit TDC 25 psec ECL/LVDS
WV1290BNXAAA	V1290N - 16 Ch Multievent Multihit TDC 25 psec NIM
WVX1290AEXAA	VX1290A - 32 Ch. Multievent Multihit TDC 25 psec ECL/LVDS (no JAUX)
WVX1290BNXAA	VX1290N - 16 Ch. Multievent Multihit TDC 25 psec NIM (no JAUX)

V775 - V775N 32 / 16 Channel Multievent TDC

T26

The Mod. V775 is a 1-unit wide VME 6U module housing 32 Time-to-Digital Conversion channels. The Full Scale Range can be selected via VME from 140 ns to 1.2 µs with 8 bit resolution. The board can operate both in COMMON START and in COMMON STOP mode. Each time interval between the COM signal and the input signal is converted into a voltage level by the TAC sections. The outputs of the TAC sections are multiplexed and subsequently converted by two fast ADC modules (5.7 µs conversion time). The Mod. V775N houses 16 channels on LEMO 00 connectors and shares most of its features with the Mod. V775.
The integral non linearity is ±0.1% of full scale range (FSR), measured from 2% to 95% of FSR; the differential non linearity is ±1.5% of FSR, measured from 3% to 100% of FSR. The ADCs use a sliding scale technique to reduce the differential non-linearity.
Programmable zero suppression, multievent buffer memory, trigger counter and test features complete the flexibility of the unit. The module works in A24/A32 ADDRESS mode. The data transfer occurs in D16, D32, BLT32 or MBLT64 mode. The unit supports also the Chained Block Transfer (CBLT32/CBLT64) and the Multicast commands. The boards support live insertion.

- **Full scale range programmable from 140 ns to 1.2 µs**
- **12 bit resolution with 15 bit dynamic range**
- **35 ps LSB**
- **5.7 µs / 32 ch and 2.8 µs / 16 ch conversion times**
- **600 ns fast clear time**
- **Zero and overflow suppression for each channel**
- **±0.1% integral non linearity**
- **±1.5% differential non linearity**
- **32 event buffer memory**
- **BLT32/MBLT64/CBLT32/CBLT64 data transfer**
- **Multicast commands**
- **Live insertion**
- **Libraries, Demos (C and LabView) and Software tools for Windows and Linux**

Ordering Information

Code	Description
WV775XACAAAA	V775AC - 32 Channel Multievent TDC (No 12V DCDC, No live ins)
WV775XNCAAAA	V775NC - 16 Channel Multievent TDC (No 12V DCDC, No live ins)

V972 Delay Unit

T27

The Mod. V972 is a 1-unit wide VME 6U module that houses a delay unit with a range from 0 to 31.5 ns with a 2.6 ns offset. The delay can be set in 0.5 ns steps via front panel toggle switches. The unit is made up of calibrated coaxial cable stubs for high accuracy delay and does not require any power supply. The module features LEMO 00 I/O connectors.

- **Completely passive delay via a set of calibrated coaxial cable stubs (50 Ohm)**
- **0 to 31.5 ns delay with 2.6 ns offset**
- **0.5 ns resolution**
- **±100 ps accuracy on 0.5 to 8 ns delay steps; ±200 ps accuracy on 16 ns step**
- **VSWR < 1.15**

Ordering Information

Code	Description
WV972XAAAAAA	V972 - Delay Unit (2.6 to 34.1 ns)

V993B Dual Timer

T27

The Model V993B Dual Timer is a 1-unit VME module housing two identical triggered pulse generators.
The module produces NIM/TTL (NIM/TTL selection is performed via an on-board switch) and ECL pulses whose width ranges from 50 ns to 10 s when triggered. Output pulses are provided normal and negated.
Timers can be re-triggered with the pulse end marker signal, a short pulse occurring at the end of each output pulse.
The coarse adjustment of the output width is provided via a 9-position rotary switch, the fine adjustment can be performed via either a rotary handle or by providing an external voltage.
The trigger START can be provided via either an external signal (NIM, TTL or ECL) or manually via a front panel switch.
The module features also VETO and RESET input signals.
RESET is also avaible on a front panel switch.
The V993B is equipped with LEMO 00 connectors for NIM/TTL signals and male pin couples for ECL signals.

- **Manual or pulse triggered START (NIM, TTL or ECL)**
- **Monostable or bistable operation**
- **NIM, TTL and ECL output pulses from 50 ns to 10 s**
- **Manual or pulse triggered RESET**
- **(NIM, TTL and ECL) END-MARKER pulse**
- **VETO input**

Ordering Information

Code	Description
WV993XBAAAAA	V993B - Dual Timer

V538A 8 Channel NIM-ECL/ECL-NIM Translator

T28

The Mod. V538A is a 1-unit wide VME module housing 8 independent logic level translators.
Each of the 8 channels accepts a NIM or ECL signal and provides two NIM and two ECL outputs (OUT 0÷7 A, B). The NIM and ECL inputs of each channel are ORed prior to fan-out.
The maximum operating frequency is 300 MHz.
Two front panel input bridged connectors accept a COMMON IN NIM signal, which allows the use of the module as a fan-out of 16 NIM and 16 ECL signals.

- **8 independent NIM to ECL/NIM and ECL to NIM/ECL channels**
- **NIM and ECL fan-out of 2**
- **300 MHz maximum operating frequency**
- **COMMON IN input with a fan-out of 16 (both NIM and ECL)**
- **I/O delay <5 ns**

Ordering Information

Code	Description
WV538XBAAAAA	V538AB - 8 Channel NIM-ECL/ECL-NIM Translato