Advanced Implantation Detector Array (AIDA): Technical Specification version 1

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Objective

The objective of the Advanced Implantation Detector Array (AIDA) project is to develop, commission and exploit a state of the art silicon detector array for decay spectroscopy experiments using the SuperFRS fragment separator at the FAIR accelerator facility based at GSI, Darmstadt, Germany. It is anticipated that AIDA will be operated in conjunction with other detection systems, such as gamma-ray and neutron detector arrays, which requires that AIDA should be very compact while still accepting all ions from the fragment separator.

To achieve these objectives AIDA will use large area double-sided silicon strip detector (DSSSD) and application specific integrated circuit (ASIC) technologies. AIDA will be used for implantation-decay experiments and perform spectroscopy quality measurements of charged particle decays with energies from tens of keV to MeV. The challenge is to achieve this within microseconds of multi-GeV exotic ion implants and with an instrumentation density to match the very high degree of detector segmentation required for the observation and characterisation of long-lived decays.

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1 Introduction

1.1 Implantation-Decay Correlation

Very high energy ($\sim 100 - 200$MeV/u, $A \leq 240$ ions), very exotic (i.e. radioactive) heavy-ions are implanted into a stack of double-sided silicon strip detectors (DSSSDs). These nuclei subsequently undergo radioactive decay emitting low energy β-particles, protons, α-particles, neutrons and γ rays. The charged particles are detected by the DSSSDs. Beta particles are characterised by continuum energy spectra to low energies. Other charged particles are characterised by discrete peaks. The neutrons and γ rays are detected by neutron and gamma detector arrays close packed around the DSSSDs. The detector systems are schematically illustrated in figure 1

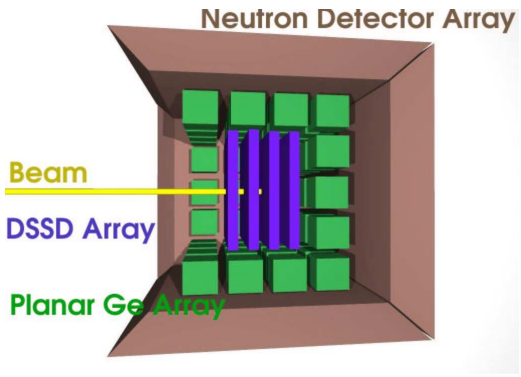

Figure 1: Conceptual illustration of the DEcay SPECtroscopy (DESPEC) detector systems.

The DSSSD strips identify where (x, y) and when (t_0) the nuclei were implanted. Subsequent radioactive decay(s) at the *same* position (x, y) at times $t_1(, t_2 \ldots)$ can be correlated with the implant. Observation of a number of such correlations enables the determination of the energy distribution of the radioactive decay and its half-life (decay time).

If the implantation events are distributed across a highly segmented DSSSD the average time between implants at each position (x, y) is greater than the average decay time and random correlations (two, or more implants at the same position followed by radioactive decays - which decay correlates with which implant ... ?) are minimised. For a given decay time, higher segmentation means a higher total implantation rate.

1.2 Practicalities

The energy deposited by the implant in the DSSSD is ∼GeV, and higher. The energy of the subsequent decay events is ∼MeV. Average time between implantation and decay is $\sim \mu$s−s.

We cannot assume that it will be possible to preempt the arrival of high energy implants by, for example, using external signals to switch the preamplifiers to reset. The instrumentation must detect, respond and recover itself.

DSSSD array area is ∼24cm×8cm. Each layer of DSSSD stack consists of multiple, 1mm thick, DSSSD wafers with a junction and ohmic strip pitch of $\sim 625\mu$m. Strips on one side of the DSSSD wafer are series connected. The stack consists of a maximum of 8 DSSSD layers. Another configuration will have an array area of ∼8cm×8cm (common DSSSD wafer design and therefore common segementation).

1.3 Required Capabilities

- Selectable Gain
  high ∼20MeV Full Scale Range (FSR) **OR** intermediate ∼1GeV FSR

  AND

  low ∼20GeV FSR (via separate overload recovery signal processing)
  energy measurement of implantation and decay events

- Selectable threshold $< 0.25 - 10\%$ FSR Minimum threshold <50keV @ high gain
  $\Rightarrow$ rms noise <5keV assuming threshold = 5σ
  observe and measure low energy betas, beta detection efficiency

- Integral $< 0.1\%$? and differential non-linearity $< 2\%$? for $> 95\%$ FSR
  spectrum analysis, calibration, threshold determination

- Autonomous overload detection and recovery $\sim \mu$s
  observe and measure fast implantation-decay correlations

- Nominal signal processing time $< 10\mu$s
  observe and measure fast decay-decay correlations

- Receive(transmit) time-stamp data
  correlate events with data from DAQs of other detector sub-systems (gamma and neutron detector arrays, upstream tracking detectors)

- Timing trigger for coincidences with other detector systems
  time resolution < BUTIS clock period (5ns)
  minimise random correlations, DAQ rate management, neutron ToF

1.4 Timescale

- EPSRC grant submission: January 2006
- EPSRC physics prioritisation panel: April 2006
- Project commencement: 1 August 2006
- Project prototype/commissioning: 2009/10
- Experimental programme commencement: 2010/11

2 Double Sided Silicon Strip Detector (DSSSD)

2.1 DSSSD Wafer

- DC design
- Common biasing to p^+n junction and n^+n ohmic strips via integrated polysilicon resistors $(15 \pm 5)\mathrm{M}\Omega$
- Detector thickness 1000μm
- Wafer area 8cm $\times$ 8cm ($6''$ wafer technology) or 8cm $\times$ 4cm ($4''$ wafer technology)
- 128×128 strips (8cm $\times$ 8cm) or 128×64 strips (8cm $\times$ 4cm)
- Strip pitch 625μm
- Inter-strip distance 50μm (consistent with obtaining $> 10^7\mathrm{M}\Omega$ resistance between n^+n ohmic strips)
  $\Rightarrow\sim 85\%$ of detector area is active
- Multiple guard rings for both p^+n junction and n^+n ohmic sides of the wafer
- Dead space (passivation, guard rings, common bias line and polysilicon bias resistors) surrounding active area ≤ 1.5mm
- Operating bias ≤ 200V
- Typical wafer leakage current $1-5\mathrm{nA/cm}^2/100\mu$m (20°C) at operating bias $\Rightarrow 0.64-3.2\mu$A for 8cm $\times$ 8cm area and 1000μm thickness
- Maximum (8cm $\times$ 8cm) wafer leakage current $< 5\mu$A (20°C) at operating bias
- Maximum strip leakage current $<$ 100nA (20°C) at operating bias
- 100% of strips functional to above specification

Operating bias is defined as the voltage required to obtain maximum charge collection and equivalent resolution for p^+n junction *and* n^+n ohmic strips for α-particles, whether incident on the junction or ohmic strips.

2.2 DSSSD Package

- Two package types: (i) 24cm × 8cm using (3 off 8cm × 8cm or 6 off 4cm × 8cm wafers) with series bonded n^+n strips, (ii) 8cm × 8cm using (1 off 8cm × 8cm or 2 off 4cm × 8cm wafers) with series bonded n^+n strips
- FR4 transmission PCB mounting
  thickness? ribs? additional stiffener? what material?
- Flexible Kapton PCB cabling directly bonded to PCB
- Tri-plate (ground/signal/ground planes) flexible Kapton PCB
  construction, plate separation, track width and pitch to be defined
- Flexible Kapton PCB connector type?
  minimum 128 electrical connections, length < 80mm
- Flexible Kapton PCB length ∼20cm
- PCB design to permit (i) use at any position in DSSSD stack, (ii) use at 0° or 180° with respect to an axis normal to the surface of the detector and other DSSSD planes in the stack
- PCB design to include thermocouple connection point
  could the thermocouple signals be routed via the Kapton PCB?
- PCB dimensions ∼ 26cm × 10cm ×2 − 3mm, ∼ 10cm × 10cm ×2 − 3mm,

2.3 Planned DSSSD Procurement

- 1 off prototype 24cm × 8cm detector
- 1 off prototype 8cm × 8cm detector
- 9 off production 24cm × 8cm detectors
- 9 off production 8cm × 8cm detectors

2.4 Intrinsic Resolution Limits of Silicon Detectors

The term intrinsic detector resolution refers to the response of a detector to a mono-energetic source of radiation and assumes that we can neglect the effects of dead layer, recombination, trapping and incomplete charge collection.

For β-particles we assume that the energy resolution will be equivalent to the electronic noise of the instrumentation. For protons and α-particles we assume that the energy resolution will be the quadratic sum of the statistics of the ionisation process, the effects of nuclear collisions at the end of the particle track and the electronic noise. Statistics: for 1MeV protons and 5MeV α-particles the contributions are 1.5keV FWHM and 3.4keV FWHM respectively. Collisions: for protons and α-particles the contributions are 0.7keV FWHM and 6.3keV FWHM respectively. For 1MeV protons and 5MeV α-particles the quadratic sums of the statistical and collisional contributions are 2.3keV FWHM and 7.2keV FWHM respectively. Unless the electronic noise is significantly lower than 12keV FWHM (1400e^- rms), the intrinsic detector resolution will be dominated by the electronic noise. If we assume (i) a resolution of 12keV FWHM, (ii) that data from discrete (Gaussian) peaks should be spread over 4 channels FWHM (for accurate centroid determination) and (iii)that the high gain range corresponds to 20MeV FSR then this implies that we need 13-bit ADCs. If the resolution is better then we will need 14-bit ADCs.

For heavy-ions ($A \geq 12$) the intrinsic energy resolution will be completely dominated by the effects of nuclear collisions at the end of the particle track and charge collection effects arising from the high density charge deposition. Lindhard and Neilson (Phys. Lett. 2 (1962) 209) estimate the contribution from nuclear collisions as

$$\Delta E_{\text{coll}}(\text{keV FWHM}) = 0.7 Z^{\frac{1}{2}} A^{\frac{4}{3}} \tag{1}$$

which ranges in value from ∼0.8MeV (^{58}Ni) to ∼10MeV (^{238}U).

2.5 Implantation Event Characteristics

The maximum energy loss of heavy-ions in 1mm of silicon (normal incidence):

Ion	ΔE_{max} (GeV)
^{58}Ni	3
^{120}Sn	7
^{238}U	17

The maximum energy that can be deposited in 1mm of silicon at, or near, normal incidence is therefore ≤20GeV which establishes the FSR requirement for the high-energy signal processing instrumentation.

Range of heavy-ions in silicon as a function of incident energy (normal incidence):

	Range (mm)			
Ion	50MeV/u	100MeV/u	200MeV/u	300MeV/u
^{58}Ni	1.0	3.3	11.8	20.9
^{120}Sn	0.8	2.3	7.1	13.7
^{238}U	0.6	1.7	4.7	8.9

Calculations performed using SRIM-2003 (http://srim.org). To implant ions at a distance of $3-5$mm into the DSSSD stack requires energies of $\sim 100-200$MeV/u.

Multi-GeV implants are expected to result in data from a cluster of strips for each DSSSD plane traversed by the ion. It is expected that ∼5 adjacent p^+n junction and ∼5 adjacent n^+n ohmic strips per DSSSD plane will produce data per event with the majority of the energy to be found at the cluster centre.

The energy and spatial distribution for the incoming implantation ions will be determined by the properties of the SuperFRS, low-energy branch (LEB) and any degraders, tracking detectors, AIDA entrance window etc. We assume that ions of a given A/q will be implanted across the DSSSD planes with a Gaussian transverse profile ($\sigma_x = \sigma_y \sim 1$cm) and a depth distribution ($\sigma_z \sim 1-2$mm). We assume implantation rates across the 24cm × 8cm DSSSD plane of ∼ 10kHz, with peak rates for ions with a given $A/q \sim 1$kHz. If we wish to observe lifetimes ∼s then this implies a segmentation of ~ 0.5mm × 0.5mm.

The observables of interest are:

- position/track of implant
  p^+n and n^+n strip numbers
- absolute energy of implant
  to $\sim 0.1\%$ precision
- implant time
  for time correlation with respect to (i) subsequent charged-particle decay events and (ii) isomeric decays detected by other detector arrays, precision (per event) 5ns
- time of implant
  by prompt trigger, precision < 5ns?

2.6 Decay Event Characteristics

We assume that the silicon detector responds linearly to deposited energy. The energy calibration for electrons and protons will differ from the α-particle calibration ($\sim 1-2\%$) due to the pulse height defect.

Typical decay event for protons (energy $0.5-2$MeV, range $7-50\mu$m) and α-particles (energy $3-12$MeV, range $15-100\mu$m) will consist of one p^+n junction strip and one n^+n ohmic strip from one DSSSD plane. A fraction of events (inter-strip area:total area) will occur between strips and these events will typically be 1 or 2 adjacent p^+n junction

strip(s) and 1 or 2 adjacent n^+n ohmic strip(s). In addition, for those decays due to implants close ($< 100\mu$m) to the surfaces of the DSSSDs it is possible for the decay to have sufficient energy to escape one DSSSD plane and be stopped in another. These events would therefore consist of data from two DSSSD planes with the event structure for each DSSSD plane as described above.

β-particles of interest will have energies in the range from ∼tens of keV to > 10MeV (range >25mm) - a large fraction of the β-particles of interest will not be stopped in one DSSSD plane. In addition, there is a significant probability that the β-particles will be scattered by the silicon. Events can therefore consist of data from multiple adjacent strips and DSSSD planes. There will be inter-strip events as described above.

The observables of interest are:

- position of decay
  p^+n and n^+n strip numbers
- absolute energy of charged-particle decay
  centroid of energy distribution of multiple decays to $\ll$ 1LSB
- absolute energy of threshold
  β detection efficiency, to 1LSB
- decay time
  for time correlation with respect to previous implantation events or charged-particle decays, precision (per event) 5ns
- time of decay
  by prompt trigger for time of flight (ToF) measurements, precision < 5ns

2.7 Radiation Damage

2.7.1 Operational Lifetime

To be defined.

2.7.2 Leakage current

The MSL type BB/5 DSSSD (area 32mm × 32mm, thickness ∼ 70μm) is used for implantation decay experiments using the Fragment Mass Analyser (FMA) at the Argonne National Laboratory. These detectors continue to provide useful data with leakage currents $\leq 5\mu$A at $\sim -10°$C. Scaling by area and thickness to the AIDA DSSSD we could expect a leakage current of $\sim 450\mu$A per 8cm × 8cm wafer or $\sim 3\mu$A per strip at $\sim 0°$C. This per strip leakage current would correspond to ∼50keV FWHM of noise for a shaping time $\tau = 1\mu$s: the noise would vary as $\sqrt{\tau}$ (see Appendix A). This might be sufficient for some measurements of α and proton decays but it would compromise low threshold detection of β-particles as the threshold would need to be increased to ∼110keV (5σ).

The above considerations indicate that it would be advantageous to cool the DSSSDs to a temperature significantly below 0°C. Because the silicon wafers are attached to the detector PCB using an electrically conductive epoxy the lower temperature limit is ~ -20°C. The DSSSDs and their mounting will need to be designed to ensure good thermal contact to achieve and maintain the temperatures required. Thermocouples to measure the temperature of the mounting and DSSSD PCB temperature will also be required.

Caveats The MSL type BB/5 is used with $40-80$MeV $A = 100-200$ ions which have a range significantly less than the thickness of the silicon wafer - damage is localised in depth (whereas for AIDA DSSSDs it will be more uniformly distributed through the wafer thickness) and therefore the scaling probably underestimates the leakage current of the AIDA detector. The MSL type BB/5 detector bias is usually set at $\times 3-5$ the depletion voltage - this is significantly higher than we will be able to achieve with the AIDA DSSSD, therefore the scaling probably overestimates the leakage current of the AIDA detector. This might also indicate that we will not be able to achieve equivalent charge collection and therefore resolution with the lower electric field of the 1000μm AIDA DSSSDs and therefore not be able to operate at equivalent levels of radiation damage.

2.7.3 Mitigation strategies

- Use number of detector layers appropriate to range of implanted ions
- Rotate detector layers - distribute radiation dose
- Detector cooling - leakage current reduction, improved charge collection
- Increased detector bias - improved charge collection
- Instrumentation physically separated from DSSSDs and protected by heavy-metal shield

3 Application Specific Integrated Circuit (ASIC)

A schematic diagram of ASIC functionality is shown in figure 2.

3.1 Low-energy channel ($0-20$MeV)

3.1.1 Preamplifier

- Differential input, with adjustable operating point, for optimum performance for both polarities of charge;
- Feedback capacitor $\sim$ 1pF, with feedback stabilisation circuit (equivalent to a high-value resistor);

- Input referred noise 1400e$^-$ rms = 5keV(Si) rms, preferably lower;
- Adjustable operating point, for optimum performance with both positive and negative charge;
- Integral non-linearity $< 0.1\%$.

3.1.2 Shaper

- Variable shaping time ($\sim 0.5 - 5\mu$s), to minimise ballistic deficit;
  Risetime variations $< 0.05\tau$ to maintain ballistic deficit effects $< 0.1\%$ assuming $CR - RC$ shaping (K.Hatch, IEEE Trans. Nucl. Sci. NS15 (1968) 303).
- $\sim$ 1V range of output voltage;
- Integral non-linearity $< 0.1\%$.

3.1.3 Slow amplifier/comparator

- Bandwidths matched to shaper (to avoid adding noise);
- Amplifier with $\times$10 gain before comparator, to minimise effect of offset variations;
- Usable threshold range 50keV$-$2MeV ($0.25 - 10\%$ full-scale);
- Low end of threshold determined by offsets and noise - desirable to achieve 25keV;

3.1.4 Fast comparator

- Signal taken straight from pre-amp output, without band-limiting;
- Timing resolution <5ns, but with high noise (unsuitable for operation with low thresholds);
- Direct connection to control logic, to provide high-speed digital timing pulse;
  should be OR'd with slow comparator output

3.1.5 Peak-hold

- Rectifying current mirror architecture (to maintain output linearity)
- Low-leakage design, for good stability
  Assume 1V FSR, 14-bit ADC $\Rightarrow$ 1LSB = 61μV
  Droop $\ll$1LSB, 0.1LSB say $\Rightarrow$ droop $< 6\mu$V per readout cycle ($< 10\mu$s)

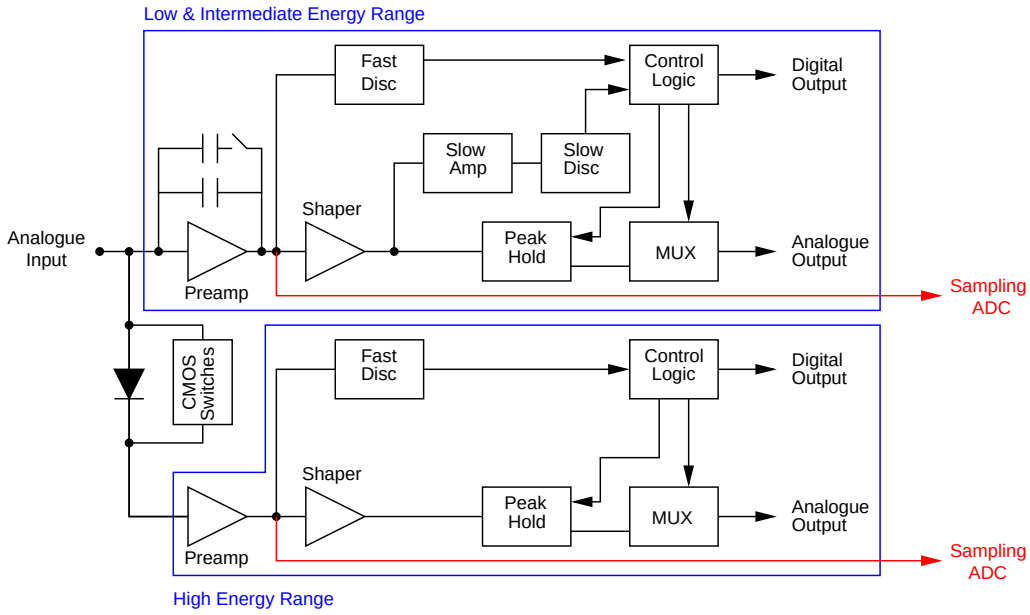

Figure 2: Schematic diagram of the functionality of one ASIC channel

3.2 Intermediate energy channel $(0 - 1\mathbf{GeV})$

Preamplifier feedback $\sim$ 50pF. Scale noise, minimum threshold etc. from low energy $(0 - 20\text{MeV})$ specification.

3.3 High-energy channel $(0 - 20\mathbf{GeV})$

3.3.1 Pre-amp

- Similar to low-energy design, but optimised for $\sim$ 1nF feedback capacitor;
- Large current flow in amplifier output transistors (needs to exceed the peak current from the detector);
- Input referred noise $\sim 5 \times 10^6 \text{e}^-\text{rms}$, $\sim$20MeV (Si) rms.

3.3.2 Diode and CMOS switches

- Diode to connect high-energy amplifier to detector when low-energy channel saturates;
- CMOS switches connected in parallel with diode, after saturation has been detected;
- Switches to be reset, after the charge has been integrated by the high-energy amplifier.

Fast shaper, Peak-hold, Fast comparator: As before. Minimum threshold $< 2\%$ FSR. Fast shaper noise not constrained by shaping time. Slow amplifier/comparator: Omitted (noise performance is not so critical for the higher energies)

3.4 Control Logic

This block manages the link between the peak-hold circuits and the multiplexers. The stored voltages from the peak-holds are accessed in sequence, whenever over-threshold conditions are detected. The logic will also handle the reset of analogue circuitry, including the CMOS switches. The intention is to minimise the recovery time from high-energy pulses - the target is a few microseconds.

The multiplexers will provide analogue voltages over a 1V range for the external ADC. It will be possible to provide a reference voltage, so the ADC can operate in fully differential mode. The reference voltage will match any drift of the active multiplexer outputs, for example variations with temperature or power supply.

3.5 Overload Recovery

The effect of the 20GeV implant in the detector is to cause a rapid change of voltage on the amplifier inputs for the channel. The low-energy amplifier goes into saturation, and the signal charge is immediately coupled to the high-energy amplifier. The coupling is initially via a forward-biased diode, but the connection is maintained by CMOS switches until the high-energy amplifier has completed the integration of the charge.

The next step is to disconnect the high-energy amplifier and to reset the low-energy amplifier. This will speed up the recovery from the implant event, giving sensitivity to decay products within a few microseconds. The reset could be implemented by switched feedback components in the amplifier, and probably in the low-energy shaper as well. It will not be necessary to wait many shaper time-constants before the signal baseline is recovered.

It is important for the reset process to be clean - it must not create spurious charge injection which might trigger the low-energy comparators. This could be achieved by a time-sequence of reset pulses which allows the amplifier and shaper to recover fully before the comparator becomes active.

3.6 Package

ASIC channel pitch to be compatible with strip pitch of DSSSD ($\sim 625\mu$m). 8 (c. 5mm $\times$ 6mm) or 16 (c. 10mm $\times$ 6mm) channels per ASIC depending on the expected defect density of the processed wafers and the NRE/production costs of the MPW run.

3.7 ASIC Production Requirements

Each 24cm×8cm DSSSD requires 512 channels of instrumentation (384 p^+n strips, 128 n^+n strips). Each 8cm×8cm DSSSD requires 256 channels of instrumentation (128 p^+n strips, 128 n^+n strips).

To evaluate the prototype ASIC with a fully instrumented 8cm×8cm DSSSD would require a minimum of 32 (size c. 5mm × 6mm) or 16 (size c. 10mm × 6mm) operational dies. To evaluate the prototype ASIC with a fully instrumented 24cm×8cm DSSSD would require a minimum of 64 (size c. 5mm × 6mm) or 32 (size c. 10mm × 6mm) operational dies.

For the production ASIC, ten DSSSDs will require 5120 channels of instrumentation which implies a minimum of 640 (size c. 5mm × 6mm) or 320 (size c. 10mm × 6mm) operational dies.

4 Front End Electronics (FEE)

A diagram illustrating the FEE card concept and functionality is shown in figures 3 and 4. Each FEE card will support 128 channels of instrumentation.

Preamplifier differential inputs - p^+n/n^+n and reference voltage (reference voltage varied depending what type of strip is connected to other pin) means that FEE cards can be used for either p^+n junction or n^+n ohmic strips.

4.1 ADC

Typical ADC - Analog Devices AD976A 200kSPS, 16-bit ADC. Power dissipation $<$ 100mW.

For the prototype ASIC design, it will be possible to connect a sampling ADC directly to the output of the charge sensitive preamplifier to evaluate the use of digital signal processing instead of the more conventional shaper, peak detect & hold and ADC configuration. Potential advantages include the ability to measure decay-decay correlations to ∼100ns, pulse shape analysis, ballistic deficit corrections etc. Example ADC - Analog Devices AD9222-50 Octal, 50MSPS, 12-bit ADC. Power dissipation $<$ 95mW per channel. SOIC package 64-pin LFCSP_VQ size ∼9mm × 8.9mm which would require devices on both sides of the FEE PCB to approach the necessary channel pitch necessary to provide an ADC per channel.

4.2 FPGA

Xilinx Virtex 4FX for control, data processing, event building. With integrated ethernet port.

4.3 Other

- Power supply regulators and filtering.
- ROM for FPGA configuration data.
- Fibre-optic ethernet driver.
- Estimated FEE PCB size 80mm × 220mm.
- Power dissipation 25W per FEE PCB.
- Each FEE PCB to have a unique, electronically readable, identification number. This will enable (i) the use of *ab initio* calibrations/parameters/corrections determined during laboratory bench acceptance tests, (ii) the monitoring of operational parameters for effects such as radiation damage.

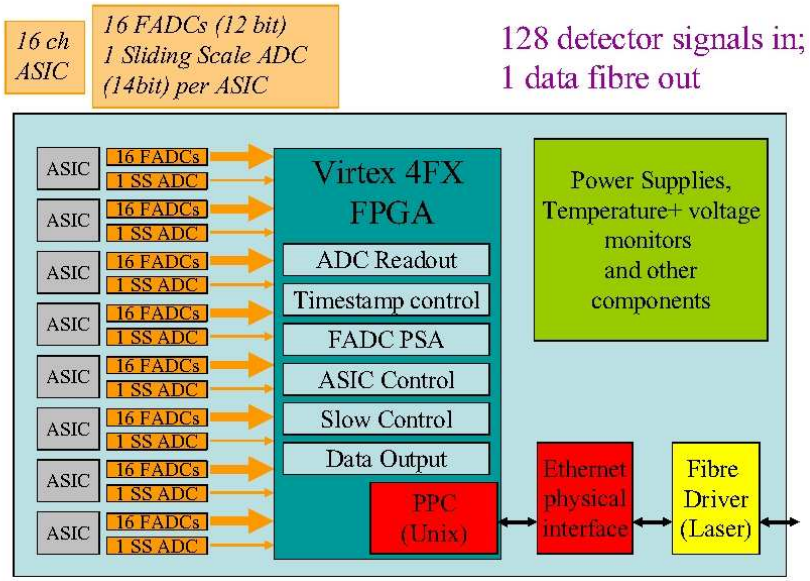

Figure 3: Front End Electronics (FEE) concept

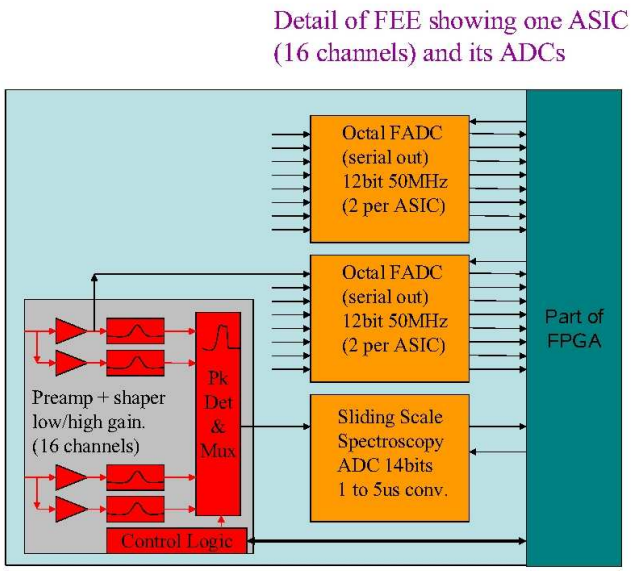

Figure 4: Front End Electronics (FEE) concept showing detail for one ASIC

4.4 FEE Production Requirements

Each 24cm×8cm DSSSD requires 512 channels of instrumentation (384 p^+n strips, 128 n^+n strips). Each 8cm×8cm DSSSD requires 256 channels of instrumentation (128 p^+n strips, 128 n^+n strips). Each FEE card provides 128 channels of instrumentation.

To evaluate the prototype ASIC with a fully instrumented 8cm×8cm DSSSD would require a minimum of 2 FEE cards. To evaluate the prototype ASIC with a fully instrumented 24cm×8cm DSSSD would require a minimum of 4 FEE cards.

For production, ten 24cm×8cm DSSSDs will require a minimum of 40 FEE cards.

5 Data Acquisition (DAQ)

A diagram illustrating the DAQ concept and functionality is shown in figure 5

- Data acqusition architecture compatible with NUSTAR DAQ standard.
- BUTIS link to AIDA via fibre-optic connection.

6 Software

6.1 Data Format

Standard NUSTAR format - to be defined.

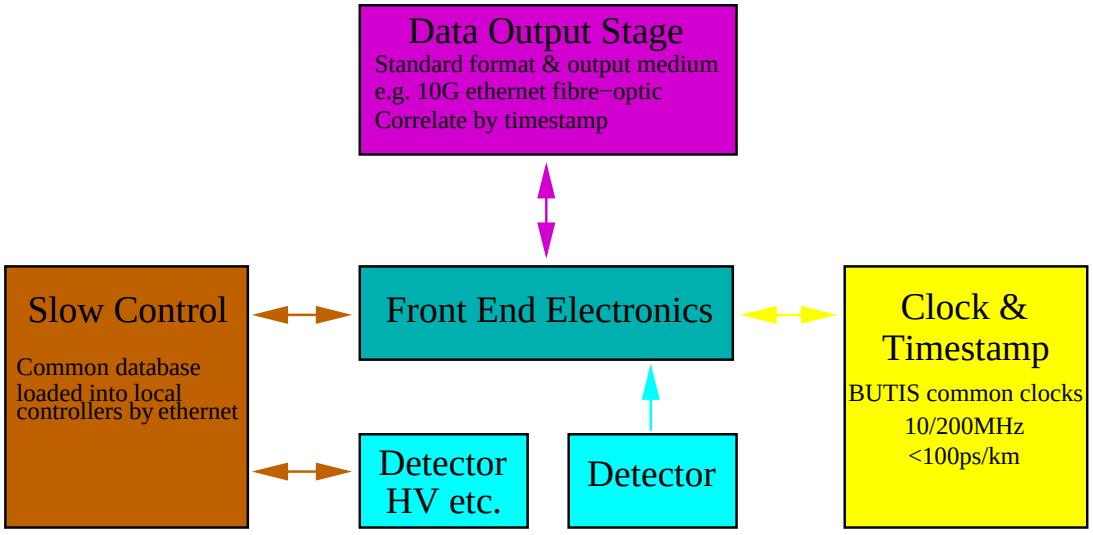

Figure 5: NUSTAR Data Acquisition (DAQ) concept

6.2 Slow Control Interface

- Web-based interface (SOAP?)
- Control and parameter history to be available as strip chart (cf. EPICS at TRIUMF).

6.2.1 ASIC Control

Controls required:

- ASIC gain, shaping time, threshold(s) per channel, power supplies ...
- ...

Parameters to be included in data stream with a timestamp on a periodic (10s−1min?) basis

- ASIC gain, shaping time, threshold(s) per channel, power supplies ...
- ...

6.2.2 Subsystems Control

Controls required:

- AIDA DSSSD bias, voltage/current trip, voltage set point, ramp rate
- Coolant recirculator (on/off/set point)

- Vacuum pump (on/off)
- ...

Parameters to be included in data stream with a timestamp on a periodic (10s−1min?) basis

- Accelerator parameters of interest
- SuperFRS parameters of interest
- AIDA DSSSD bias, leakage current, status (on/off/over-voltage/over-current/fail/trip)
- Coolant recirculator status, operating temperature
- AIDA DSSSD mounting block, DSSSD PCB temperatures
- AIDA DSSSD enclosure vacuum pressure
- FEE PCB ID numbers
- ...

7 Systems Integration

7.1 AC Coupling

- For full-scale response (20MeV=1V FSR) in one high gain channel, we require $<$ 0.25% FSR ($<$ 2.2fC) response in adjacent channels. Coupling capacitance between adjacent channels is (see appendix)

$$24\text{cm} \times 1.6\text{pF/cm} + 20\text{pF} = 58\text{pF} \tag{2}$$

So strip voltage fluctuation is given by

$$\delta V \leq \frac{Q}{C} \leq \frac{2.2\text{fC}}{58\text{pF}} \leq 38\mu\text{V} \tag{3}$$

To achieve this voltage fluctuation the coupling capacitance required is

$$C_c \geq \frac{\text{FSR}}{\delta V} C_f \geq \frac{1\text{V}}{38\mu\text{V}} 1\text{pF} \geq 26\text{nF} \tag{4}$$

The nearest decade value is 22nF.

- Assuming a 22nF coupling capacitor, a full-scale response for an intermediate gain channel (1GeV = 1V FSR, $C_f = 50$pF) will be accompanied by a voltage fluctuation of
$$\delta V = \frac{1\text{V}}{440} = 2.3\text{mV} \tag{5}$$
on the detector strip. This will inject charge
$$\delta Q = \delta V \times 58\text{pF} = 0.13\text{pC} \tag{6}$$
which corresponds to 0.3% crosstalk.

- Assuming a 22nF coupling capacitor, a full-scale response for an intermediate gain channel (20GeV = 1V FSR, $C_f = 1$nF) will be accompanied by a voltage fluctuation of
$$\delta V = \frac{1\text{V}}{22} = 45\text{mV} \tag{7}$$
on the detector strip. This will inject charge
$$\delta Q = \delta V \times 58\text{pF} = 2.6\text{pC} \tag{8}$$
which corresponds to 3% crosstalk.

- Require 22nF/200V+ coupling capacitor per channel
Required rating exceeds that available for detector integrated coupling capacitors (typically 100pF/100V).

- Ceramic, low $1/f$ noise

- Locate on DSSSD PCB, FEE PCB or intermediate position dependent on cost, size and channel pitch.

- Options?

7.2 Detector Bias

- Voltage $\leq$ 500V, current $\leq$ 3mA per DSSSD plane

- Polarity ?

- Bias configuration? (see figure 6)

- Noise $\leq 1.2\mu$V rms (bandwidth defined by instrumentation)
Should be negligible contributor to total noise. Assume total noise of 12keV FWHM $\Rightarrow$ noise contribution $\leq$ 3keV FWHM, $\leq 350\text{e}^-$ rms
$$\delta V \leq \frac{Q}{C_D} \leq \frac{350 \times 1.6021 \times 10^{-19}}{46 \times 10^{-12}} \leq 1.2\mu\text{V rms} \tag{9}$$

- Detector power dissipation?

- ...

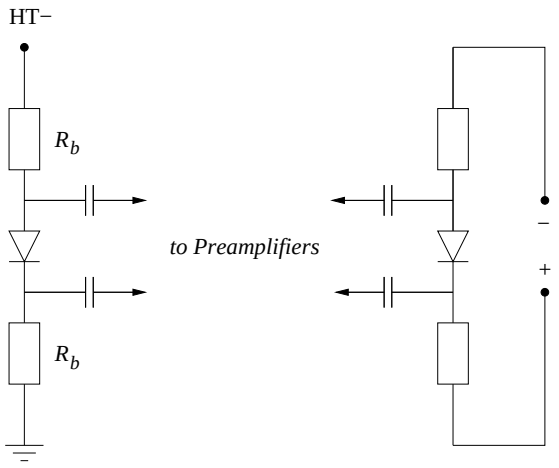

Figure 6: Detector bias options

7.3 Power Supplies

To be defined.

7.4 Test and Calibration

General functional test, measurement of dc offsets (to $\ll$1LSB) and measurement of integral non-linearity by charge injection to test inputs with precision pulser.

General functional test and precision calibration (to $\ll$1LSB) by external radioactive (conversion electron, alpha) sources. Calibration using known decays possible but will require implantation of parent nuclei into the same region of the detector array as the implantations of interest to the experiment. Because the flexible Kapton cabling will surround the DSSSD stack it will not be possible to insert a source to illuminate the detectors from the side of the stack: in any event this would be a poor geometry, particularly for α-particles. A better option might be to insert spacers between DSSSD layers (they might also act as stiffeners for the DSSSD PCBs). The internal surface of the spacer would be a knife edge - a low level radioactive source could be electro-deposited on the knife edge surfaces. This would provide both a better geometry for detection, illumination of only the edges of the silicon wafers and calibration data to every channel. Radioanuclide options might include ^{207}Bi or a mixed alpha source. Alternatively, the edges of the silicon wafers might be 'contaminated' with a suitable radionuclide, e.g. ^{227}Ac.

Radioactive sources typically provide a few discrete peaks (conversion electrons $\sim 500-1000$keV, α-particles $\sim 3-8$MeV. Commonly, the experimental data will lie outside energy range calibrated and it will be necessary to use extrapolation to determine the energy. The precision that can be achieved is obviously dependent on the linearity of the instrumentation - it will be necessary to use the response function determined from the pulser data. In particular, peak detect circuits usually exhibit increasing non-linearity in

the lower 5% of their operating range - it is important that any non-linear effects should exhibit a continuous trend. This will enable requirements for the precision of the absolute energy measurement of decays and threshold to met from minimum threshold to FSR.

7.5 Detector Enclosure

Internal volume of DSSSD enclosure maintained at roughing pressure ($< 10^{-3}$mbar) by oil-free (scroll) pump.

7.6 Detector Cooling

Recirculating coolant (ethanol?) to DSSSD support frame. DSSSD planes in good thermal contact with support frame.

7.7 Instrumentation Cooling

Forced air cooling.

7.8 Cabling and Connectors

Fibre-optic for data and control. Others (e.g. local power) to be defined.

7.9 Screening and Grounding

AIDA system will be electrically isolated from *all* other DESPEC and SuperFRS detector systems and other equipment/mechanics.

Detector enclosure to provide EMI/RFI screening. Detectors, signal cables and feedthroughs to be electrically isolated from the enclosure and mounting to avoid ground loop problems.

Ground to single point, clean experimental mains power distribution point.

8 Mechanical

8.1 Design Control

The mechanical design of AIDA will be a controlled document held by CCLRC Daresbury Laboratory. This document will define the position of, and space required by, AIDA. It will therefore define the space *not available* to other DESPEC and SuperFRS systems. The mechanical design document will be made available to the DESPEC collaboration via the web (URL to be provided).

8.2 Installation

The AIDA system will be installed on rails to permit routine transfer to/from the in-beam position.

8.3 Materials

Detector enclosure material types and thicknesses selected to minimise γ ray attenuation and neutron absorption. Thin aluminium (for vacuum) with external woven carbon fibre (for additional strength)?

8.4 Design Concepts

Figures 7 to 12 illustrate current design concepts. The diagrams are colour coded as follows:

Dark Grey Heavy metal radiation shield to protect instrumentation.

Light Brown Instrumentation enclosures.

Silver Support frame

Green/Blue Detectors and enclosure.

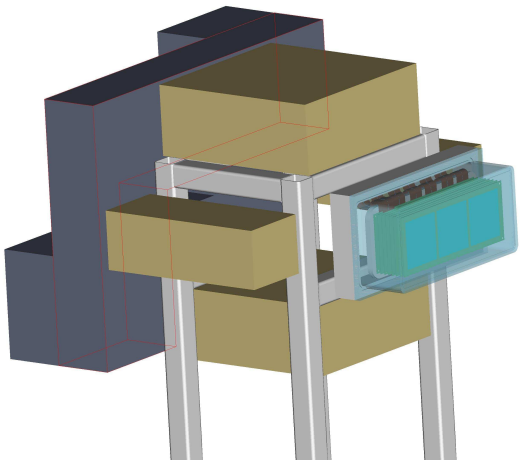

Figure 7: AIDA front

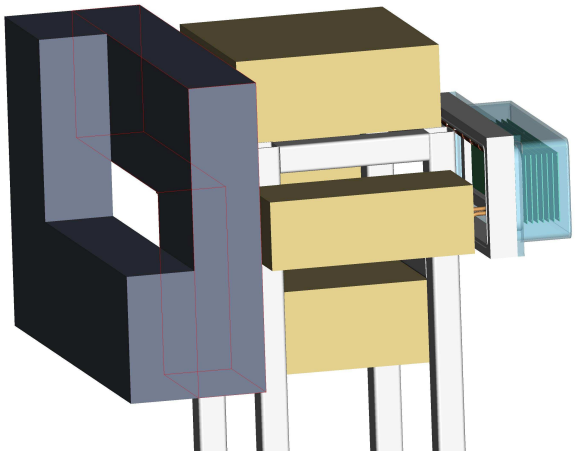

Figure 8: AIDA back

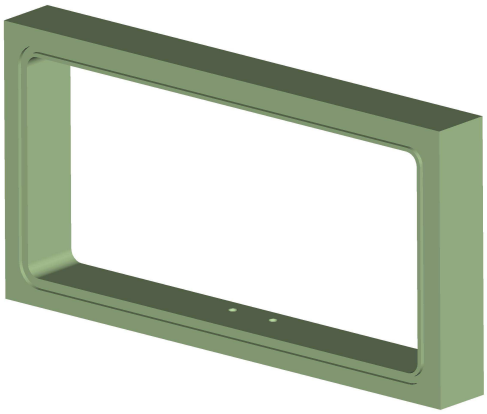

Figure 9: AIDA support frame

A Noise Analysis

This section discusses a *representative* noise analysis for the front end (in this context - detector and preamplifier). It is designed to illustrate the relative importance of the various contributors to the the total noise - actual design and optimisation strategies are discussed elsewhere (see S.L. Thomas, presentations to AIDA collaboration meetings).

Sources of parallel noise are:

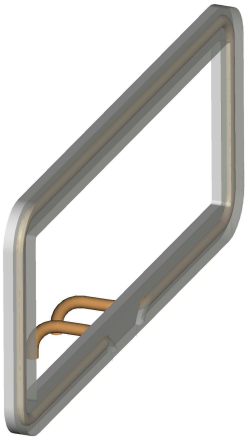

Figure 10: AIDA cooling frame

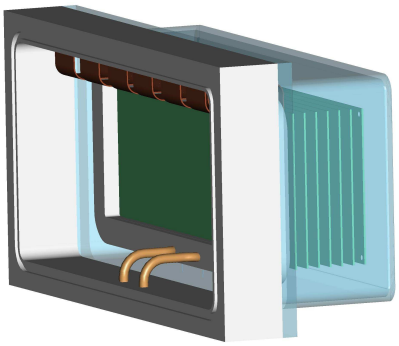

Figure 11: AIDA detector chamber

- detector leakage current I_D
- input FET gate leakage current I_g
- detector bias resistor R_b
- preamplifier feedback resistor R_f
- ...

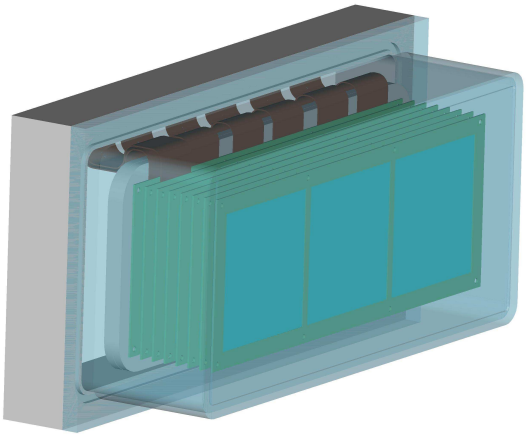

Figure 12: AIDA detector chamber front

The total parallel noise is given by the expression

$$i_n^2 = 2qI_D + 2qI_g + \frac{4kT}{R_b} + \frac{4kT}{R_f} + \dots \tag{10}$$

where k is Boltzman's constant, T the absolute temperature and q the charge of an electron. The input FET gate leakage current is typically sub-nA. By comparison, the expected detector leakage currents are in the range $1 - 1000$nA per strip. The MSL quoted polysilicon bias resistors value is (15 ± 5)MΩ. The feedback of the preamplifier is expected to be stabilised by a very high value resistance (1GΩ, say) in the form of a transistor. For parallel noise, the only appreciable terms are therefore the contributions from the detector leakage current (i.e. we assume $I_D \gg I_g$) and the detector bias resistor (i.e. we assume $R_f \gg R_b$).
Sources of series noise are:

- input FET with transconductance g_m
- ...

The total series noise is given by the expression

$$v_n^2 = \frac{2}{3}\frac{4kT}{g_m} + \dots \tag{11}$$

Assuming $CR - RC$ shaping with shaping time $\tau = CR = RC$ then the silicon equivalent parallel and series noise referred to the input can be calculated as follows

$$e_n = \frac{2.35 i_n e\epsilon}{q}\sqrt{\frac{\tau}{8}} = 5.16 \times 10^{13} i_n \sqrt{\tau} \text{ keV FWHM (Si)} \tag{12}$$

$$e_{ns} = \frac{2.35 v_n C e \epsilon}{q\sqrt{8\tau}} = 5.16 \times 10^7 v_n \frac{C}{\sqrt{\tau}} \text{ keV FWHM (Si)} \quad (13)$$

where $\epsilon = 3.66$eV (Si), $q = 1.6021 \times 10^{-19}$C, shaping time $\tau(\mu$s),input capacitance C (pF), parallel noise i_n (A/$\sqrt{\text{Hz}}$) and series noise v_n (V/$\sqrt{\text{Hz}}$).

The total input capacitance C is

$$C = C_D + C_{\text{Cable}} + C_{\text{FET}} + C_f \quad (14)$$

where C_D is the detector capacitance, C_{Cable} the capacitance of the cabling and connectors between the DSSSD and the preamplifier, C_{FET} the input FET shunt capacitance (estimated as $\sim$ 20pF) and C_f the preamplifier feedback capacitance ($\sim$ 1pF). Demaria *et al.*(NIM A447 (2000) 142) parameterise the capacitance of strip detectors with strip widths and pitches from $60 - 240\mu$m. For strip detectors of 320μm thickness they obtain the following expression for detector capacitance per unit strip length

$$C_{\text{int}} = 0.03 + 1.62\frac{(w + 20\mu\text{m})}{p} \quad (15)$$

$$C_{\text{back}} = 1.05 \quad (16)$$

$$C_D = C_{\text{int}} + C_{\text{back}} \quad (17)$$

where C_{int} is the interstrip capacitance (pF/cm), C_{back} the capacitance to the backplane (pF/cm), p the strip pitch (μm) and w the strip width (μm). For a detector of 1000μm thickness, strip pitch 625μm and strip width 575μm this expression becomes

$$C_D = 0.03 + 1.62\frac{(575 + 20\mu\text{m})}{625} + 1.05\frac{320}{1000} = 1.9\text{pF/cm} \quad (18)$$

Strip length varies from 8cm to 24cm. Minimum and maximum detector capacitances are therefore 15pF and 46pF. The capacitance of flexible kapton tri-plate cable is $\sim$1pF/cm (A. Deutsch *et al.*, IBM J. Res. Dev. 37 (1993) 22). If we assume a flexible Kapton PCB length of 20cm then the capacitance is $\sim$20pF. The total input capacitance C therefore varies from 56pF to 87pF.

Figure 13 shows the calculated noise for the minimum and maximum input capacitances and a range of strip leakage currents. The calculations assume:

- input FET transconductance 10mA/V
- bias resistor temperature 273K
- input FET and feedback resistor temperatures 313K
- noiseless shaper
- no $1/f$ noise

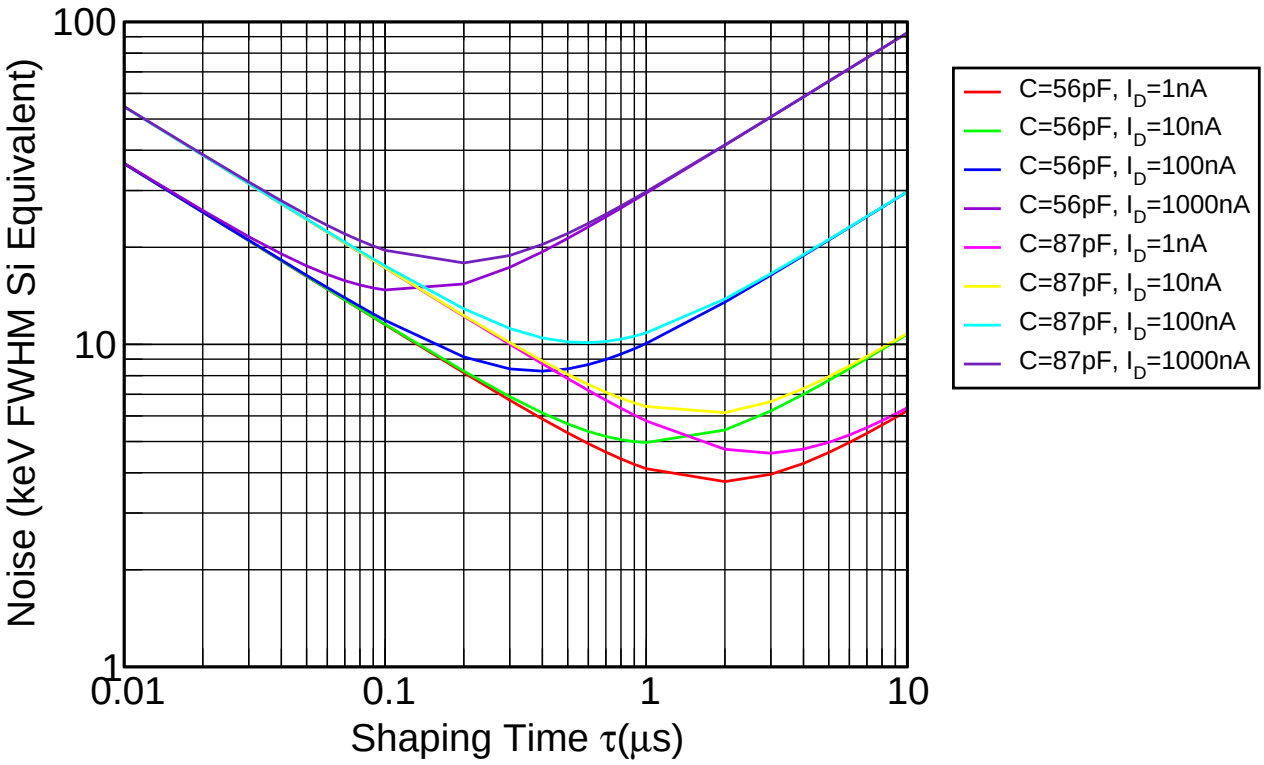

Figure 13: Detector and preamplifier noise (assuming $CR - RC$ shaping, g_m=10mA/V) for different input capacitances and detector leakage currents.

For a shaping time $\tau = CR = RC = 1\mu$s the various individual contributions to the total noise are:

- input FET transconductance (g_m = 10mA/V) 3.1 and 4.8keV FWHM for input capacitance C=56 and 87pF respectively
- detector leakage currents ($I_D = 1, 10, 100, 1000$nA) 0.92, 2.9, 9.2 and 29keV FWHM respectively
- detector bias resistor ($R_b = 15\text{M}\Omega$) 1.6keV FWHM

A.1 Detector Bias Resistor

The strip leakage current shot noise equals the thermal noise of the bias resistor when the voltage drop across the bias resistor is equivalent to

$$\Delta V = \frac{2kT}{q} = \frac{2 \times 1.38 \times 10^{-23} \times 273}{1.6 \times 10^{-19}} = 47\text{mV} \tag{19}$$

Provided the voltage drop across the bias resistor is greater than 47mV then the leakage current shot noise will exceed the thermal noise of the bias resistor. Micron Semiconductor Ltd. (MSL) quote typical leakage currents of 10nA per strip, (maximum 100nA per strip) at 'full depletion' and 20°C. Leakage current decreases by a factor of $\times 2$ per 8°C decrease in temperature so the typical per strip leakage current will decrease to $\sim$1.5nA at 0°C. To satisfy the above condition the bias resistor will need to be $\sim$30MΩ. Unfortunately, MSL cite poor tolerance control due to low doping levels for resistance values > 20MΩ. However, the leakage current will increase significantly during the operational lifetime of the detector due to radiation damage. The contribution of the 15MΩ bias resistor to the total noise appears to be relatively small in comparison to other noise sources.