Project Specification

Project Name: DESPEC AIDA

Version: 1.0

APPROVAL

	Name	Signature	Date
Project Manager	Stephen Thomas		
Customer/Sponsor	Tom Davinson		

DISTRIBUTION:

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1 DESCRIPTION

The objective of the DESPEC Advanced Implantation Detector Array (AIDA) project is to develop, commission and exploit a state of the art silicon detector array for decay spectroscopy experiments using the SuperFRS fragment separator at the FAIR accelerator facility based at GSI, Darmstadt, Germany. It is anticipated that AIDA will be operated in conjunction with other detection systems, such as gamma-ray and neutron detector arrays, which requires that AIDA should be very compact while still accepting all ions from the fragment separator.

To achieve these objectives AIDA will use large area double-sided silicon strip detector (DSSSD) and application specific integrated circuit (ASIC) technologies. AIDA will be used for implantation-decay experiments and perform spectroscopy quality measurements of charged particle decays with energies from tens of keV to MeV. The challenge is to achieve this within microseconds of multi-GeV exotic ion implants and with an instrumentation density to match the very high degree of detector segmentation required for the observation and characterisation of long-lived decays.

2 SCOPE

2.1 Includes

Detailed design, simulation, layout and preliminary testing of the AIDA IC (two iterations). Testing at RAL will be based on the IMS chip tester, with packaged devices mounted on a standard adapter board. The tests will aim to verify the basic functionality and yield of the ICs - it will not be possible to measure analogue performance with high accuracy.

2.2 Excludes

Detector design, data acquisition system, beam testing.

3 DELIVERABLES

Each 24cm x 8cm DSSSD requires 512 channels of instrumentation (384 p+n strips, 128 n+n strips). Each 8cm x 8cm DSSSD requires 256 channels of instrumentation (128 p+n strips, 128 n+n strips). To evaluate the prototype ASIC with a fully instrumented 8cm x 8cm DSSSD would require a minimum of 32 (size c. 5mm x 6mm) or 16 (size c. 10mm x 6mm) operational dies. To evaluate the prototype ASIC with a fully instrumented 24cm x 8cm DSSSD would require a minimum of 64 (size c. 5mm x 6mm) or 32 (size c. 10mm x 6mm) operational dies. For the production ASIC, ten DSSSDs will require 5120 channels of instrumentation which implies a minimum of 640 (size c. 5mm x 6 mm) or 320 (size c. 10mm x 6mm) operational dies.

4 CONSTRAINTS

4.1 Budget

Fabrication of prototype ASICs: £35250
ASIC verification and test environment: £20000
Fabrication of production ASICs: £47000

4.2 Schedule

See Workplan AIDA_Gantt1.mpp or AIDA_Gantt1.pdf

4.3 Performance

Low-energy channel (0-20MeV)

Pre-amp:
- Differential input, with adjustable operating point, for optimum performance for both polarities of charge;
- Feedback capacitor ~1pF, with feedback stabilisation circuit (equivalent to a high-value resistor);
- Input referred noise 1400 electrons rms = 5keV(Si) rms, preferably lower;
- Adjustable operating point, for optimum performance with both positive and negative charge;
- Integral non-linearity <0.1%.

Shaper:
- Switchable shaping time (~0.5us to 5us), to minimise ballistic deficit;
- ~1V range of output voltage;
- Integral non-linearity <0.1%.

Slow amplifier/comparator:
- Bandwidths matched to shaper (to avoid adding noise);
- Amplifier with x 10 gain before comparator, to minimise effect of offset variations;
- Usable threshold range 50keV-2MeV (0.25-10% full-scale);
- Low end of threshold determined by offsets and noise - desirable to achieve 25keV;

Fast comparator:
- Signal taken straight from pre-amp output, without band-limiting;
- Timing resolution <5ns, but with high noise (unsuitable for operation with low thresholds);
- Direct connection to control logic, to provide high-speed digital timing pulse;

Peak-hold:
- Rectifying current mirror architecture (to maintain output linearity)
- Low-leakage design, for good stability. Droop< 6μV per readout cycle (<10μs)
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Intermediate energy channel (0 - 1 GeV)

Preamplifier feedback ~50pF. Scale noise, minimum threshold etc. from low energy (0 - 20MeV) specification.

High-energy channel (0-20GeV)

Pre-amp:
- Similar to low-energy design, but optimised for ~1nF feedback capacitor;
- Large current flow in amplifier output transistors (needs to exceed the peak current from the detector);
- Input referred noise ~5e6 electrons rms, ~20MeV(Si) rms.

Diode and CMOS switches:
- Diode to connect high-energy amplifier to detector when low-energy channel saturates;
- CMOS switches connected in parallel with diode, after saturation has been detected;
- Switches to be reset, after the charge has been integrated by the high-energy amplifier.

Shaper, Peak-hold, Fast comparator: As before.

Slow amplifier/comparator: Omitted (noise performance is not so critical for the higher energies)

Control logic

This block manages the link between the peak-hold circuits and the multiplexers. The stored voltages from the peak-holds are accessed in sequence, whenever over-threshold conditions are detected. The logic will also handle the reset of analogue circuitry, including the CMOS switches. The intention is to minimise the recovery time from high-energy pulses - the target is a few microseconds.

The multiplexers will provide analogue voltages over a 1V range for the external ADC. It will be possible to provide a reference voltage, so the ADC can operate in fully differential mode. The reference voltage will match any drift of the active multiplexer outputs, for example variations with temperature or power supply.

Overload Recovery

The effect of the 20GeV implant in the detector is to cause a rapid change of voltage on the amplifier inputs for the channel. The low-energy amplifier goes into saturation, and the signal charge is immediately coupled to the high-energy amplifier. The coupling is initially via a forward-biased diode, but the connection is maintained by CMOS switches until the high-energy amplifier has completed the integration of the charge.

The next step is to disconnect the high-energy amplifier and to reset the low-energy amplifier. This will speed up the recovery from the implant event, giving sensitivity to decay products within a few microseconds. The reset could be implemented by switched feedback components in the amplifier, and probably in the low-energy shaper as well. It will not be necessary to wait many shaper time-constants before the signal baseline is recovered.

It is important for the reset process to be clean - it must not create spurious charge injection which might trigger the low-energy comparators. This could be achieved by a time-sequence of reset pulses which allows the amplifier and shaper to recover fully before the comparator becomes active.

Package

ASIC channel pitch to be compatible with strip pitch of DSSSD (~625μm). 8 (c. 5mm x 6mm) or 16 (c. 10mm x 6mm) channels per ASIC depending on the expected defect density of the processed wafers and the NRE/production costs of the MPW run.

4.4 Regulatory

5 IPR AND CONFIDENTIALITY

CCLRC Technology owns the design databases it has produced. Any production tools, eg masks or phototools, derived from these databases will be procured by CCLRC Technology. None of these items will be released unless the appropriate protective agreements are in place.

6 PROJECT MONITORING

The web-based monitoring system will be operated.