New results on silicon microstrip detectors of CMS tracker

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Abstract

Interstrip and backplane capacitances on silicon microstrip detectors with p^+ strip on n substrate of 320 μm thickness were measured for pitches between 60 and 240 μm and width over pitch ratios between 0.13 and 0.5. Parametrisations of capacitance w.r.t. pitch and width were compared with data. The detectors were measured before and after being irradiated to a fluence of 4×10^{14} protons/cm^2 of 24 GeV/c momentum. The effect of the crystal orientation of the silicon has been found to have a relevant influence on the surface radiation damage, favouring the choice of a $\langle 1\,0\,0 \rangle$ substrate. Working at high bias (up to 500 V in CMS) might be critical for the stability of detector, for a small width over pitch ratio. The influence of having a metal strip larger than the p^+ implant has been studied and found to enhance the stability. © 2000 Elsevier Science B.V. All rights reserved.

1. Introduction

At the LHC, bunch crossings will be separated in time by 25 ns and each bunch crossing will generate a large number of particles. Silicon microstrip detectors are fast enough to identify the bunch crossing, but they need a read-out electronics of comparable shaping time. This is beneficial in terms of shot noise from the leakage current; on the contrary the capacitive load which the strips on the detectors present to the electronics results in a significant or even dominant contribution to the noise. Therefore, it is crucial to understand the dependence of the strip capacitance on the different detector geometries and the effect on stability of the detector, in order to optimise the overall performances. Special attention has to be paid to the impact of the irradiation which the detectors will receive at the LHC. The impact of $\langle 1\,0\,0 \rangle$[1] silicon crystal orientation on the radiation surface damage has been studied, bearing in mind that in CMOS technology the $\langle 1\,0\,0 \rangle$ orientation is preferred to

$\langle 1\,1\,1 \rangle$ because it has less SiO_2 interface charges: these are also important for microstrip silicon detectors since they increase the interstrip capacitance. In high energy only $\langle 1\,1\,1 \rangle$ has been normally used and no detailed studies of the implications of this choice on surface radiation damages have been done so far.

As the strip pitches used in the CMS silicon tracker vary between 60 and 240 μm [1], these studies have been performed over this wide range of strip geometries.

2. Detectors and measurements

A special R&D detector layout has been developed. On one detector wafer of 6.3×6.3 cm^2 surface, 12 sub-detector regions are fitted which have 32 strips each and which are separated from each other by n^+ implants. Four different pitches are implemented (60, 80, 120 and 240 μm) such that for each pitch there are three sub-detectors. This allows to vary a second parameter, in this case the implant width. The detectors were fabricated by Hamamatsu Photonics. Three different batches were produced, called GEOM1, GEOM2 AC and GEOM2 DC; the first two have AC coupling to metal lines while the latter is DC coupled. Each batch was split in detector with high-resistivity

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[1] In $\langle 1\,0\,0 \rangle$ substrates the wafer is cut along the $\langle 1\,0\,0 \rangle$ plane, i.e. along one face of the cubic cell; in $\langle 1\,1\,1 \rangle$ it is cut along the $\langle 1\,1\,1 \rangle$ plane, i.e. along the diagonal of the cubic cell. This has an impact on the interface with the SiO_2, given the different amount of dangling bonds available in the two cases and how they interact with impurities.

(6 kΩ cm) $\langle 1\,1\,1 \rangle$ orientation and low-resistivity (1 kΩ cm) $\langle 1\,0\,0 \rangle$ orientation.

The characterisation of detectors consists of three basic measurements: leakage current (I_{leak}) drawn by a sub-detector at a known temperature; capacitance of the metal strips on a sub-detector to the backplane (backplane cap. C_{back}); capacitance of a metal strip to all its neighbours (interstrip cap. C_{int}).

These measurements are performed all in one go for all the 12 sub-detectors using a switch system that allows to perform this full measurement program automatically: capacitances were measured by an LCR bridge at four different frequencies 5, 10, 100 kHz and 1 MHz; the currents were measured by the voltage drop across a 100 kΩ resistor. All instruments in the system are connected to a PC via GPIB bus and controlled by LabVIEW. The detectors are mounted on a temperature-controlled chuck at around $-5°C$ and under a constant flow of nitrogen: this is inside a box placed in a cold room running at temperatures between $-5°C$ and $-10°C$ such that the ambient temperature is close to the detector temperature. Details on the system can be found in Ref. [2].

In order to study the effects of radiation damage, several multigeometry detectors were irradiated cold and under a bias of 100 V at a CERN PS primary beam line supplying 24 GeV protons with a fluence equivalent to 2.4×10^{14} 1 MeV neutrons. At this fluence the substrate of both the low- and high-resistivity detectors is under type inversion. All detectors were kept well below 0°C after irradiation; therefore, the total time those irradiated detectors were at room temperature is not more than a few hours.

Unirradiated high-resistivity detectors deplete at around 80 V and low resistivity ones at around 300 V. After irradiation, they deplete at around 300 V (high resistivity) and around 250 V (low resistivity).

All measurements are referred to a bias voltage of 500 V if not stated differently and after waiting for at least 3 h at the maximum voltage. No changes in the results are observed if biases down to 1.5 times the depletion voltage are considered, except for irradiated high-resistivity detectors (see comments in Section 4). A frequency of 1 MHz has been used and an amplitude of 30 mV for the AC signal sent by the LCR meter.

3. Capacitance parametrisations

3.1. Interstrip capacitance

The measured interstrip capacitances for GEOM1 detectors are shown in the top left plot of Fig. 1 vs. w/p.[2] The interstrip capacitances of different regions with the same pitch are lying on straight lines with similar slopes but different offsets. For a given value of w/p the interstrip capacitance decreases approximately linearly for increasing pitches. This is in contrast with expectations found in literature [3] where an electrostatic calculation is made for a strip in between two semi-infinite plates from which it is separated by gaps $(p - w)$, resulting in a dependence on w/p only for $0.15 < w/p < 0.50$ of $C_{int} = (0.9 + 1.7w/p)$ pF/cm.

This approximation, assuming an infinite wafer thickness, is a poor one already for $p = 120$ μm and it breaks down for $p = 240$ μm, where the pitch is comparable to the detector thickness.

It is possible to express the interstrip capacitances as linearly dependent on $(w + 20\ \mu m)/p$ as shown in the top right of Fig. 1. It is found that

$$C_{int} = \left[0.03 + 1.62\frac{(w + 20\ \mu m)}{p} \right] \text{pF/cm} \qquad (1)$$

with a sigma of 0.06 pF/cm.

3.2. Backplane capacitance

In literature, a semi-analytical solution of the Poisson's equation predicts a backplane capacitance C_{back} of a microstrip detector dependent on the segmentation [4]

$$C_{back} = \left(\varepsilon_0 \varepsilon_{Si} \frac{p}{d} \right) C_{wp} \quad \text{where} \quad C_{wp} = \frac{1}{1 + p/d\, f(w/p)}, \qquad (2)$$
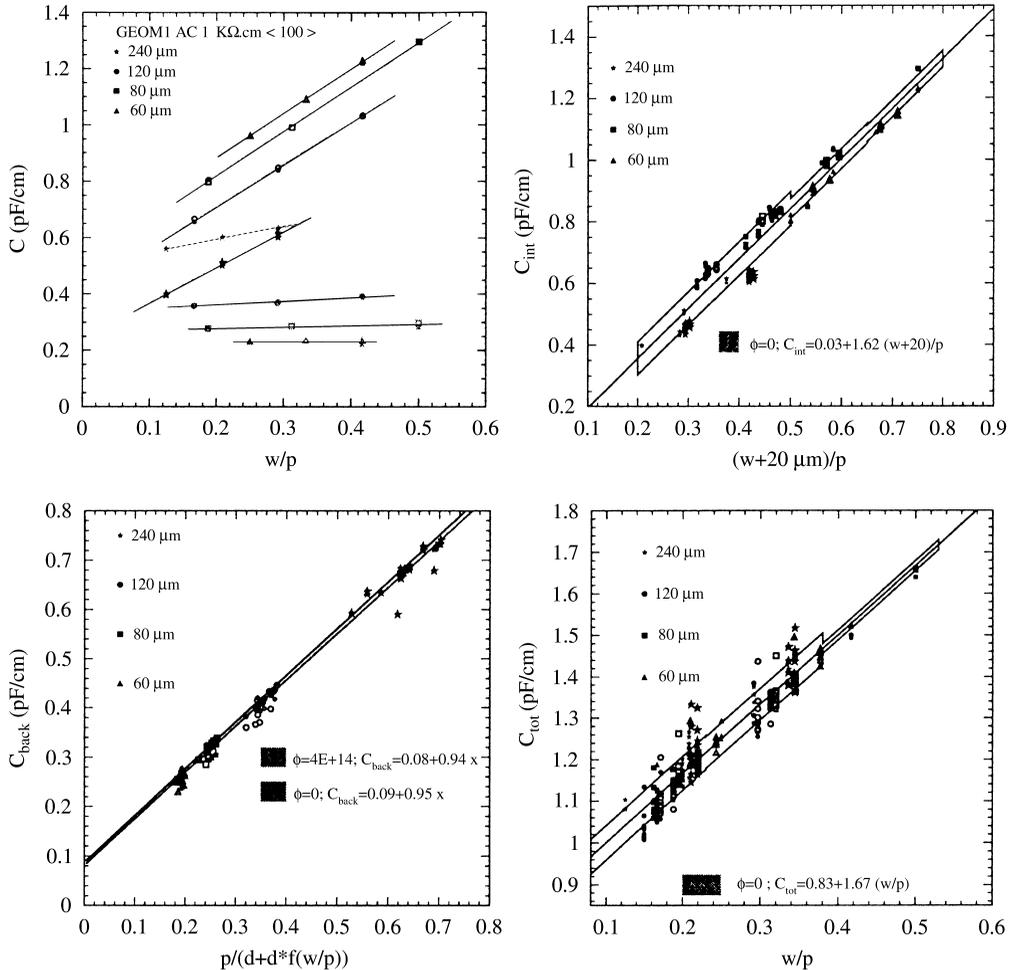
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[2] w and p are the implant width and pitch.

Fig. 1. Top left: Dark lines (light lines) represent fits to measured values of C_{int} (C_{back}) vs. w/p for one detector. C_{int} decreases as pitch increases; the opposite for C_{back}. Top right: C_{int} vs. $(w + 20 \, \mu m)/p$ for all unirradiated detectors. Bottom left: C_{back} vs. $p/d \, C_{wp}$ both for unirradiated and irradiated detectors. Bottom right: Total capacitance for all unirradiated detectors: it scales with w/p. Empty bands represent 1 standard deviation region around the best line fit.

where f is expressed as a series expansion in w/p with power from -2 to 2, d is the detector thickness and C_{wp} is a correction factor almost linear on the pitch and varying from 0.6 to 0.95 for $p = 240 \, \mu m$ pitch for increasing w/p from 0.1 to 0.5. Results on C_{back} are shown in the bottom right plot of Fig. 1 vs. $(p/d \, C_{wp})$: here, one finds a slope not far away from the expected $\varepsilon_0 \varepsilon_{Si} = 1.05 \, pF/cm$ and an intercept different from zero, given the small spread of values measured. The difference from the

prediction cannot be accounted for by the uncertainty of the wafer thickness alone.

3.3. Total capacitance

The total capacitance C_{tot} is obtained by adding the measurements of interstrip and backplane capacitances. Results are shown in the bottom right plot of Fig. 1 as a function of w/p. In the overall range, the measurements of C_{tot} can be expressed as

a function of the w/p ratio only. This indicates that the increase of the backplane capacitance at smaller pitch is almost exactly compensated by the decrease of the interstrip capacitance (see the left top of Fig. 1). It is found that

$$C_{tot} = \left(0.83 + 1.67\frac{w}{p}\right) \text{ pF/cm} \qquad (3)$$

with a sigma of 0.04 pF/cm. This is an important scaling that is not found in literature for large pitches. The total strip capacitance has been calculated by an electrostatic simulation [5] solving a two-dimensional Poisson's equation and provides a linear dependence of C_{tot} on w/p but shows already a slight decrease for a pitch of 100 μm. These model predictions, in the range of pitches considered, are still compatible with the results shown here within 0.2 pF/cm.

4. Radiation damage and crystal orientation

4.1. Interstrip capacitance

After the exposure to irradiation, for $\langle 1\,1\,1 \rangle$ high-resistivity detectors a significant increase in the measured interstrip capacitances is found, see Fig. 2 top plots; after 3 h at the maximum voltage C_{int} decreases but reaches a stable value.

The correlation between the measured capacitance and the effective width used to parametrise the data is degraded but still visible. On the contrary, for $\langle 1\,0\,0 \rangle$ low-resistivity devices no changes in the measured interstrip capacitances are observed after the exposure to radiation.

The behaviour of $\langle 1\,0\,0 \rangle$ and $\langle 1\,1\,1 \rangle$ is very different as is obvious from the plots of Fig. 3 where C_{int} is displayed vs. voltage before and after irradiation. The measurement of irradiated detectors is shown as measured at two different frequencies, 100 kHz and 1 MHz. It is visible that after irradiation $\langle 1\,0\,0 \rangle$ is almost constant and flat at 1 MHz; on the contrary $\langle 1\,1\,1 \rangle$ has a sharp rise for decreasing biases. C_{int} displays also a frequency dependency, being higher for lower frequencies in $\langle 1\,1\,1 \rangle$.

The measurements were made for all three different batches and always the $\langle 1\,0\,0 \rangle$ C_{int} was unchanged after irradiation, both at 300 and 500 V, while $\langle 1\,1\,1 \rangle$ was slightly higher at 500 V and substantially higher at 300 V. Difference in the amount of increase for different batches for $\langle 1\,1\,1 \rangle$ indicates a sensitivity to the processing parameters which could affect the growth of the silicon oxide.

4.2. Backplane capacitance

It is unchanged after irradiation; see the bottom left plot of Fig. 1.

4.3. Total capacitance

It is increased by the increase of C_{int} for $\langle 1\,1\,1 \rangle$ detectors and unchanged for $\langle 1\,0\,0 \rangle$, see Fig. 2 bottom plots. The linear dependence is still visible but degraded for $\langle 1\,1\,1 \rangle$. The relevance of the difference in the measured C_{tot} after irradiation between $\langle 1\,1\,1 \rangle$ and $\langle 1\,0\,0 \rangle$ is confirmed also by the S/N ratio and noise measurements at the testbeam as shown in Fig. 4 for detectors with $p = 60$ μm. After irradiation, the S/N is 20% higher for $\langle 1\,0\,0 \rangle$ than for $\langle 1\,1\,1 \rangle$, as expected from laboratory measurements. The higher S/N of $\langle 1\,0\,0 \rangle$ for unirradiated detector is due to an 8% thicker substrate. The noise figure shown on the right plot displays a dependency on the voltage as shown by laboratory measurements, where after irradiation $\langle 1\,1\,1 \rangle$ substrates have much higher value of C_{int} than $\langle 1\,0\,0 \rangle$ substrates when going to lower bias voltage.

4.4. Consideration on the results

C_{int} is known to depend on the positive charges trapped on the SiO_2 since they attract electrons in the region between strips that behaves as a conductor layer. Investigations on MOS structures have revealed that before irradiation, as expected, $\langle 1\,0\,0 \rangle$ has a smaller trapped charge than $\langle 1\,1\,1 \rangle$ when a good SiO_2 is grown. After irradiation, the total amount of charge in the SiO_2 is not dramatically lower in $\langle 1\,0\,0 \rangle$, according to measurements on MOS irradiated with photons. One can argue that the difference in C_{int} after irradiation between the two crystal orientations is due to the effect of
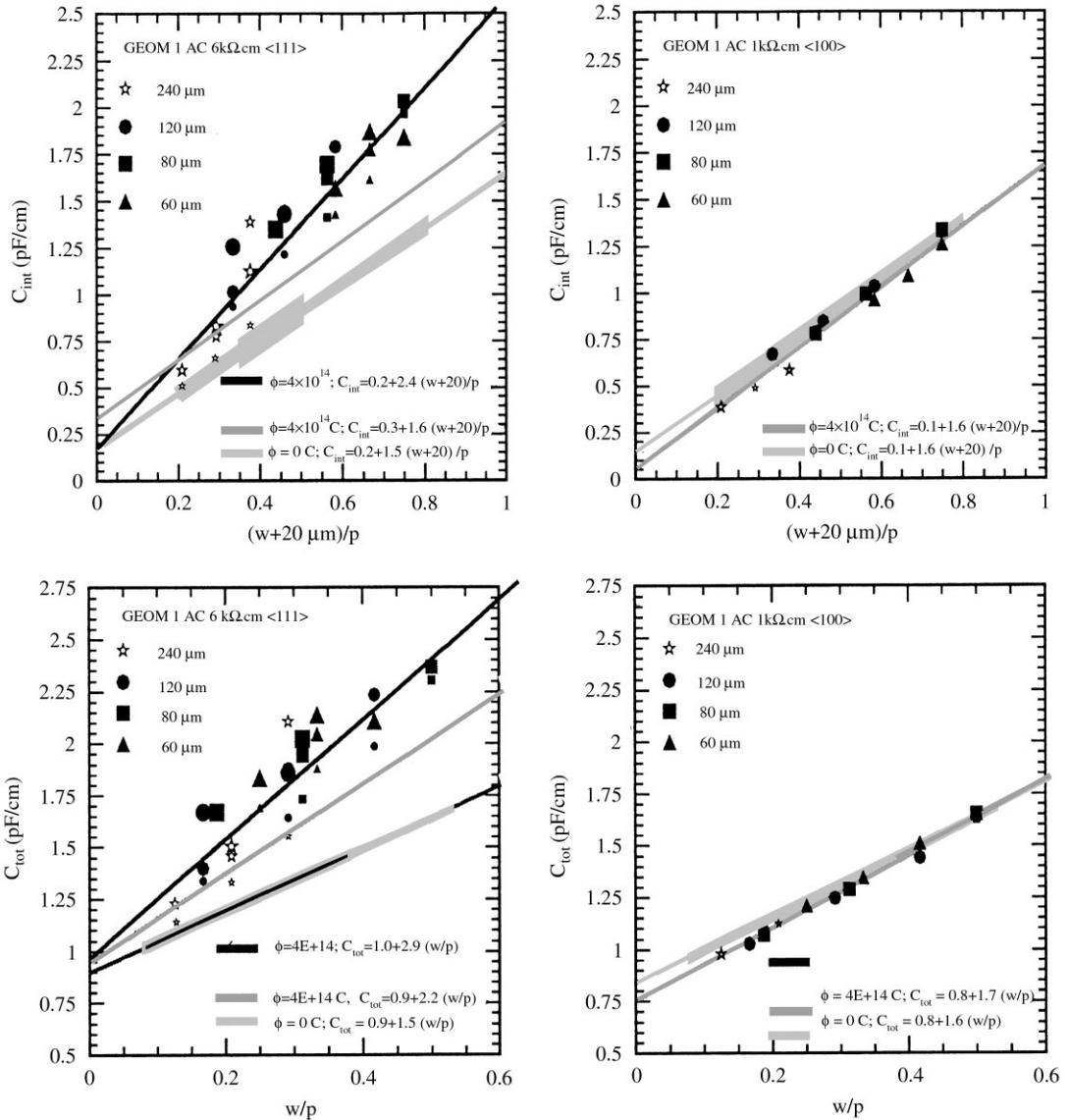
Fig. 2. Results after irradiation with protons, equivalent to 2.4×10^{14} 1 MeV n. On the top C_{int} plots; at the bottom C_{tot} plots. On the left and right, respectively, results for high-resistivity $\langle 1\,1\,1 \rangle$ and low-resistivity $\langle 1\,0\,0 \rangle$ detectors. The light-grey band represents 1 standard deviation region around the best line fit for unirradiated detectors. Measurements performed after an initial wait of 3 h at the maximum voltage are indicated by the letter C. Data points are shown only for irradiated detectors.

dangling bonds in the mobility of the charges accumulated between strips, as also shown in Fig. 3, and therefore their interaction with the defects in the bulk, but further studies are needed to understand the effect.

5. High voltage stability

Two classes of problems can occur when operating the detector at very high bias voltage: breakdown in the guard ring and breakdown in the
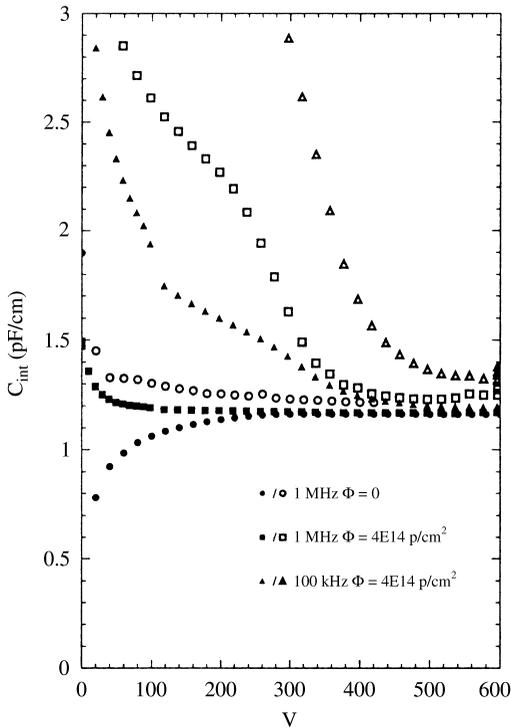
Fig. 3. C_{int} per unit length measured on AC coupled detectors ($p = 60\ \mu m$, $w/p = 0.2$) before and after irradiation: full symbols $\langle 100 \rangle$ low-resistivity detector, empty symbols $\langle 111 \rangle$ high-resistivity detector.

strips. The first is due to the high electric field present in proximity to the edges of the detector where high surface currents can originate. The use of a multi-guard design to reduce this effect has been studied elsewhere [1]. The detectors used in these tests have a single guard strip design. The breakdown in the strips happens because a very high electric field is present at the edge of the p^+ implant and the magnitude of the field depends on the geometry: it is expected to be higher for large pitches and for small values of w/p ratio. The breakdown field for silicon is 30 V/μm. In practice, breakdown can occur at lower fields if the high electric field triggers a breakdown in a few imperfect strips and impair, at least locally, proper operation of the detector.

The high field in the silicon substrate is influenced by the position of the end of the metal line above the implant because of fringing effect. Some work was done in the past to study the effect of high electric fields in the region close to n^+ implants in a double-sided detector with double metal layer [6,7], and it is evident that if a metal strip larger than the implant is adopted then the fringing is moved away from the implant end. Simulation studies have been performed in CMS for single-sided p^+ and show that a larger metal determines
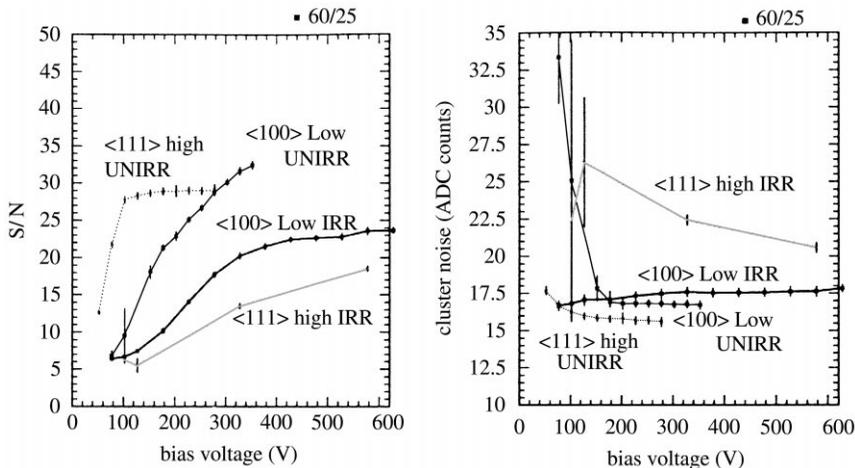

Fig. 4. Test beam results: in dark colour $\langle 111 \rangle$ detectors; in lighter colour $\langle 100 \rangle$ detectors. On the left plot S/N measurements vs. voltage and on the right noise vs. voltage (1 ADC is about 55 electrons). Data for both irradiated and unirradiated detectors are displayed (see text). $p = 60\ \mu m$, $w = 25\ \mu m$; Strip length was 6 cm and premux chip (integration time of 50 ns) was used. Temperature was $-5°C$.

a lower field in the silicon and a higher field in the more robust SiO_2 layer, that has a breakdown field of 600 V/μm. In order to analyse the breakdown in strips a sensitive method was developed, given that even just few strips in breakdown have to be detected. To do that, the second derivative of I_{leak} with respect to the voltage is calculated and when it is positive define that to be a breakdown. Correlated to breakdown of this kind, a departure from pn junction behaviour of C_{back} has also been found which starts to increase.

For unirradiated devices the breakdown is not a problem, given the lower depletion voltage involved, and yet for $w/p = 0.2$ no evident breakdown has been seen up to 600 V. After irradiation the picture changes substantially. In Fig. 5 are shown the results for irradiated AC detectors for $\langle 1 1 1 \rangle$ high resistivity. Since measurements were done tending to a maximum voltage of 600 V, if the

device did not go into breakdown up to this value for this detector it is set at $V_{bdwn} = 600$ V. It is seen that AC GEOM1 detectors for $\langle 1 1 1 \rangle$ high resistivity for all pitches start to go into breakdown already at 400 V for $w/p = 0.2$.

The beneficial effect of the overmetal in AC GEOM2 detectors is clearly evident. For $\langle 1 1 1 \rangle$ high resistivity the regions without overmetal still go into breakdown similar to that for GEOM1 detectors. The regions of GEOM2 with the same w and p, in the same detector, but with the 8 μm metal overhang, are stable up to 600 V, with the exception of $p = 240$ μm, $w/p = 0.2$ that it is stable up to 520 V, still 100 V more than the region without overhang.

For AC $\langle 1 0 0 \rangle$ low-resistivity devices the benefit from having the overmetal is still visible for GEOM2 devices, while in the low statistics of GEOM1 devices do not suffer high voltages: this could be related to a difference in the processing. For DC detectors, the overmetal is still beneficial, but in general the breakdown performances are degraded compared to the AC devices.

6. Conclusions

The dependence of capacitance in p^+ on n microstrip detectors, on the width and the pitch of implants has been studied in a large phase space of parameters. C_{int} has been found to be linear in w but decreasing for increasing pitches. C_{back} roughly follows expectations. An important scaling of C_{tot} on w/p has been found.

The choice of $\langle 1 0 0 \rangle$ substrate is shown to be more radiation robust than standard $\langle 1 1 1 \rangle$. $\langle 1 1 1 \rangle$ was chosen a long time ago by the high-energy physics community because it was less affected by metal pitting in the substrate, and has never been revisited after the technological problem of pitting was solved by industrial processing. The use of $\langle 1 0 0 \rangle$ does not show any drawback and therefore has been considered by the CMS Silicon Tracker as baseline for the silicon detector.

High voltage stability in strips is important especially after high irradiations and breakdown can affect a detector with a w/p value lower than 0.2 for voltages up to 400–500 V. Stability is improved by
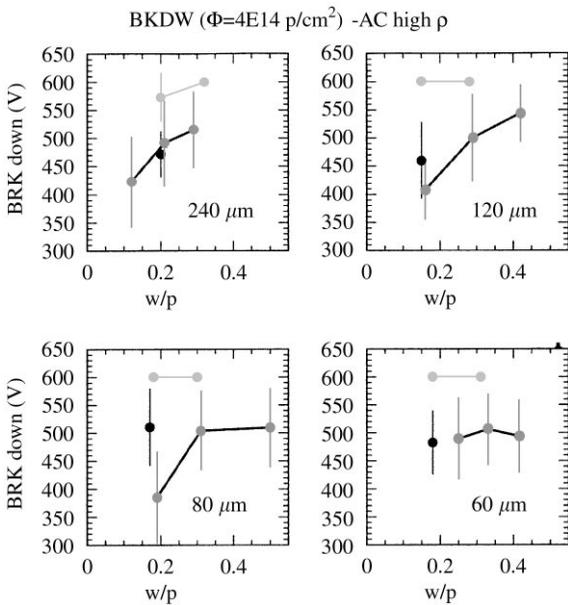
Fig. 5. Average breakdown voltage for irradiated AC detectors: light dots represent the regions with the overmetal, the dark ones the regions without. The error bars represent 1 standard deviation spread of the fitted values around the average. The analysed sample consists of two devices from GEOM1, and eight devices from GEOM2 all with high resistivity. 600 V was the higher bias investigated, so if a detector is shown with a breakdown of 600 V, this means that it did not go into breakdown.

the use of a metal width larger than implant width. No breakdown has been observed up to the maximum operational voltage accepted in CMS of 500 V when an overhang of 8 μm has been adopted.

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