AIDA FEE64 NON-LINEARITY TESTS

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Non-linearity tests were carried out for the AIDA FEE64 board at Daresbury laboratory on December 2009. The tested FEE64 board had four channels, which were tested individually. The AIDA FEE64 ADC is Analog Devices AD7686 (see specifications in Appendix). The Differential Non-Linearity (DNL) test was carried out using the PB-4 pulse and LG-1 ramp generators with ≈ 11 kHz counting rate.

As the reference voltage in the ADC is set in the middle of the dynamic range, each channel was tested with positive and negative signals. From hereafter ChX- refers to channels 379-32996 and ChX+ to channels 32590-65300. The measurement ranges were chosen so that non-linearity effects arising from the extremes of the ramp generator (i.e. when ramp generator changes its `direction') are kept minimal.

DNL

The resulting spectra from DNL measurements are shown in Fig. 1.

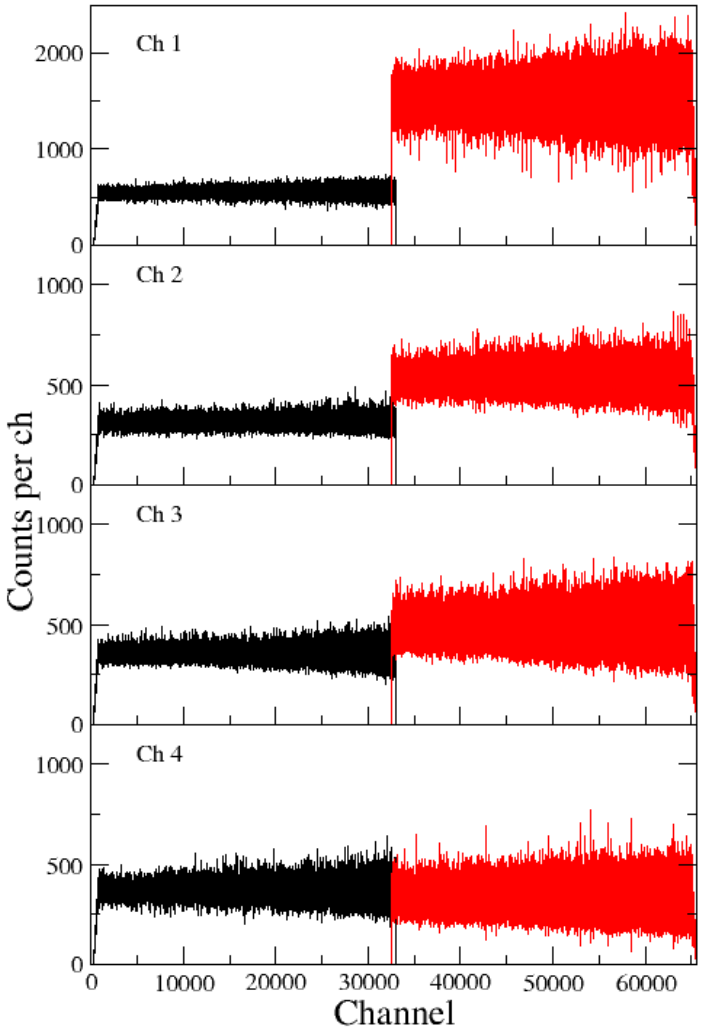

Figure 1. Pulser and ramp generator spectra of four channels on the test FEE64. Black (red) colour indicates negative (positive) polarity of the pulser.

The following quantities are quoted in the Table 1:

1. Mean $\overline{N}$ – average channel content within the measurement range.
2. Standard deviation σ of the channel contents within the measurement range.
3. $DNL = \sigma / \overline{N}$.
4. Maximum deviation ΔN_{max} from the mean within the measurement range.
5. Square root of the average channel content $\sqrt{\overline{N}}$.
6. $\sqrt{\overline{N}}/\overline{N}$.
7. Maximum of differential non-linearity L_D, L_D^{max}, as defined by Eq. 14 in IEEE Std 301-1976.

Table 1. DNL measurement results.

	$\overline{N}$	σ	DNL (%)	ΔN_{max}	$\sqrt{\overline{N}}$	$\sqrt{\overline{N}}/\overline{N}$ (%)	L_D^{max}
Ch1+	1509	188	12.5	1057	39	2.6	70
Ch1-	548	50	9.1	476	23	4.3	87
Ch2+	524	53	10.1	339	23	4.4	65
Ch2-	104	12	11.6	58	10	9.8	56
Ch3+	489	68	13.9	345	22	4.5	71
Ch3-	352	33	9.4	277	19	5.3	79
Ch4+	332	71	21.3	439	18	5.5	132
Ch4-	366	45	12.3	291	19	5.2	80

N.B. The maximum deviation ΔN_{max} is large. However, this may be due to non-linearity introduced by ramp generator. Although the extremes of the measurement range have been excluded, it is not trivial to define from which channel number such a non-linearity starts to pick up.

INL

Integral non-linearity (INL) tests were also carried out. The peak position in the spectra was measured as a function of a DC voltage over the full dynamic range with 0.512 V steps. The typical peak area was tens of thousands of counts and therefore the statistical error is negligible. Only three out of four channels were tested due to the lack of time. In Fig. 2 the results are illustrated. No visible non-linearity can be observed, at least when plotting the full dynamic range.

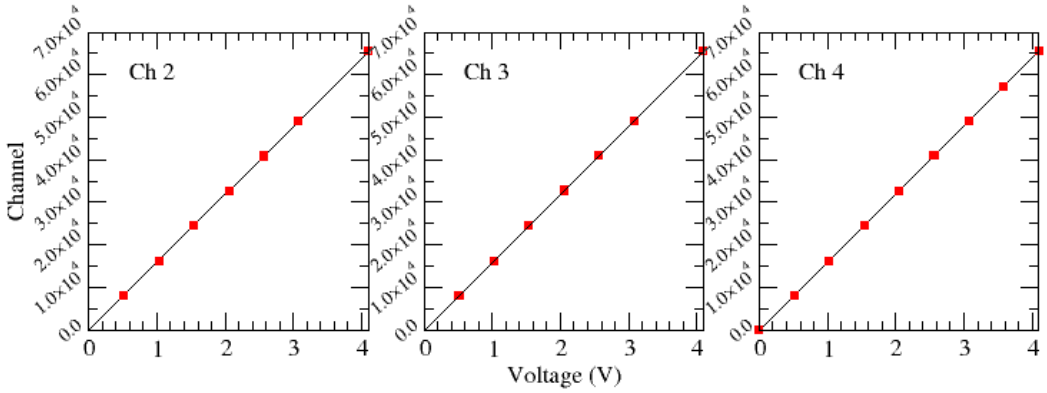

Figure 2. INL measurements for the three channels of the test FEE64. The red squares are the measurement points and the black line shows the linear behaviour.

INL, L_I, is defined as in `Selected Topics in Nuclear Electronics, IAEA, Vienna, 1986', is the maximum deviation from the linear behaviour over the measurement range. Table 2 shows the L_I values.

Table 2. The results of the INL measurements.

Channel	L_I (%)
2	0.050
3	0.026
4	0.048

16-Bit, 500 kSPS PulSAR ADC in MSOP/QFN

AD7686

FEATURES

- 16-bit resolution with no missing codes
- Throughput: 500 kSPS
- INL: ±0.6 LSB typical, ±2 LSB maximum (±0.003% of FSR)
- SINAD: 92.5 dB @ 20 kHz
- THD: −110 dB @ 20 kHz
- Pseudo differential analog input range
  - 0 V to V_{REF} with V_{REF} up to VDD
- No pipeline delay
- Single-supply 5 V operation with
  - 1.8 V/2.5 V/3 V/5 V logic interface
- Serial interface SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible
- Daisy-chain multiple ADCs and busy indicator
- Power dissipation
  - 3.75 µW @ 5 V/100 SPS
  - 3.75 mW @ 5 V/100 kSPS
- Standby current: 1 nA
- 10-lead MSOP (MSOP-8 size) and
  - 3 mm × 3 mm, 10-lead QFN (LFCSP) (SOT-23 size)
- Pin-for-pin-compatible with 10-lead MSOP/QFN PulSAR® ADCs

APPLICATIONS

- Battery-powered equipment
- Data acquisitions
- Instrumentation
- Medical instruments
- Process controls

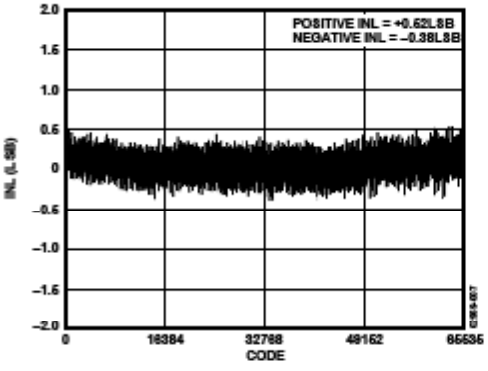

Figure 1. Integral Nonlinearity vs. Code

FUNCTIONAL BLOCK DIAGRAM

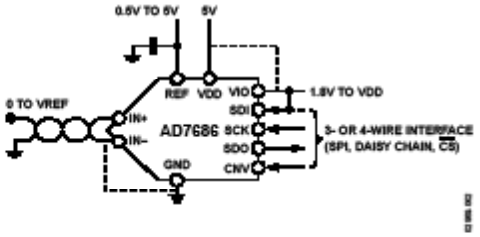

Figure 2.

Table 1. MSOP, QFN (LFCSP)/SOT-23 14-/16-/18-Bit PulSAR ADC

Type	100 kSPS	250 kSPS	400 kSPS to 500 kSPS	1000 kSPS	ADC Driver
18-Bit True Differential		AD7691	AD7690 AD7982	AD7982	ADA4941 ADA4841
16-Bit True Differential	AD7684	AD7687	AD7688 AD7693		ADA4941 ADA4841
16-Bit Pseudo Differential	AD7680 AD7683	AD7685 AD7694	AD7686	AD7980	ADA4841
14-Bit Pseudo Differential	AD7940	AD7942	AD7946		ADA4841

GENERAL DESCRIPTION

The AD7686 is a 16-bit, charge redistribution, successive approximation, analog-to-digital converter (ADC) that operates from a single 5 V power supply, VDD. It contains a low power, high speed, 16-bit sampling ADC with no missing codes, an internal conversion clock, and a versatile serial interface port. The part also contains a low noise, wide bandwidth, short aperture delay track-and-hold circuit. On the CNV rising edge, the AD7686 samples an analog input IN+ between 0 V to REF with respect to a ground sense IN–. The reference voltage, REF, is applied externally and can be set up to the supply voltage.

Power dissipation scales linearly with throughput.

The SPI-compatible serial interface also features the ability, using the SDI input, to daisy-chain several ADCs on a single, 3-wire bus or provides an optional busy indicator. This device is compatible with 1.8 V, 2.5 V, 3 V, or 5 V logic, using the separate supply VIO.

The AD7686 is housed in a 10-lead MSOP or a 10-lead QFN (LFCSP) with operation specified from −40°C to +85°C.

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