



CCLRC
Technology

AIDA design study

Overload and cross-talk

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Overview

Block diagram - top-level

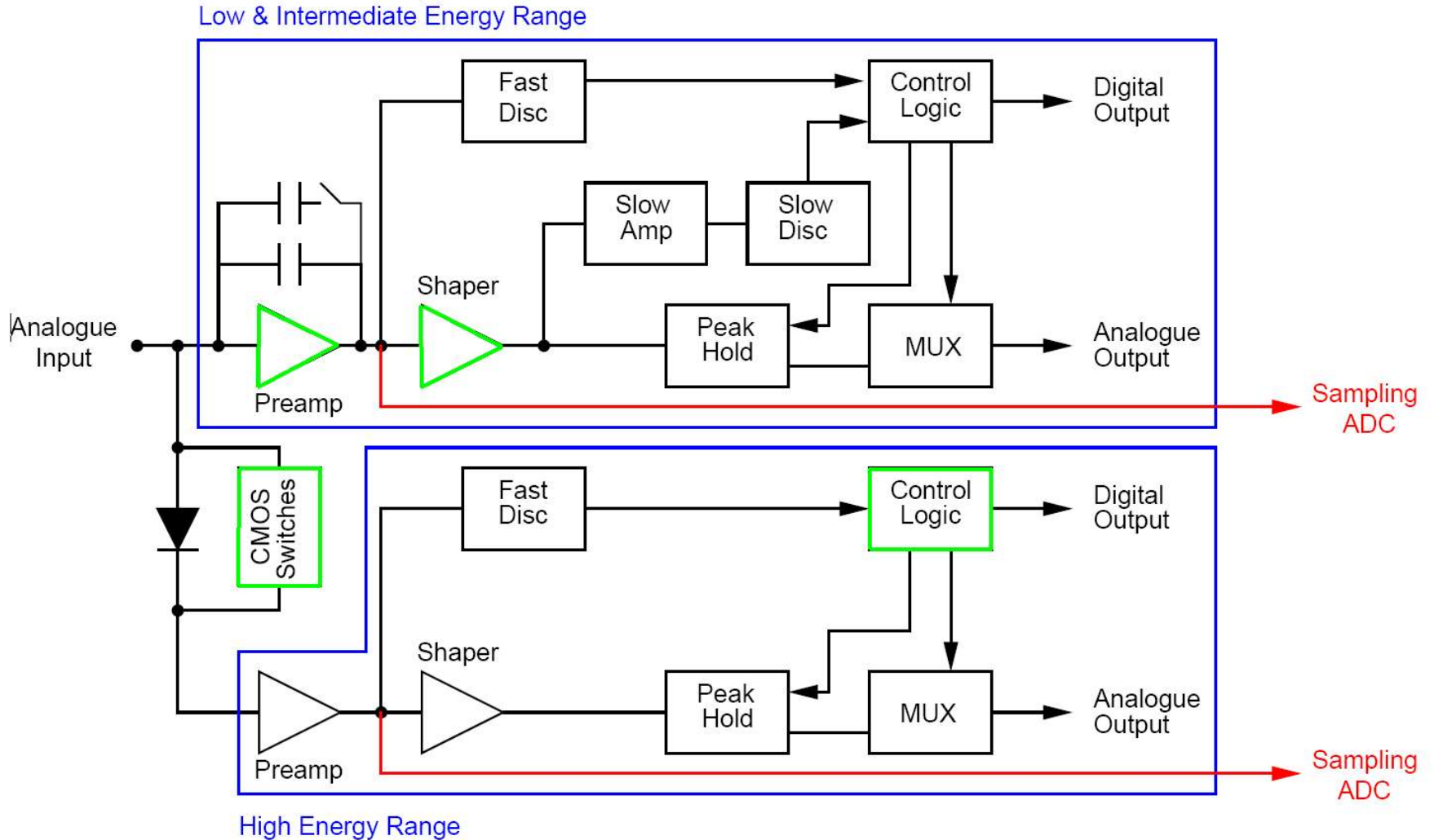
Overload recovery - the effect of fast reset

Timing of the link reset

Double-sided detector simulations

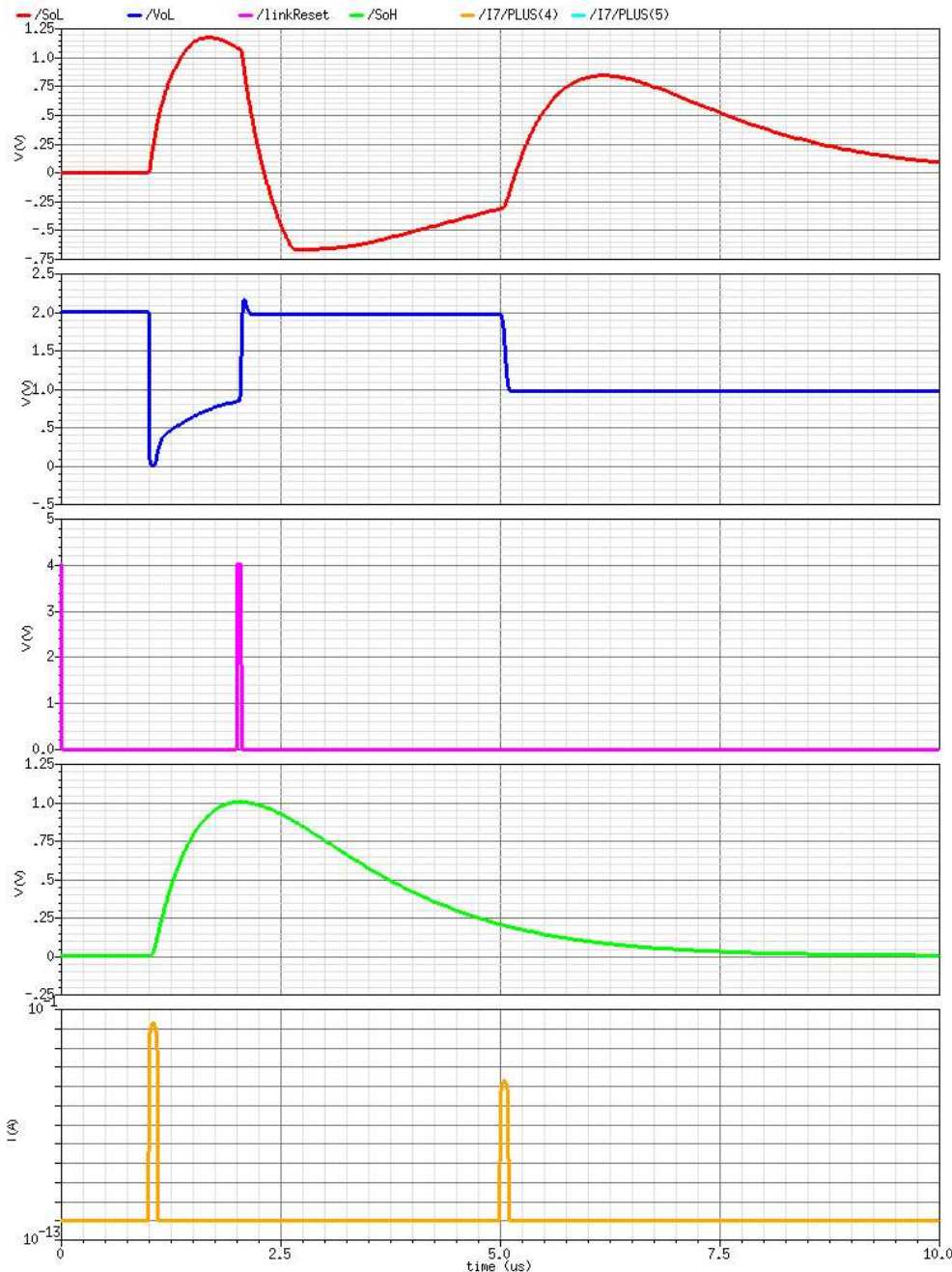
Cross-talk simulation

Conclusions



Fast overload recovery requires reset of low-energy pre-amp and shaper
 Timing signals will be produced by the high-energy control logic.

Overload recovery simulation



Low-energy shaper output, no reset

Low-energy pre-amp output, no reset

Link reset

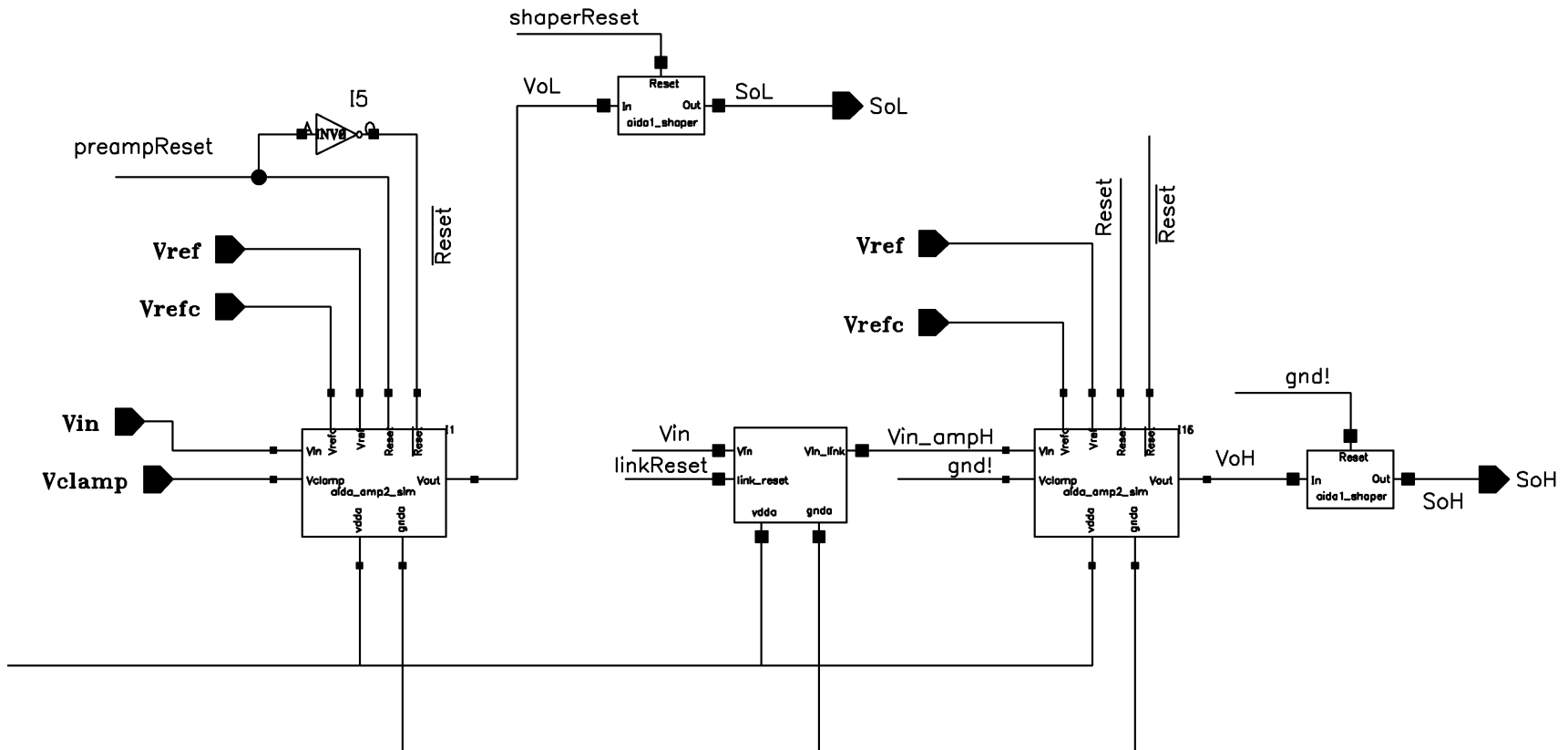
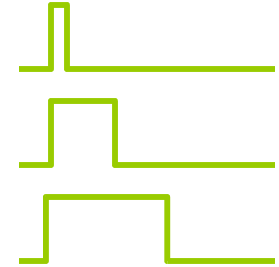
High-energy shaper output

Input current:

- 20mA peak, 1nC at $t = 1 \mu\text{s}$
- 20μA peak, 1pC at $t = 5 \mu\text{s}$

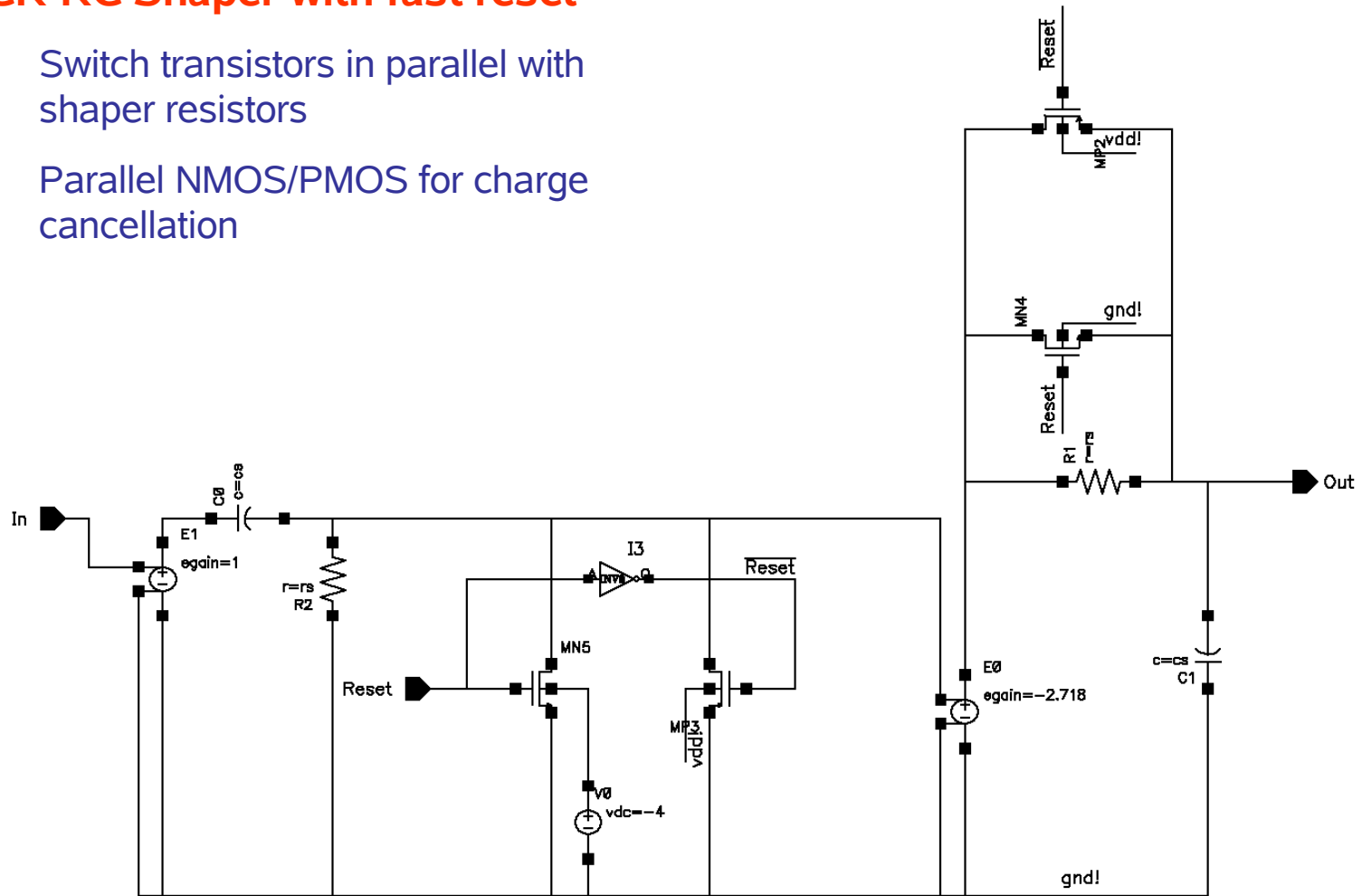
Analogue channel with additional resets

- 1 **Link reset:** disconnect link between low and high energy amplifiers
- 2 **Pre-amp reset:** fast discharge of feedback capacitor ($\sim 1\mu\text{s}$)
- 3 **Shaper reset:** transistors to short out shaper resistors ($\sim 2\mu\text{s}$)

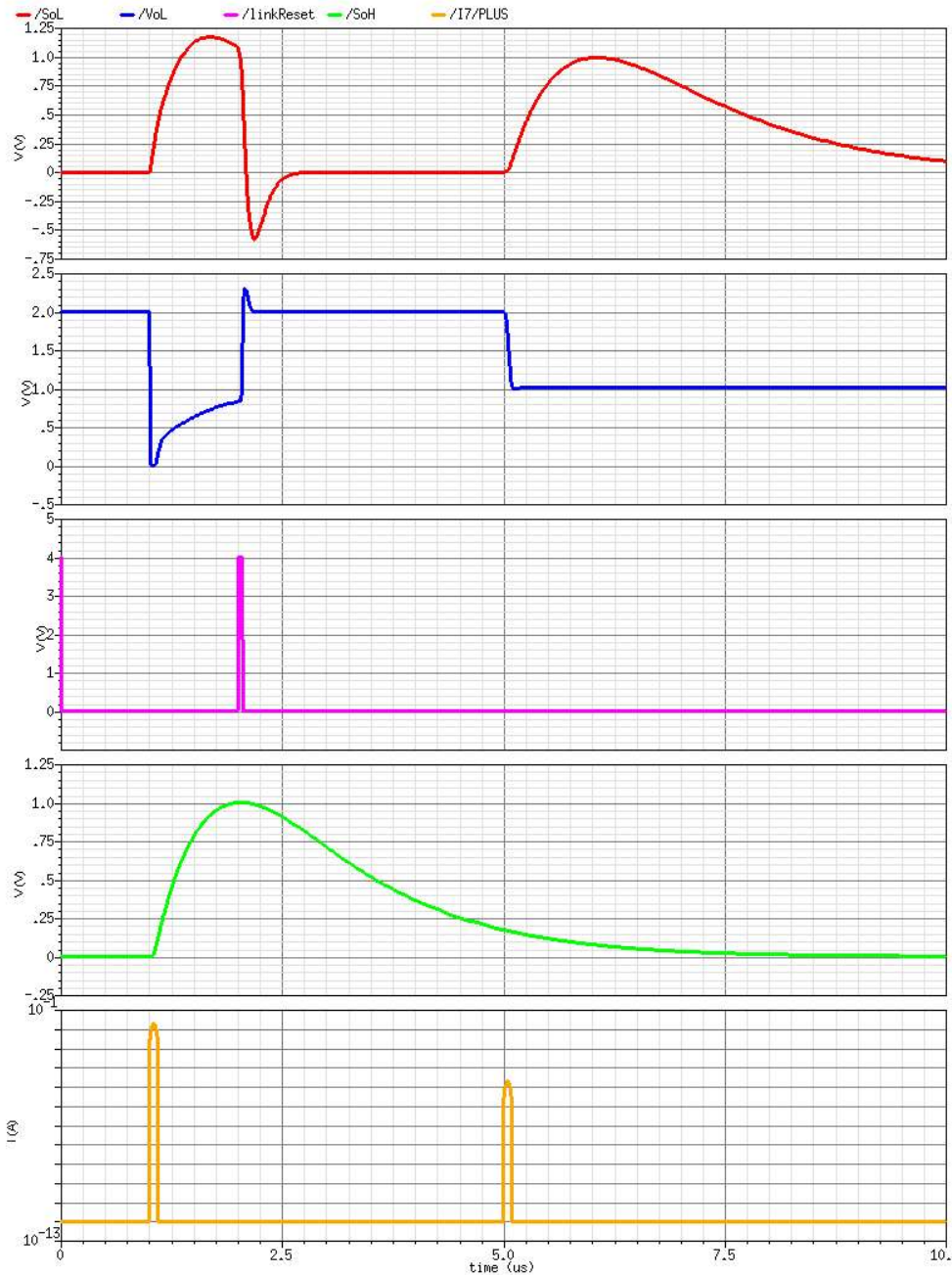


CR-RC Shaper with fast reset

- Switch transistors in parallel with shaper resistors
- Parallel NMOS/PMOS for charge cancellation



Overload recovery simulation



Low-energy shaper output, with reset

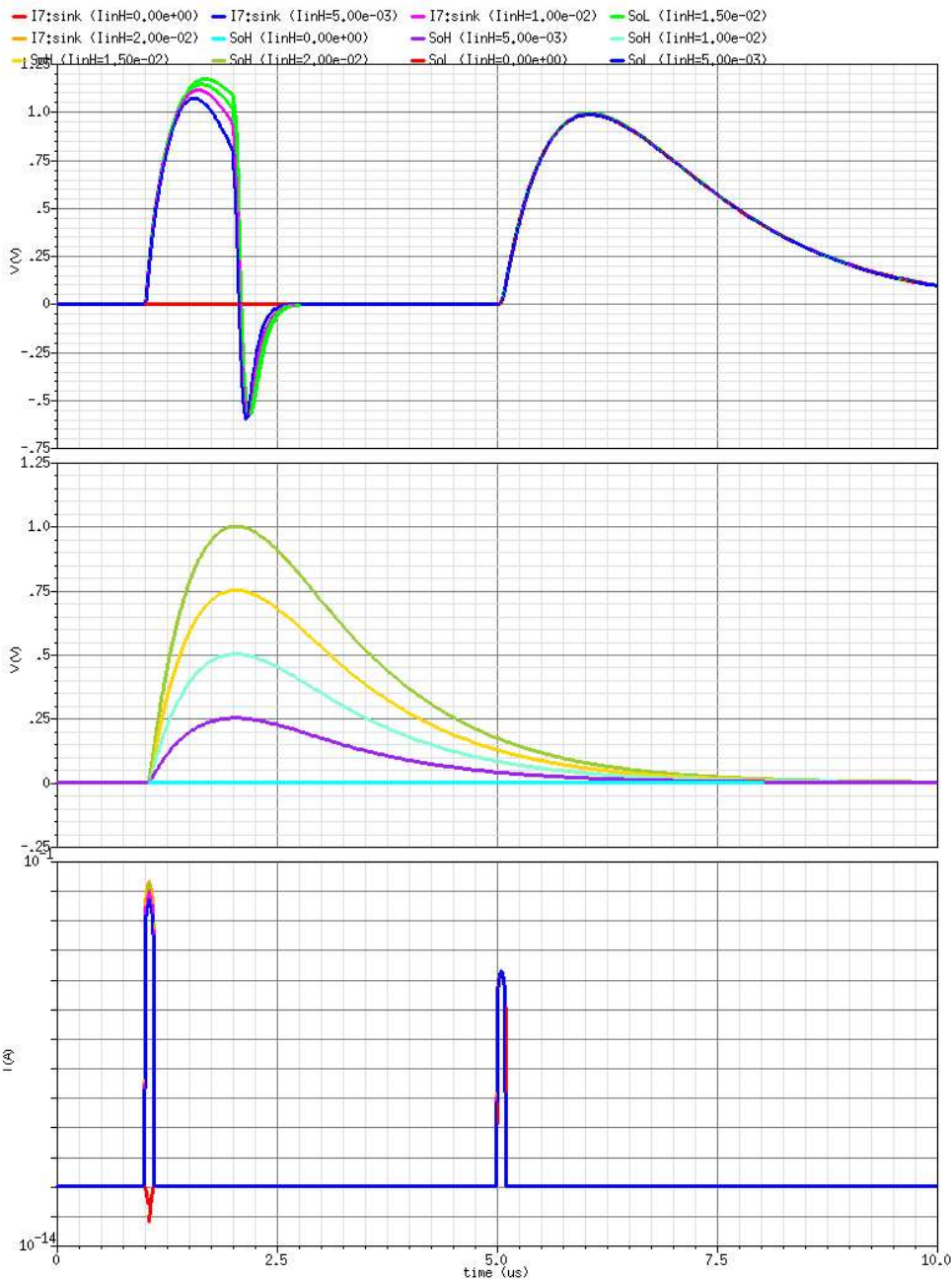
Low-energy pre-amp output, with reset

Link reset

High-energy shaper output

Input current

- 20mA peak, 1nC at $t = 1 \mu\text{s}$
- 20μA peak, 1pC at $t = 5 \mu\text{s}$

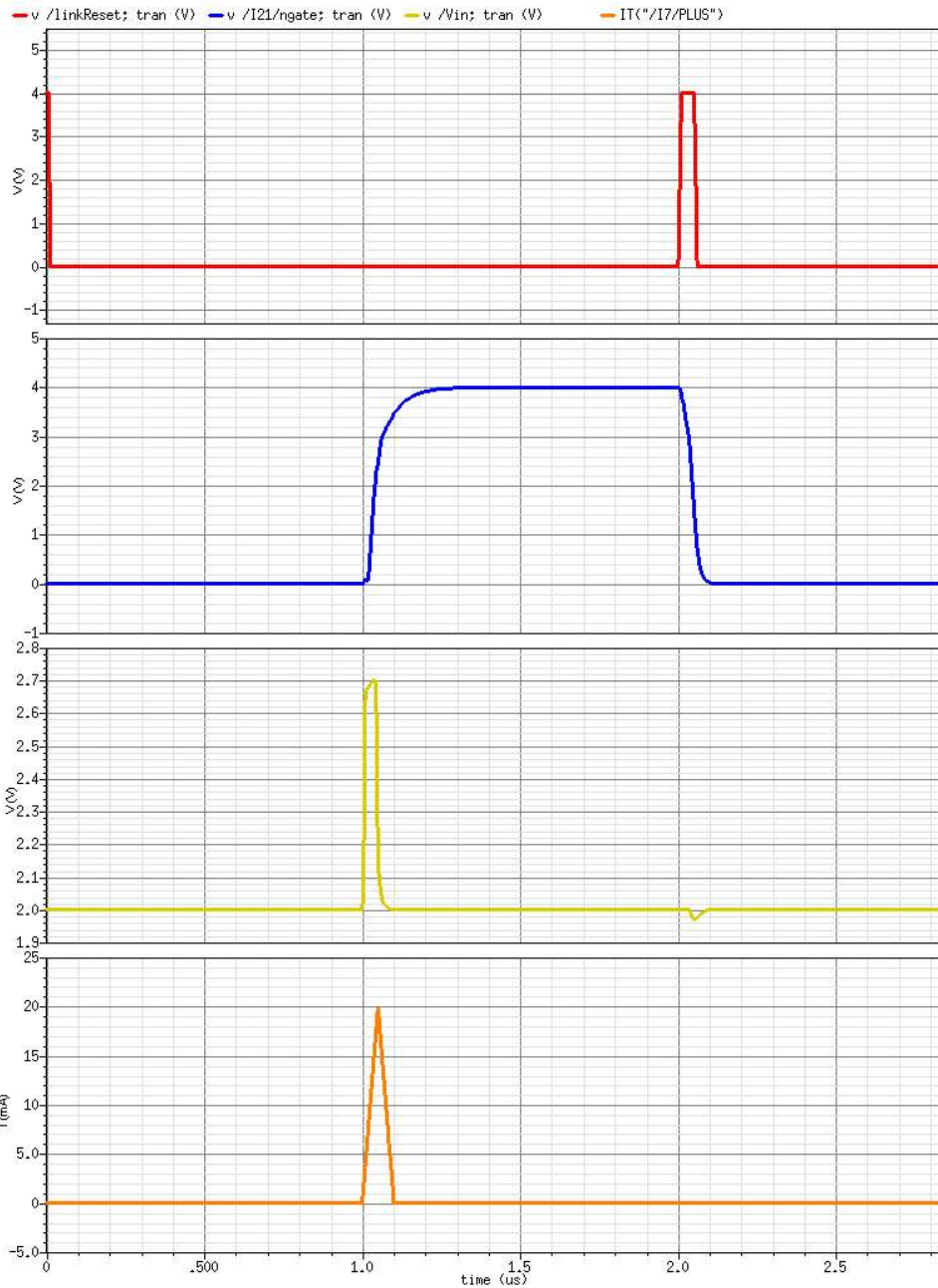


Overload recovery simulation: stepped current

Low-energy shaper output, with reset

High-energy shaper output,
0-20GeV in 5GeV steps

Input current, 0-20mA at $t = 1 \mu\text{s}$,
followed by $20\mu\text{A}$ at $t = 5 \mu\text{s}$



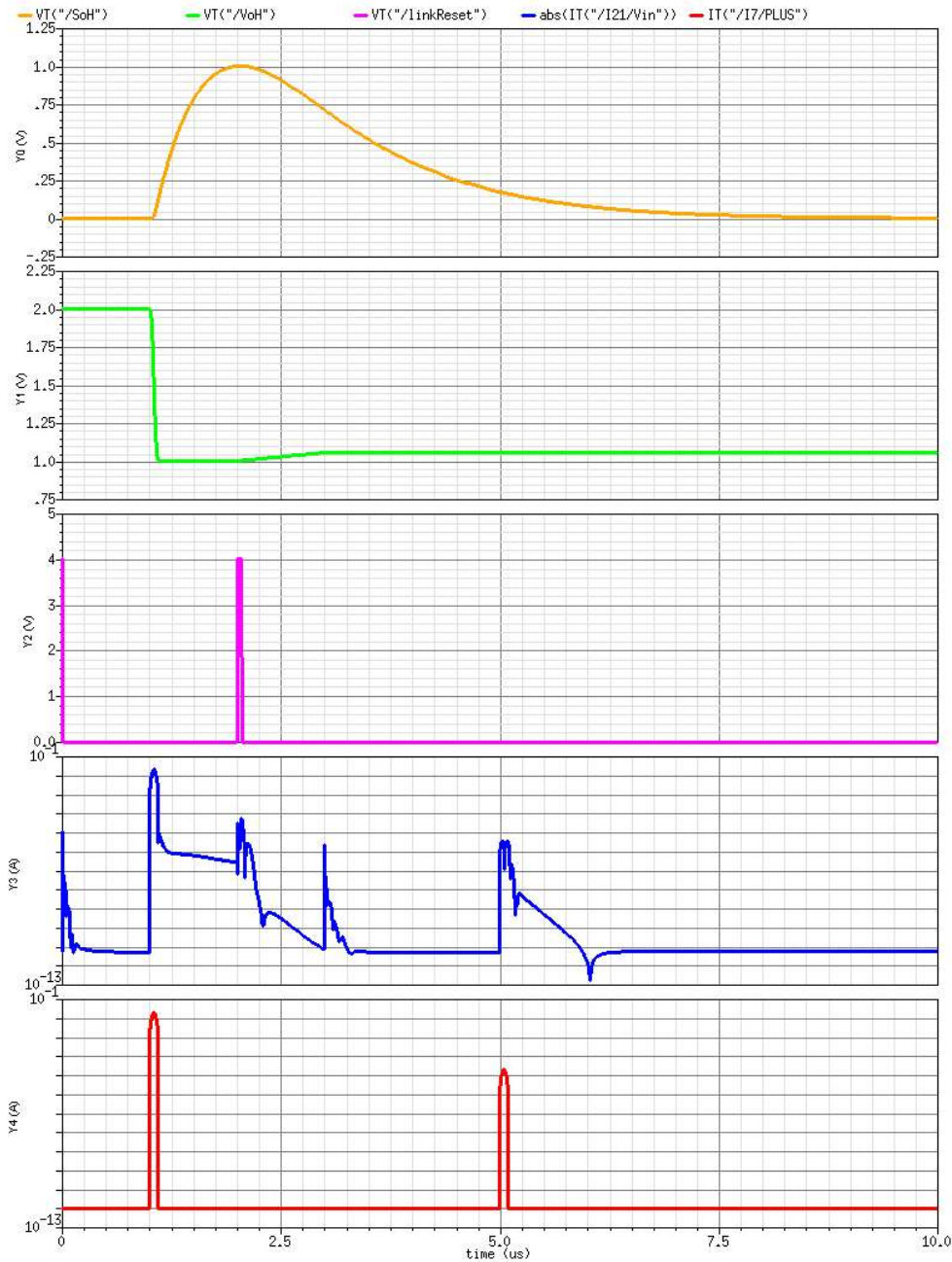
Timing of link reset

link reset

link gate control (NMOS switch)

Amplifier input voltage

Input current, 20mA at $t = 1\mu\text{s}$,



Timing of link reset

High-energy shaper output

High-energy pre-amp output

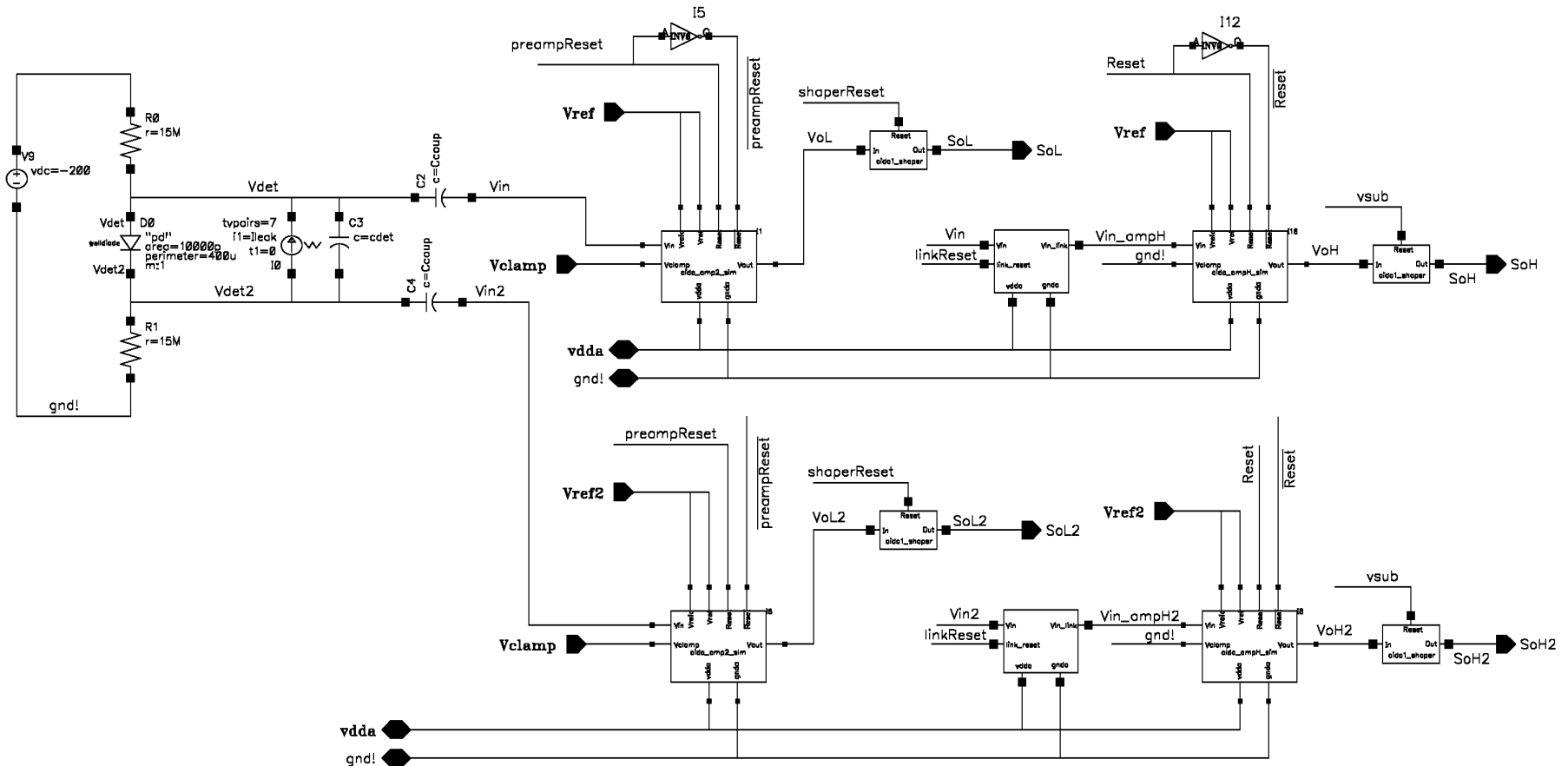
Link reset

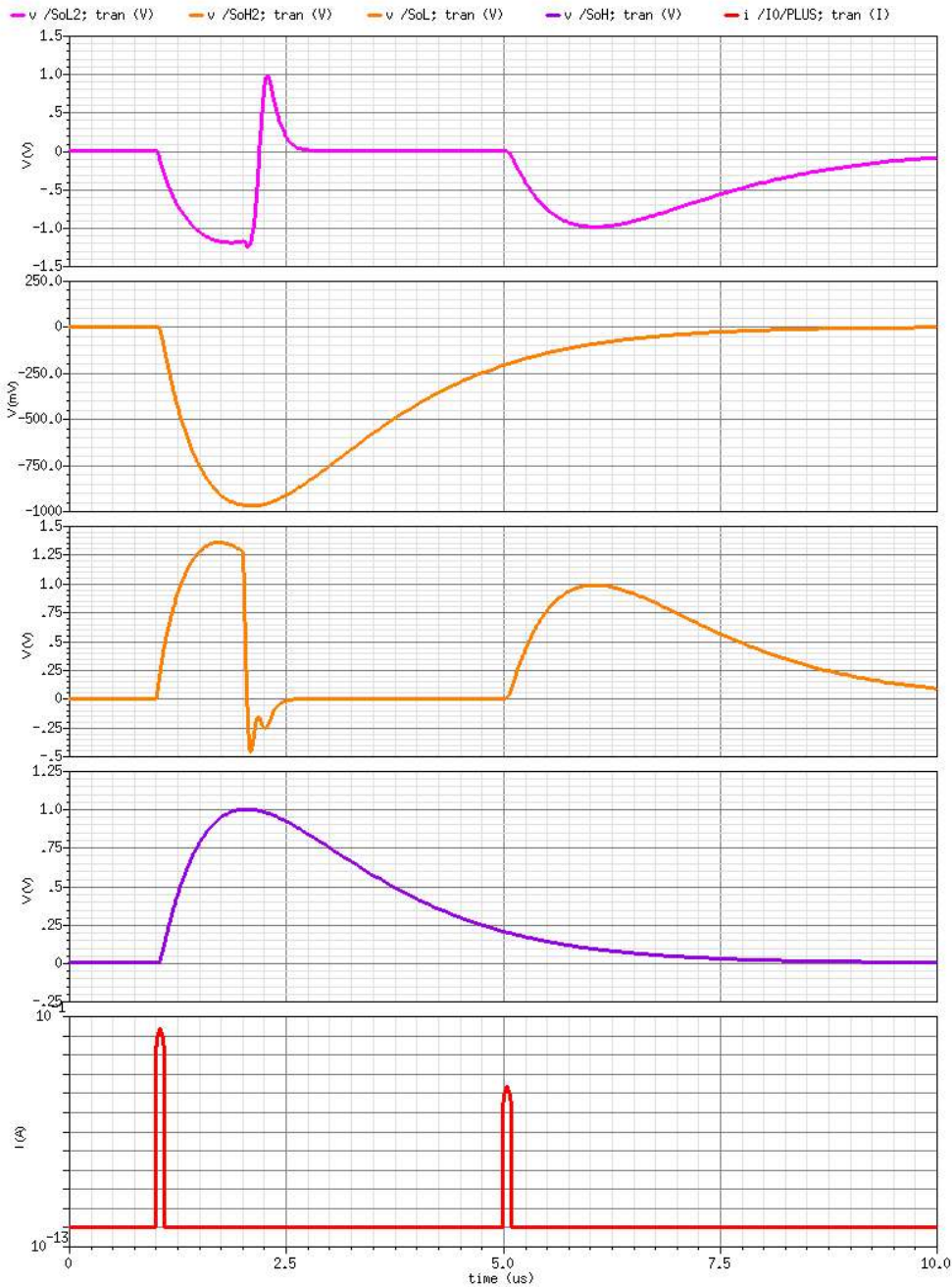
Link current

Input current

Double-sided amplifier simulations

- 15M bias resistors, 22nF coupling
- Separate bias for amplifiers, for optimum dynamic range
- Reversed polarity for diode link and comparator





Double-sided simulation

Low-energy shaper, n+ side

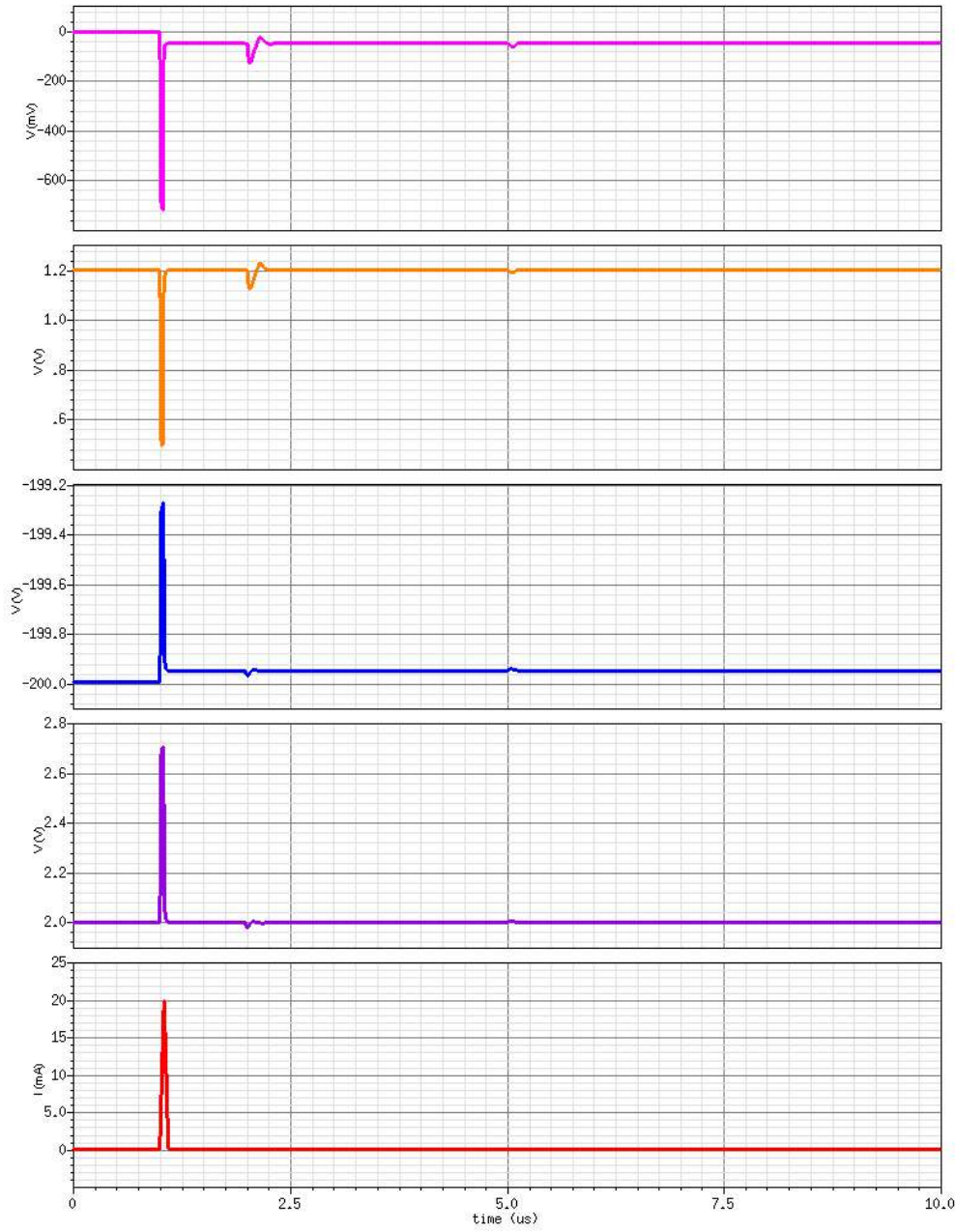
High-energy shaper, n+ side

Low-energy shaper, p+ side

High-energy shaper, p+ side

Input current: 20mA and 20 μ A

v /Vin2; tran (V) v /Vin; tran (V) v /Vdet2; tran (V) v /Vdet; tran (V) i /I0/PLUS; tran (I)



Double-sided simulation:

Detector voltage, n+ side :

700mV spike, with 50mV step

Pre-amp input, n+ side

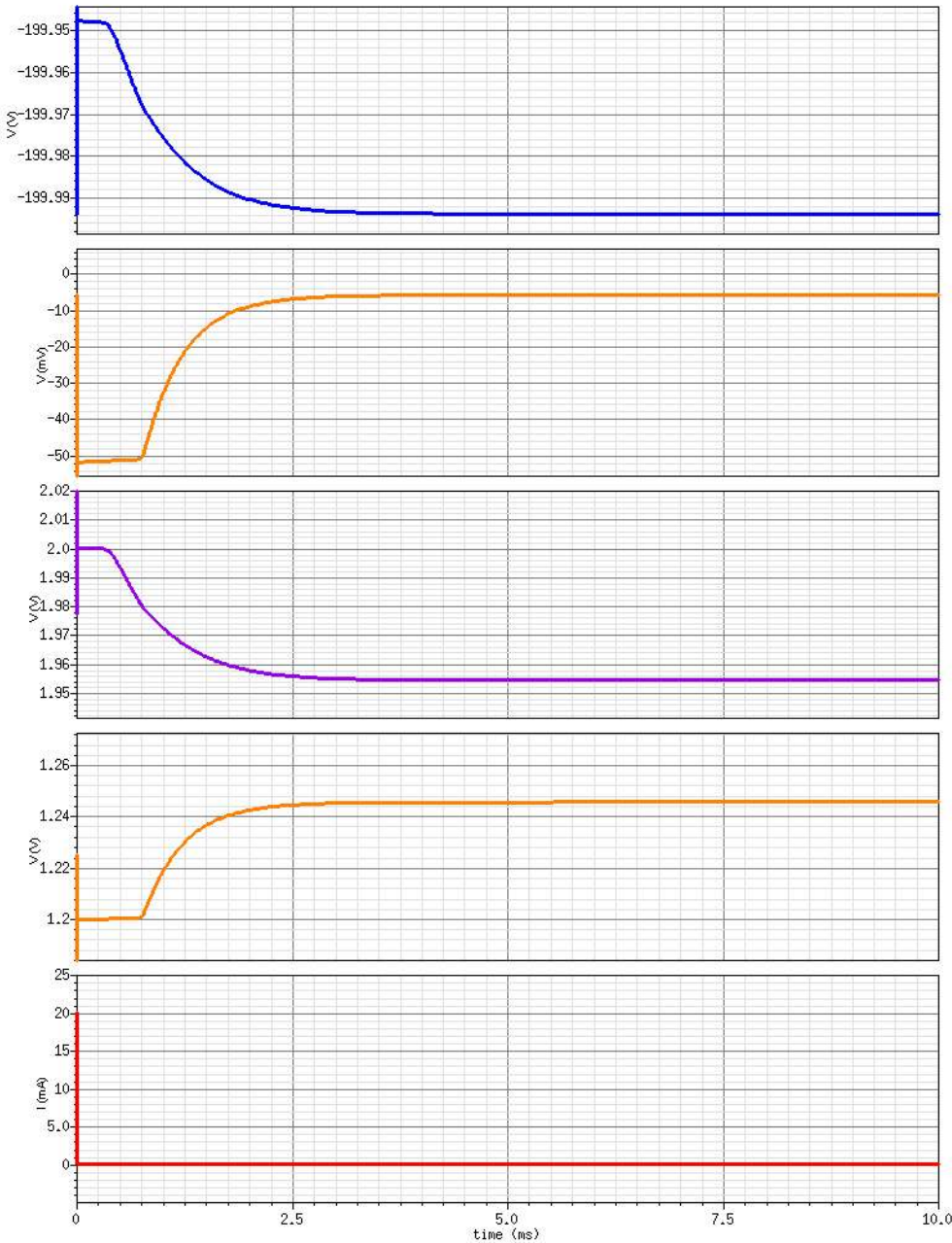
Detector voltage, p+ side :

700mV spike, with 45mV step

Pre-amp input, p+ side

Input current: 20mA

v /Vdet2; tran (V) v /Vin2; tran (V) v /Vdet; tran (V) v /Vin; tran (V) i /I0/PLUS; tran (I)



Double-sided simulation over 10ms

Warning: Simulator convergence problems, results unreliable

Detector voltage, p+ side :
recovery from 50mV step

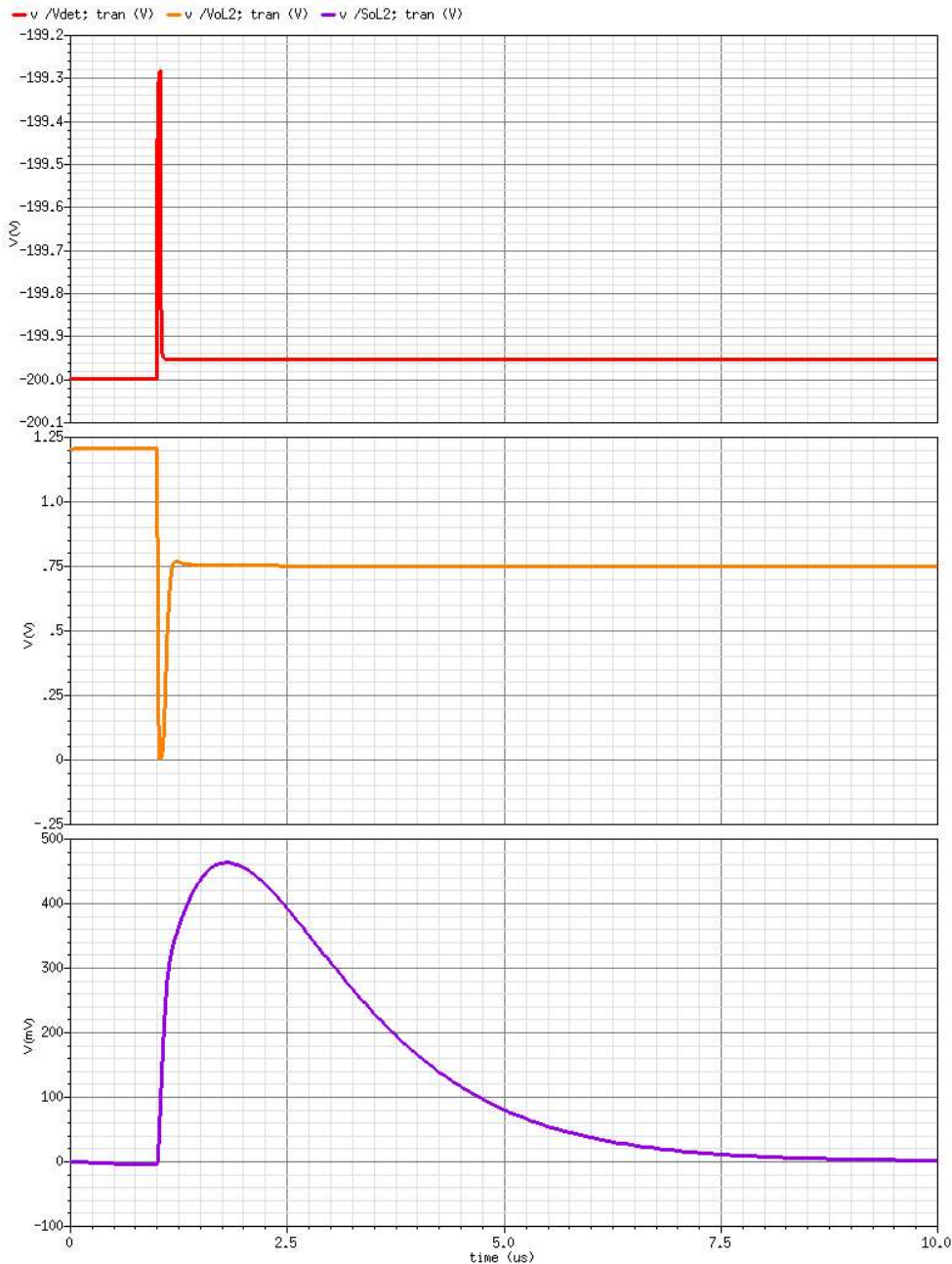
Detector voltage, n+ side
recovery from 45mV step

Pre-amp input, p+ side

Pre-amp input, n+ side

Input current: 20mA

Cross-talk simulation



Detector voltage, p+ side :
700mV spike, with 50mV step

Low-energy pre-amp output:
10pF coupling to detector voltage

Low-energy shaper output
No output on the high-energy channel

Conclusions

- Fast overload recovery is possible (a few μs)
- Extra reset pulses needed for pre-amp and shaper
- n+ read-out requires adjustment of amplifier operating point, with reverse polarity for diode and comparator
- Cross-talk effect matches earlier calculation ($\Delta V \sim 50\text{mV}$); initial voltage spike does not affect the shaper peak value