Changes to the FADC buffer circuits and ASIC mux out buffer/ADC ***(rev 6, Last Update 18/8/2010.)***

Reasons for changes to the FADC buffer circuits (sections 1-8):

1) *Improve stability*
2) *Reduce power*

Section 1- Comparison of ADA4932 and ADA4938

For both the reasons above (stability and power) it is proposed to change from ADA4938 diff amps to ADA4932. A comparison of the 2 is included in section 1 listing differences and benefits of the change.

Section 2- Change of buffer amplifier for ASIC Vref and Crosstalk via Vref

The ASIC Vref driver has insufficient output drive current to handle 16 channels and deal with transients in current demand from the diff-amps caused by output pulses. Therefore a new buffer is proposed. Section 2 explains the change and also analyses crosstalk between channels caused by coupling via Vref.

Section 3- Notes on system bandwidth

Section 4- Adding gain to the diff-amps to use full FADC range.

The diff amp output doesn't quite match the whole FADC range- can we add some gain to the diff amps? Rev 3- added table of simulated signal sizes after modification

Section 5- Operating at lower supply voltages- now obsolete (rev 5) so moved to appendix C

Section 6- Possibility of additional buffers to provide high impedance load to the ASIC

The ASIC preamp output stage has limited drive capability and so needs a relatively high impedance load. This section calculates the current load on the ASIC ouput. Subsequent ASIC simulations by Steve have confirmed that these loads can be handled by the ASIC. Therefore part of sec 6 (buffer selection table) is now obsolete and moved to appendix B.

Section 7- Checking AD4932 stability

Investigation of closed loop gain for various resistor values.

Section 8- Input impedance (and source current loading).

Section 9- Change to multiplexer ADC and gain change in associated buffer circuit

Reasons for changes-

1) to try to improve throughput/reduce inter-event gaps by using a faster ADC
2) to optimise the use of the ADC range.

History

Changes in rev3- mainly updates to section 6 amplifier table.

Changes in rev 4- move sec 6 buffer table to appendix B. Small revisions to tidy up section 2 and 4. Added sections 7 and 8

Rev 5- updated section 2 (includes AD8051 as well as AD8055) and re-simulated crosstalk using PWL pulses as well as 10MHz sine wave. Added section 9. Moved sec 5 to appendix C (obsolete).

Rev 6- continued to work on section 9- included conclusions regarding changes to ADC, changes to references and resultant change to gain and revised circuit diagram.

Section 1 Comparison of ADA4932 and ADA4938

The ADA4932 is a lower power device with lower bandwidth which is pin and function compatible with the ADA4938 used in AIDA. Both are unity gain stable.

The main differences I have found so far from the data sheets-

Parameter	**Comment**
Small signal Bandwidth	ADA4932 is 560MHz- about half the ADA4938.
Slew rate	ADA4932 is slower (2800V/us rather than 4700)
Crosstalk between 2 amps in dual package 10MHz	ADA4932 is better (-100db instead of -85dB)
Input offset voltage	ADA4932 is better (0.5mV instead of 1mV)
Input bias current	ADA4932 is better (2.3uA instead of 13uA)
Input capacitance	ADA4932 is lower (0.5pF against 1pF)
Input impedance	ADA4932 typically 2x higher
CMRR	ADA4932 is better (-100dB against -75dB)
Output balance error	ADA4932 is better (-64dB instead of -60dB)
VOCM	ADA4932 typ 25k (instead of 10k)
Power Supply Rejection Ratio	ADA4932 is better (-96 dB instead of -80dB)
Quiescent current	ADA4932 much better (9.6mA instead of 37mA)
Noise	ADA4932 is slightly worse(3.6 nV/√Hz instead of 2.6nV/√Hz)
Feedback resistors	ADA4932 data sheet talks about values of 499 and 768R as typical whereas ADA4938 data sheet mentions 200 and 402R.

V_{ocm} Both AD4932 and AD4938 recommend a buffer if multiple dual devices share an ADC Vref output to drive their V_{ocm} inputs. However the AD9252 output (fig 53 in data sheet) can drive 1mA with no significant voltage drop and the AD4932 is either 10K (operating notes) or 25K (data parameters) input impedance so worst case with 8 channels they will present 1250 ohms and consume 0.8mA.

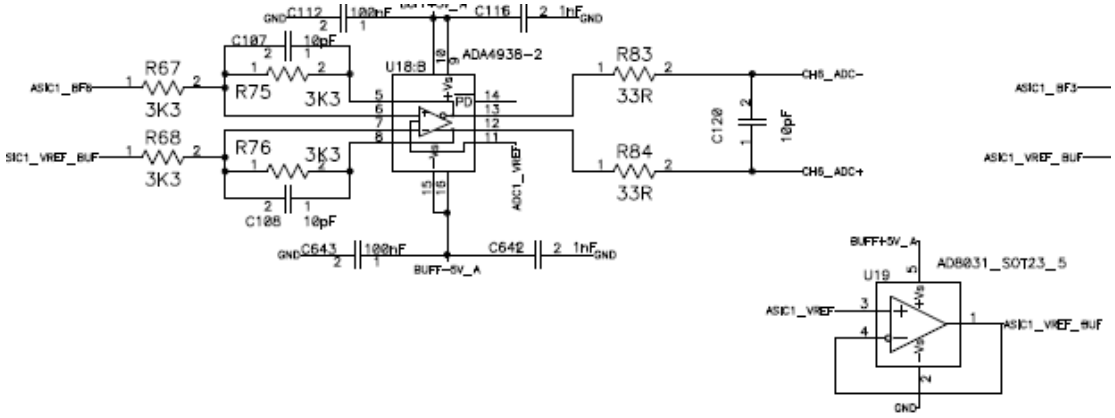
In spice simulation the ADA4932 behaves as expected and is less susceptible to oscillation than ADA4937 when provoked by a very fast step function input.

Conclusion

We should swap from ADA4938 to ADA4932 as ADC input buffers to obtain better power supply rejection, lower crosstalk, lower bandwidth and hence lower noise and less likelihood of oscillation and lower power consumption (saves about 1.7A over 64 channels).

Section 2 Buffer for ASIC_Vref_Buf and Crosstalk via Vref

Presently the buffering is done by one AD8031 driving all 16 diff amps for each ASIC.



The load presented by the diff amp circuit is approximately the sum of series and feedback resistors, R68 and R76 (assuming minimal output impedance and high input impedance of AD4932/8). For the original 3K3 design the current per channel is (1.6/6.6) mA = 0.24mA so total is 3.9mA, well within 15mA drive capability of AD8031.

However, the 3K3 values need to be reduced for amplifier stability and could go down to 330R with AD4938 (or maybe 499R with AD4932) which increases the current per channel to 2.4mA and 1.6mA with totals of 39 and 32mA respectively for all 16 channels. The max drive of AD8031 is only 15mA.

The ASIC output is not true differential so there is no requirement to track noise induced on both sides of the pair- the main function of V_{ref} is track low frequency drifts, not noise. Therefore the bandwidth of the buffer amp can be very low from this point of view. However it must also react to fluctuations in demand for current from the ADA4932 as it tracks the preamp output from the ASIC so must at least match the bandwidth and slew rate of the other ASIC output.

The AD8055 has 60mA output drive and a bandwidth wide enough (300MHz) to easily follow current demands of the AD493x diff amp. (Considered AD8605 with 80mA drive but slew rate is only 5V/us which is too slow to match the input from ASIC which could change by 1.4V in 90ns- 3x faster).

Rev5- found AD8051 which looks even better in simulation that AD8055. AD8051 has 110MHz bandwidth, 145V/us slew rate, operates from either +5V or dual ±5V supplies, available in SOT23-5. The lower bandwidth seems to reduce the overshoot and yet the amplifier still responds fast enough. AD8051 drives up to 45mA out (within 0.5V of rails); to stay within 0.4V of the rails the current is limited to just over 40mA at 25C (or about 37mA at 85C) according to fig 31 on data sheet.

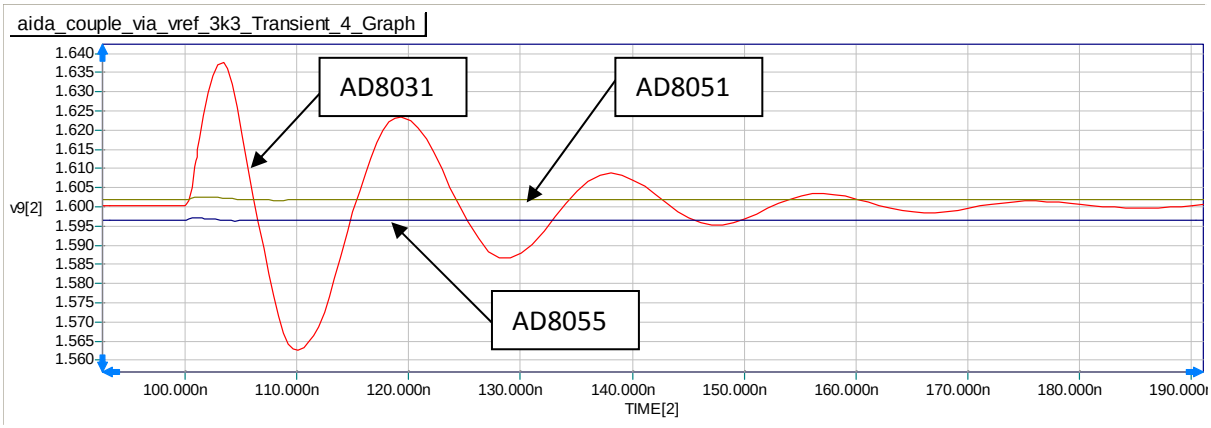
Testing buffers in Spice simulation

It is possible to provoke some ringing in the AD4938 amplifier by feeding it a 1ns rise time step[1]. The configuration simulated was with 499 feedback resistors (with no parallel capacitors) and 499 input resistors. Both diff amps were simulated as AD4932; one input was connected to the step and the

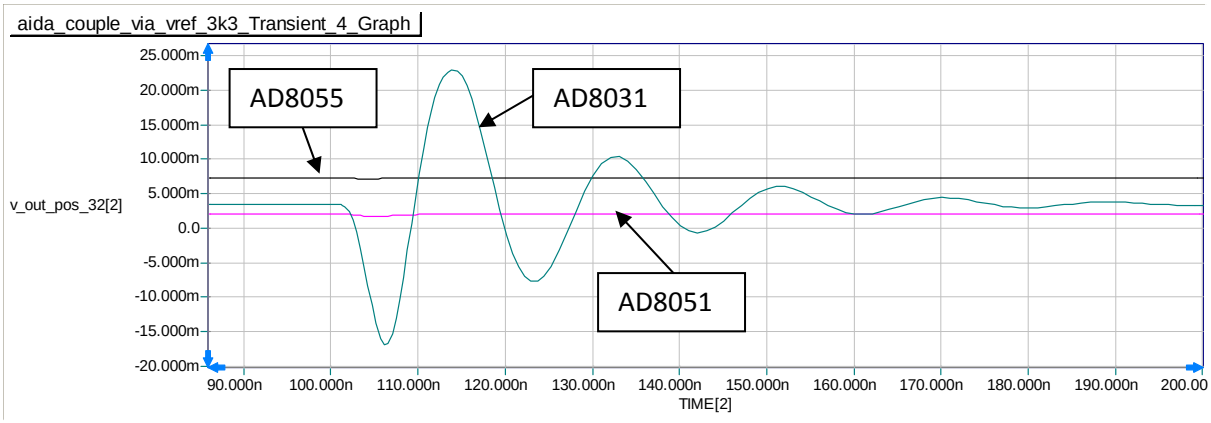
[1] Initial voltage 1.6V, pulse to 2.2V after 100ns delay, 1ns rise time, 100us fall time, 1ms width, 10ms period

other was simulated with a 1.6V DC input from the ASIC and a shared signal from the ASIC Vref buffer to see if there is any interaction between channels.

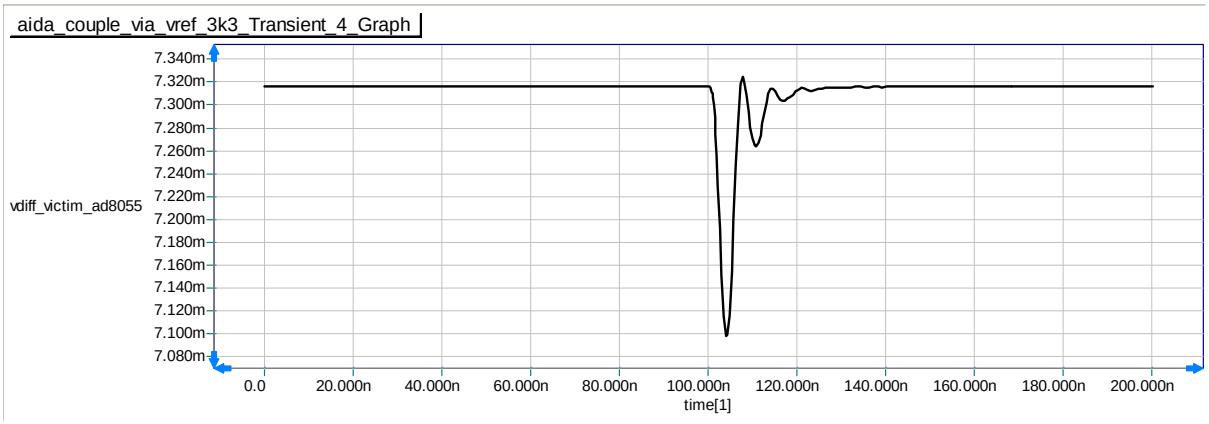
First plot shows the ASIC_Vref_Buf signal with oscillations using AD8031 and with a single (much shorter) excursion after swapping to an AD8055 or AD8051



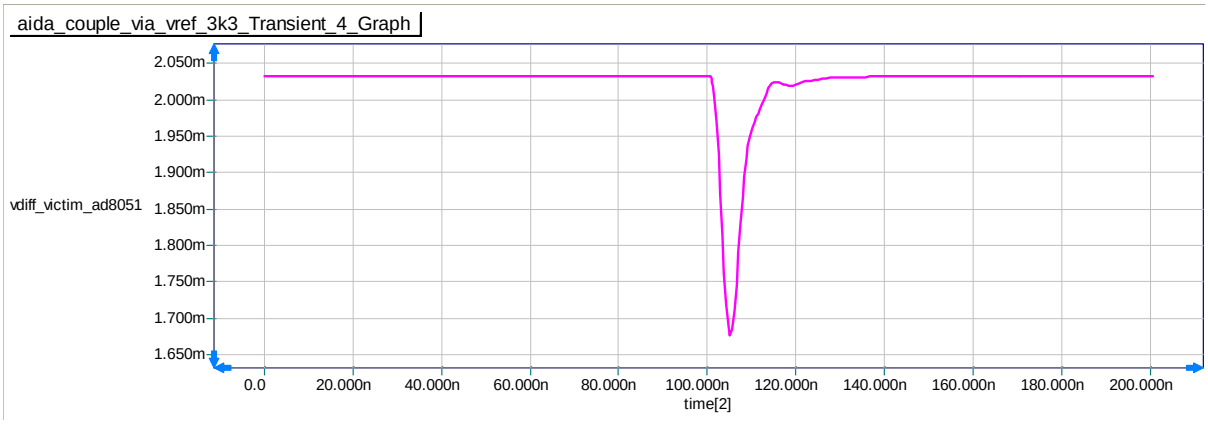
2nd plot shows the differential output of the adjacent channel output affected by the Vref signal in plot 1 when buffering with AD8031 but barely affected when buffering with AD8055 or AD8051



3rd plot shows detail from plot 2 of the adjacent channel when Vref is buffered by AD8055- the crosstalk amplitude is about 0.22mV (AD8031 in plot above is about 20mV).



4th plot shows detail from plot 2 of the adjacent channel when Vref is buffered by AD8051- amplitude is about 0.35mV (AD8031 is about 20mV). AD8051 has lower bandwidth than AD8055 so appears to integrate the crosstalk pulse slightly.



Comparison of AD8031 and AD8055 (operating on dual ±5V supply)

Parameter	AD8031	AD8055	AD8051	Comment
Output current	±15mA	±60mA typ. (min 55mA)	45ma (0.5 to 4.5V out) *(37mA for +5 supply and 0.4Vout)*	30-35mA is needed
Quiescent current	typ 0.9mA	typ 5.4	Typ 4.8mA max 5.5mA	AD8055, AD8051 are significantly worse than AD8031 (however there is only 1 per 16 channels).
Slew rate	32V/us	1400V/us	170V/us	
Bandwidth	80MHz	300MHz	110MHz	Small signal bandwidth Gain +1
Input noise	15nV/√Hz	6 nV/√Hz	16 nV/√Hz	AD8055 adds less noise
Output voltage swing	+4.1V -3V *0.5-4.3V for +5V Vcc*	±2.9min, 3.1typ for 150R (no details)	±4.75V (@30mA) *0.25-4.75V for +5V Vcc*	Taken from 25C graphs, where they have more detail than specs which assume higher loads. AD8055 has no graphs
Power supply rejection	86dB typ	86dB typ drops to 72dB for +Vs +5 to +6V	80dB typ	
Power supplies	+5V or ±5V dual rails	±5V dual rails only	+5V or ±5V dual rails	

Conclusion- AD8055 and AD8051 are both better suited than AD8031 in this application because they offer 3 -4 times more output current and faster slew rate to supply current demands at the diff amp input. There are 2 costs for this benefit- the increased quiescent current (5mA instead of 1mA) and the need for dual supplies instead of single +5V supply if the AD8055 is used (AD8051 can run on +5V/gnd). The price per unit is the same (under $2 in 1000 off quantity) and the packages are the same (SOT RJ-5) although for AD8055 a change of –Vs from 0V to -5V would needed so only the AD8051 is exactly compatible in the current design. However AD8031 could replace an AD8055 after the dual rail modification is made if a retrofit were deemed necessary for some unforeseen reason.

The choice between AD8055 and AD8051 is essentially one of bandwidth and slew rate. The ASIC reference voltage varies only by drifting so very low bandwidth is required for that. However the Vref source must supply currents to the AD4832 to balance the ASIC preamp output changes which have been simulated to have a rise time of 28ns (10-90%) for a 181mV step (therefore the approximate bandwidth is 10-15MHz; slew rate 6.5V/us). The AD8051 is fast enough for this and supplies enough current even for 0.4V Vref (37mA) and runs off the same supply as the AD8031. On paper it seems the best choice, however the simulations shown below suggest that the AD8055 performs better (by 0.6 bits) and should be selected as the buffer of choice with the AD8051 as second choice (for example if the power rail change to add -5V proves difficult).

Alt parts: AD8014- 1 rail current feedback so needs Rf (499-1k)- not drop-in. AD8061- single rail, typ 50mA but min 25mA so probably too weak. AD8065- typ 35mA (no min figure) so probably too weak.

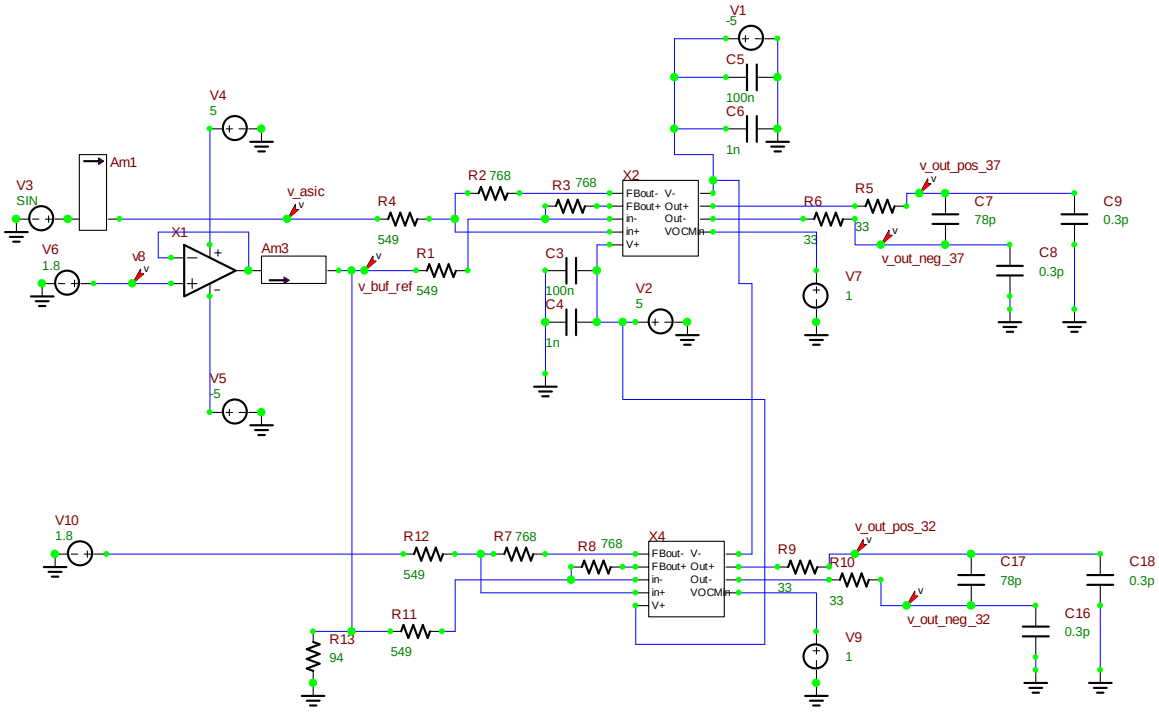
Crosstalk

Despite the huge improvement over AD8031, there is still a small risk of channel to channel crosstalk caused by a channel loading Vref heavily and dragging down neighbours- the extra current significantly reduces this effect (see simulation plots). The only way to avoid the risk entirely is to have 16 buffers per ASIC rather than 1.

The following crosstalk simulations were re-run (rev 5 on 9th Aug 2010) to include AD8051 (alongside AD8055 for comparison) and also a new simulation was included using a piecewise linear pulse from the simulation of the ASIC preamp output driving this load to provide a realistic scenario. Both simulations (sine wave and PWL ASIC output) were run on the circuit with gain as calculated in section 4.

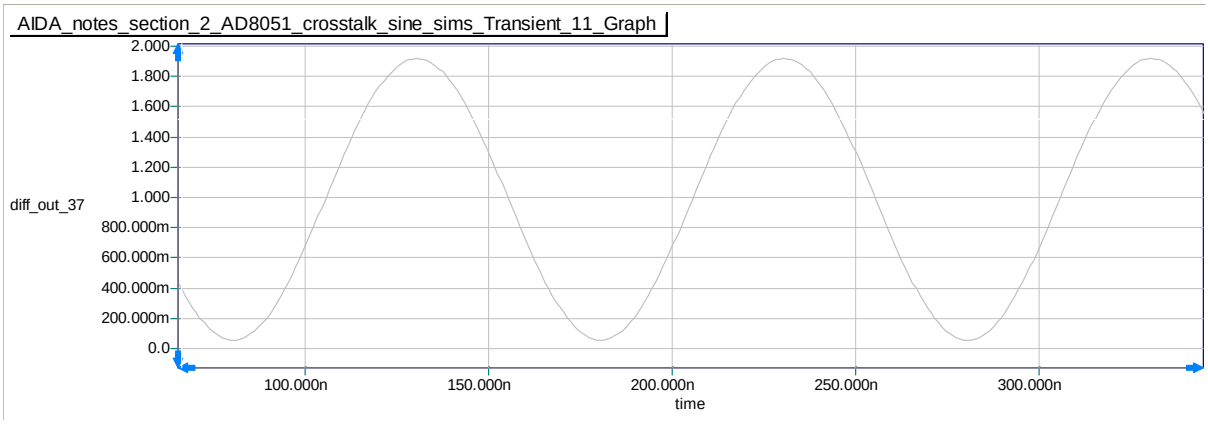
Updated (Gain x1.4) and PWL pulses simulation of crosstalk via Vref (updated rev 5, 9th Aug 2010)

Put in 1.4Vpk-pk 10MHz sine wave (centred on 1.1V) to 1 channel and left the other with 0.4 or 1.8V DC input. (Plots and results taken with 0.4V Vref). Both amplifiers are ADA4932's and share the same Vref from AD8051/AD8055 (1.8V). Also Vref is loaded by 94R to ground to emulate 14 more channels.

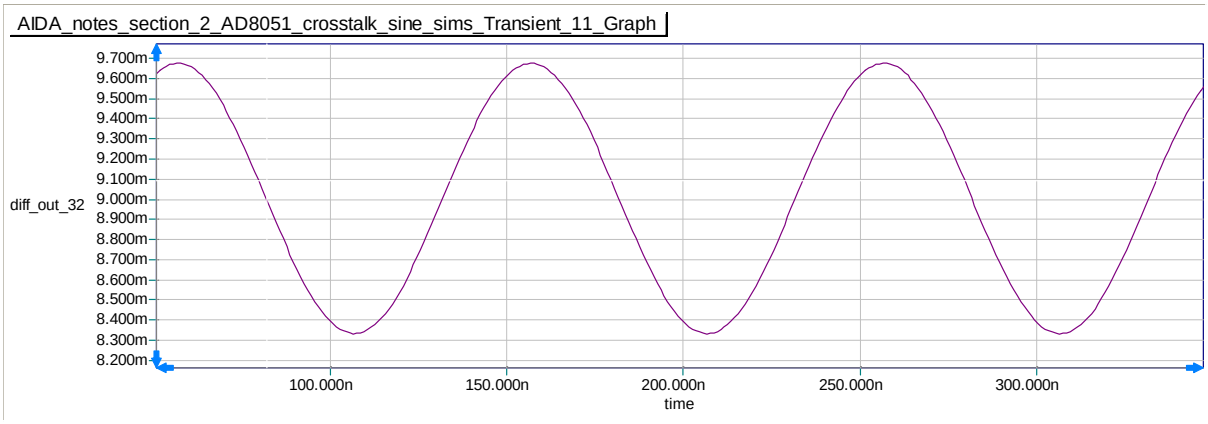


Emulate 14 more channels @549+768=1317R to ground to test loading

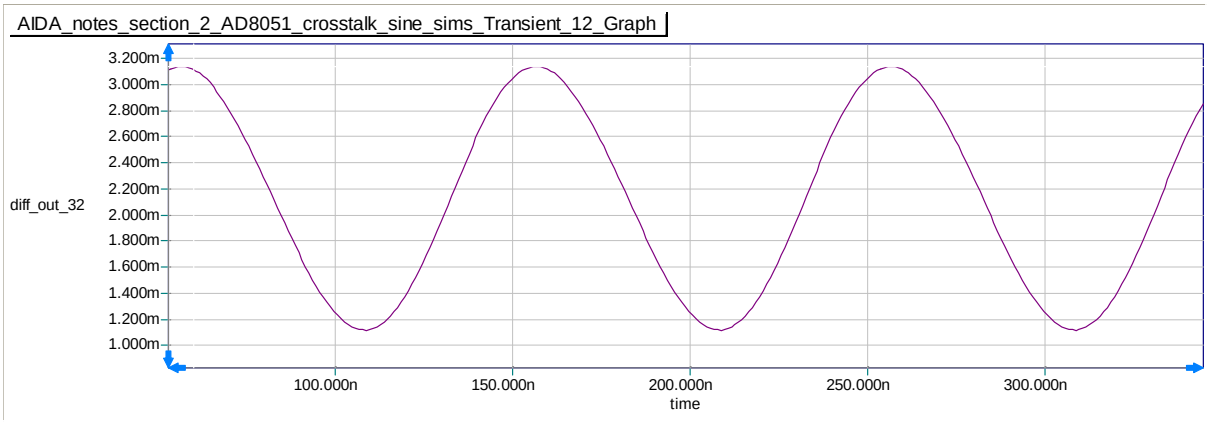
Plot below shows the output of the top amplifier in response to the 10MHz 1.4V pk-pk sine wave (1.86V pk-pk output).



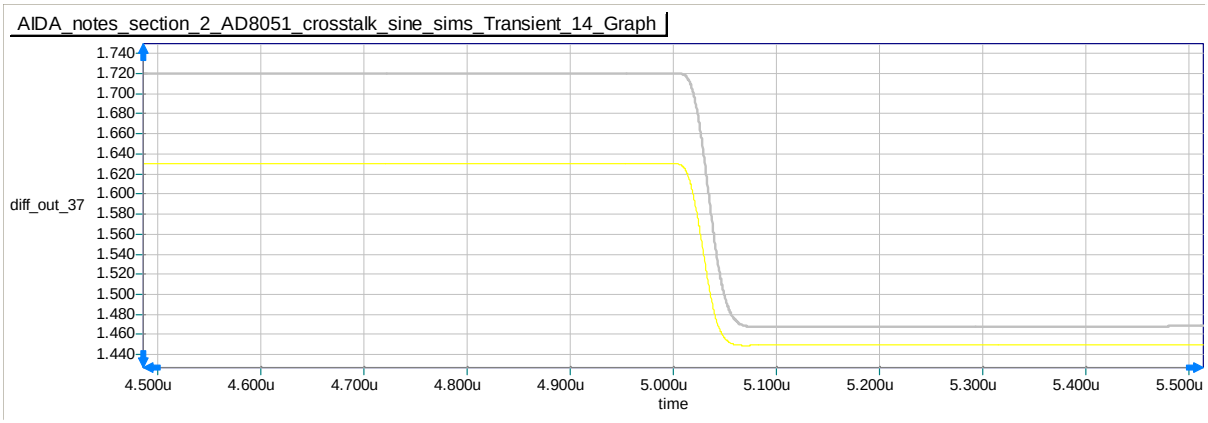
Plot below shows the output of the lower (victim) amplifier in response to the crosstalk on Vref induced from the top channel following a 10MHz 1.4V pk-pk sine wave with AD8055 buffer on Vref. Crosstalk amplitude is 1.343mV= 0.07% (10.4 bits).



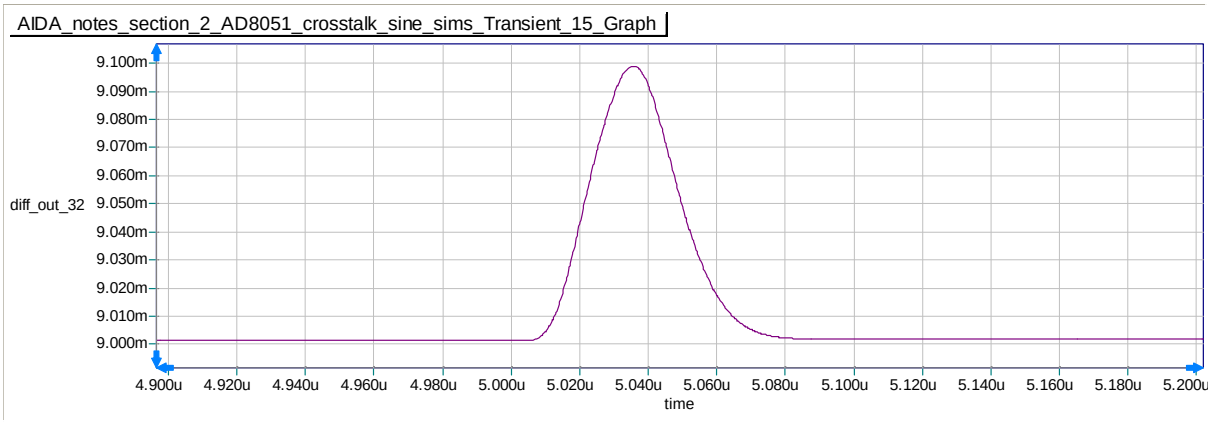
Plot below shows the output of the lower (victim) amplifier in response to the crosstalk on Vref induced from the top channel following a 10MHz 1.4V pk-pk sine wave with AD8051 buffer on Vref. Crosstalk amplitude is 2.019mV= 0.11% (9.8 bits).



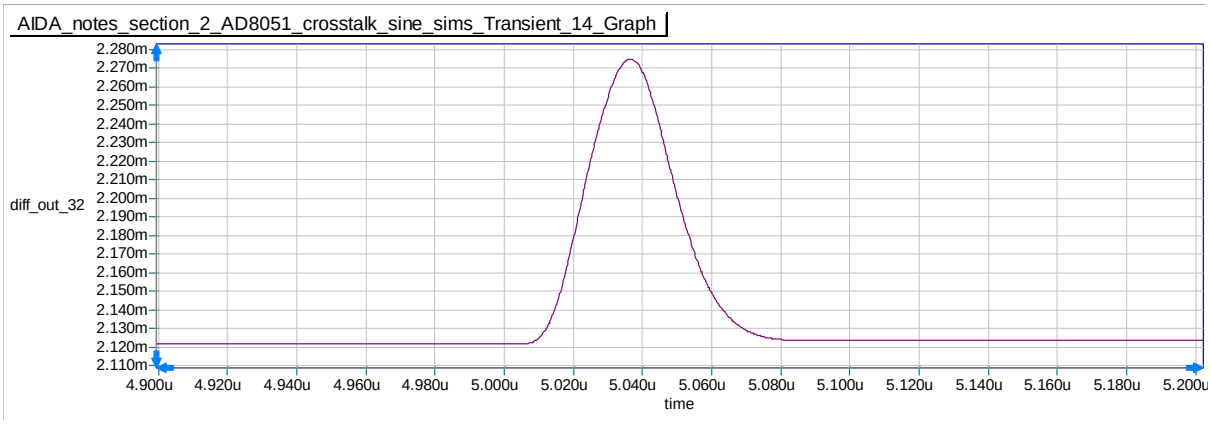
Plot below shows ASIC PWL pulse shape (yellow) and output of the top amplifier (grey)- the input signal has a step of 0.18V from 1.63 to 1.45 and the output has a step of 0.25V from 1.72 to 1.47V



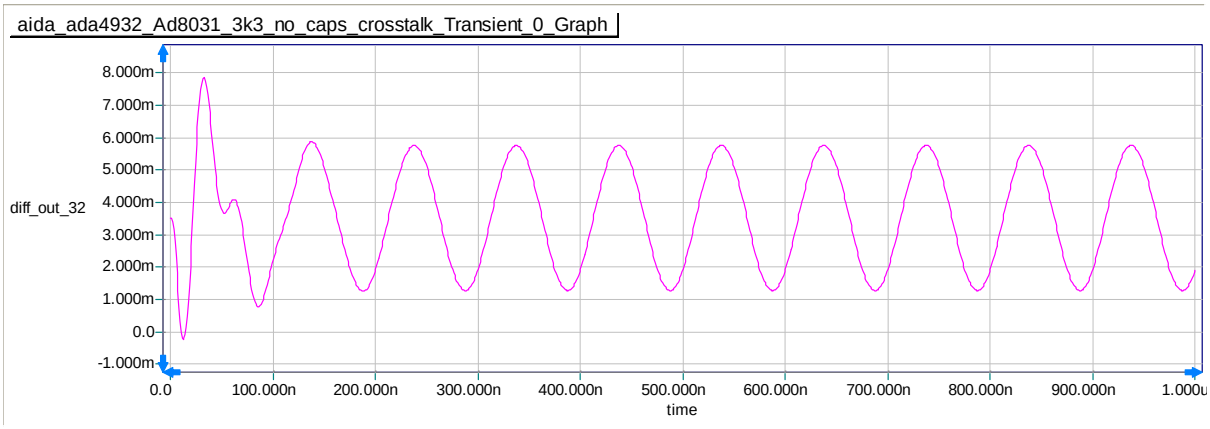
Plot below shows response in the lower (victim) channel to the Vref perturbation caused by ASIC PWL pulse shape making the output of the top amplifier output step 0.25V while Vref is buffered by an AD8055 buffer. The crosstalk pulse height is 0.098mV (0.04%; 11.3 bits).



Plot below shows response in the lower (victim) channel to the Vref perturbation caused by ASIC PWL pulse shape making the output of the top amplifier output step 0.25V while Vref is buffered by an AD8051 buffer. The crosstalk pulse height is 0.153mV (0.06%; 10.7 bits).



Finally, as a comparison, went back to AD8031 instead of AD8055, 3k3 resistors and load resistor 471R to emulate 14 more channels and match prototype (except for AD4932 diff amps). Amplitude out is 1339mV and adjacent channel crosstalk is 4.47mV pk-pk (0.33%, 8.2bits) (see below). This is consistent with Bill Helsby's measurement of 20 channels crosstalk in 4000 (0.5%).



Section 3- Notes on system bandwidth

Bandwidth analysis of AD4932 diff amp ADC driver circuit.

Initially (in the prototype) the bandwidth was severely limited (4.8MHz) by using 3k3 feedback resistors with 10pF in parallel. Removing (reducing) the 10pF has been tried in the prototypes as has reducing the 3k3 resistors back into the recommended range (330R). All these have affected the bandwidth and stability of the circuit. However, the switch to AD4932 diff amps brings a new set of recommended values (R_f, R_g = 499R for unity gain) and the analysis below uses the default values and looks at 2 different values of the capacitor across the 2 output resistors which forms a low pass filter prior to the ADC. (2^{nd} value, total 78pF, comes from Bill Helsby's suggestions).

Results from calculation and from Spice analysis are shown.

Calculation

Using 499R resistors for gain and feedback (no capacitors) the bandwidth is determined by the LPF at the output (2 x series 33R and parallel 10pF/78pF).

$Fc = 1/2\pi RC = 1/(2\pi \times 66 \times 10 \times 10^{-12}) = 241MHz$ (10pF)

or

$Fc = 1/2\pi RC = 1/(2\pi \times 66 \times 78 \times 10^{-12}) = 241MHz$ (78pF) =31MHz.

Spice

Spice frequency sweep confirms these values (30MHz and 240MHz) as the 3dB points.

Without C_{load} the 3dB point for the frequency sweep of the rest of the circuit is 475MHz

Section 4- Adding gain to the diff-amps to use full FADC range.

ASIC Preamp Output

The ASIC pre-amplifier output range is 0.4 to 1.8V with a reference range 0.2-0.6V or 1.6-2.0V depending on the charge polarity and hence whether 0.4V (neg charge) or 1.8V (pos charge) represents "0".

Diff Amp output

Output of the ADA4932 depends on the inputs: when in+ (ASIC input) = in- (vref), both Vout+ and Vout- are = +1V (Vocm). If in+ is > in- the Vout+ becomes >1V by half the difference and Vout- becomes less than 1V by half the difference.

Assuming that Vref is set such that the values of Vout+ and Vout- are never below 0 (i.e. Vref is either 0.4V or 1.8V) then the following values can be calculated.

Vin+ (ASIC)	Vin- (Vref)	Vout +	Vout-	Vout diff
1.8V	1.8V	+1V	+1V	0V
0.4V	1.8V	+0.3V	+1.7V	-1.4V
1.8V	0.4V	+1.7V	+0.3V	1.4V
0.4V	0.4V	+1V	+1V	0V

(Note- simulation shows delay of about 7.5ns between input and output)

FADC Input

The FADC (AD9252) input range is 2V differential pk-pk with Vref = 1V so maximum range is 0 to 2V on either input (±1V from +1V vref) (absolute limits of AD9252 inputs are -0.3V to +2.0V).

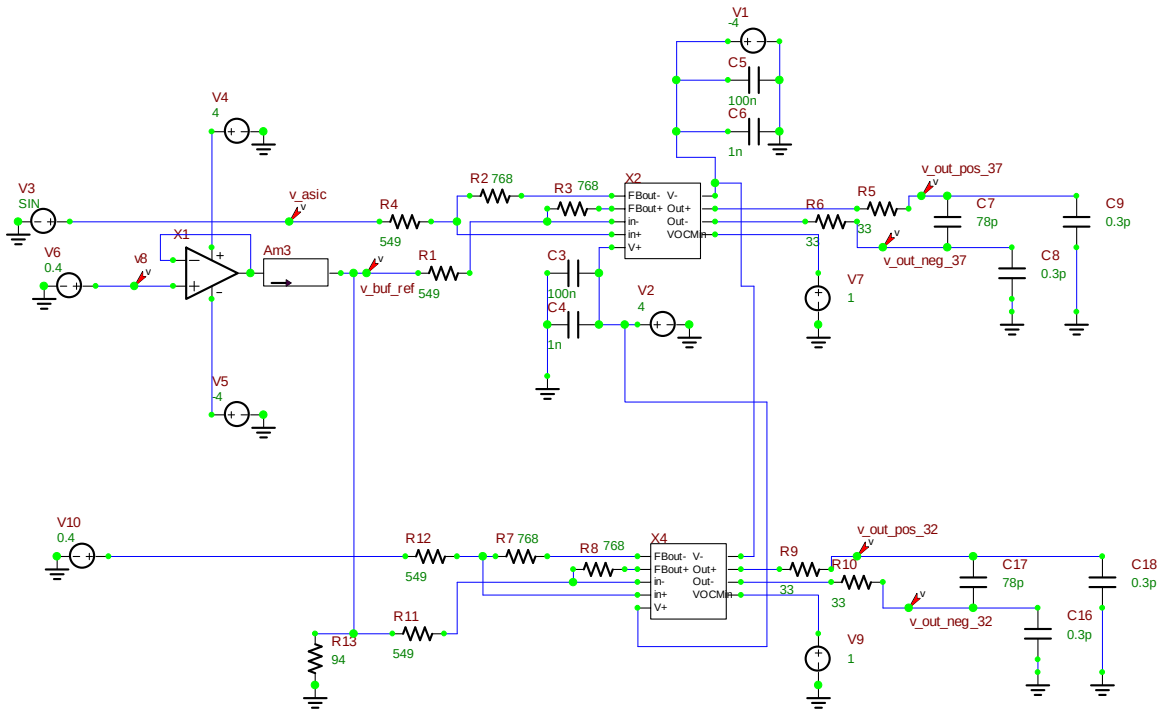
In order to use the full ADC input range it is necessary to add gain of 1.4 (2/1.4) to the diff amp.

Results in the table below were measured in simulation after implementing the gain change using values calculated in the next section:

Vin+ (ASIC)	Vin- (Vref)	Vout +	Vout-	Vout diff
1.8V	1.8V	+1.005V	+1.003V	+0.002V
0.4V	1.8V	+0.032V	+1.970V	-1.938V
1.8V	0.4V	+1.980V	+0.020V	+1.96V
0.4V	0.4V	+1.01V	+0.99V	+0.02V

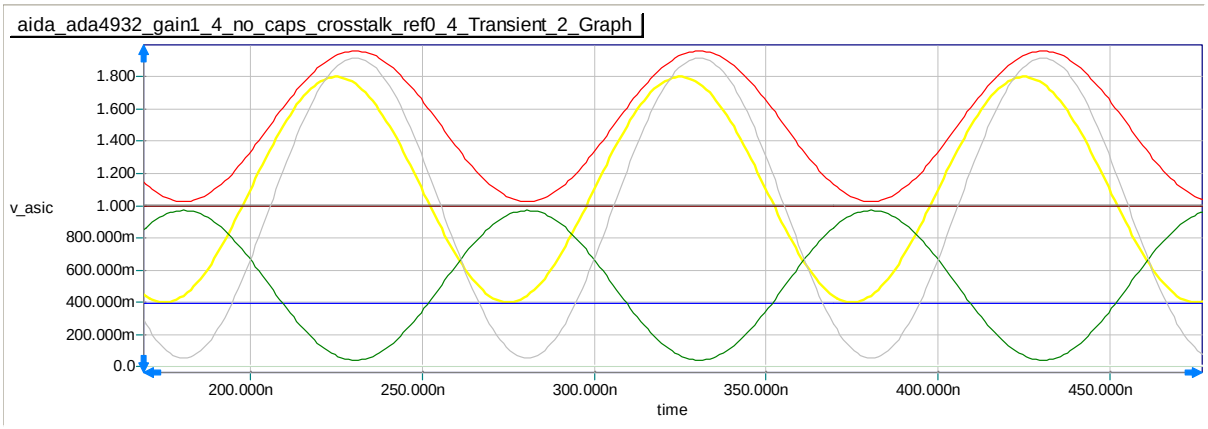
Change to diff amp (AD4932) to introduce gain of 1.4.

Gain = R_f/R_g and values of R_f suggested in the data sheet are 499R and 768R (R_G 499R to 243R). To get gain of 1.4 and assuming R_f = 768R then R_g = 768/1.4 = 549R



Emulate 14 more channels @549+768=1317R to ground to test loading

Simulation confirms that these values are correct.



Yellow trace is ASIC preamp input (0.4 to 1.8V); blue trace is Vref (0.4V), red trace is Vout+; green trace is Vout- and silver trace is Vdiff.

Crosstalk check in simulation- Vdiff for active channel is -36.5mV to -1.900V = 1.864V and Vdiff for adjacent channel is 10.39 - 9.00 = 1.39mV so crosstalk is 0.075% (10.4 bits)- no change. This crosstalk is the same for both 0.4V and 1.8V Vref values.

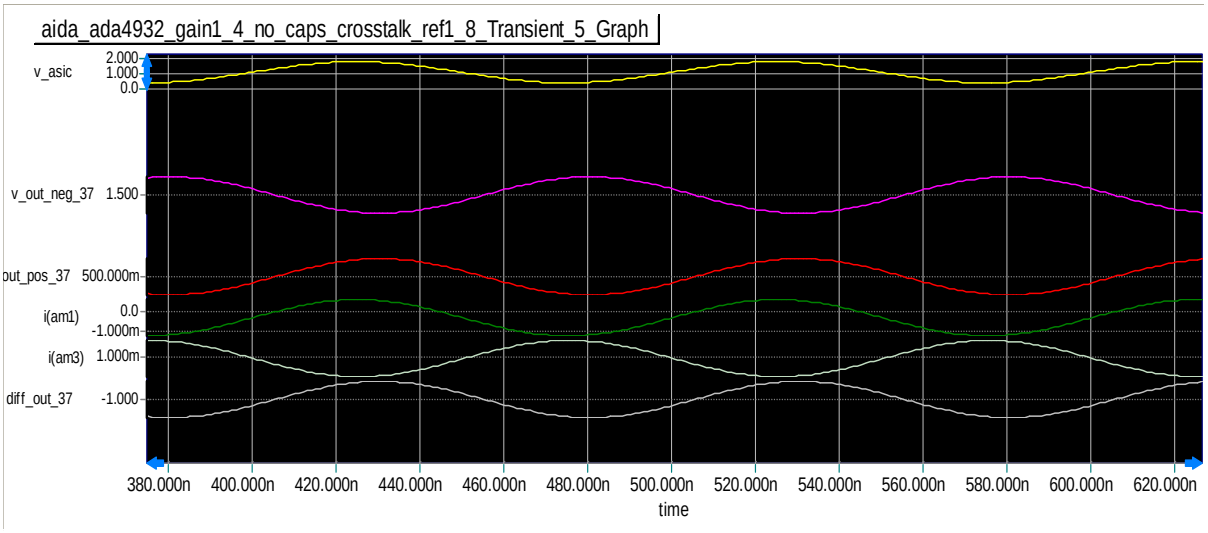
Section 5- Operating at lower supply voltages- section probably obsolete now (rev 3 onwards) moved to appendix C

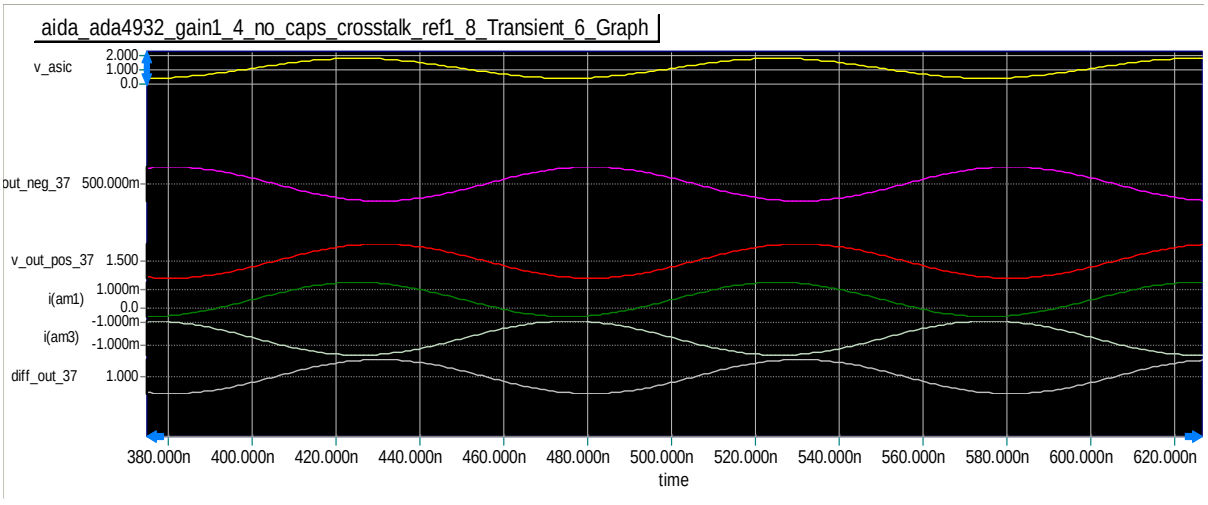
Section 6- Possibility of additional buffers to provide high impedance load to the ASIC

The load on the ASIC buffers can be determined from spice simulation. The spice simulator shows that ASIC must sink 1.2mA for a 0.4V output and source 600uA for 1.8V outputs (when V_{ref} = 1.8V). When V_{ref} is 0.4V, the ASIC must source 1.35mA for 1.8V output pulses and sink 0.45mA for 0.4V outputs. *See section 8 for further comments on variation of current load on ASIC preamp output.*

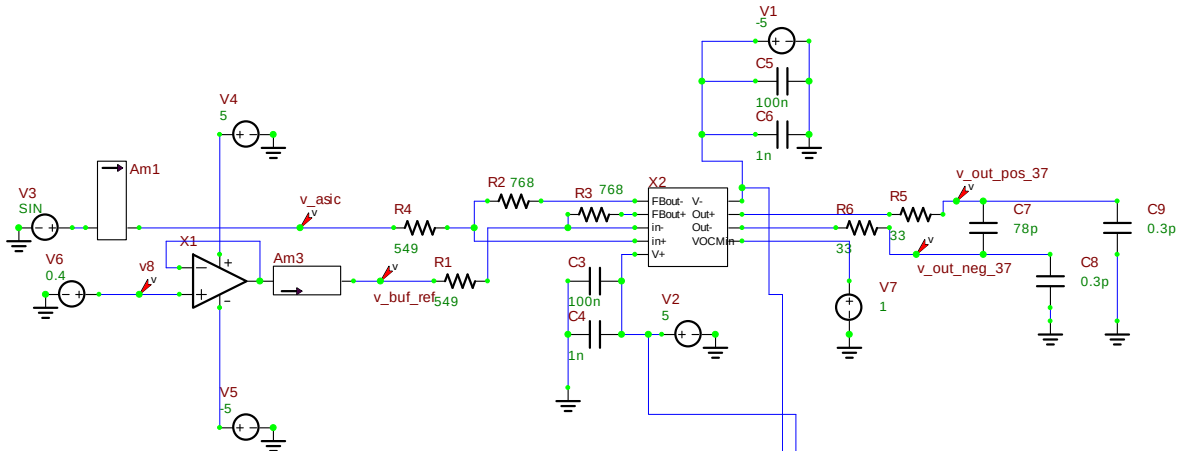
(V_{ref} current sinking varies out of phase with the ASIC preamp output: for V_{ref} of 0.4V it sinks between 0.4mA and 1.2mA and for V_{ref} of 1.8V it sources between 0.6 and 1.35mA.)

In the plots below, V_{asic} varies from 0.4 to 1.8V; am(1) measures the current sourced or sinked by that voltage source and am(3) shows the current sourced or sinked by the V_{ref} buffer. Other signals shown are Vout_neg and Vout_pos from the diff amp and also the difference between those (diff_out). In the top plot V_{ref} was 1.8V; in the bottom plot V_{ref} is 0.4V (despite the plot name) and in both cases only 1 diff amp was driven by V_{ref} as shown in the circuit below.





Circuit diagram used for simulation (in this case V_{ref} is set to 0.4V)



Rev 5 (9th August 2010)- Steve has confirmed that in simulation the ASIC can operate successfully with this circuit, sinking or sourcing up to 1.3mA.

~~If the ASIC is unable to sink/source 1.3mA per channel then we need to consider putting buffer amps on the mezzanine card, as close as possible to the ASIC. The key specs are the size, bandwidth to match ASIC preamp (rise time typically 90ns so bandwidth approx 4MHz)[2] and preferably low power, low noise.~~

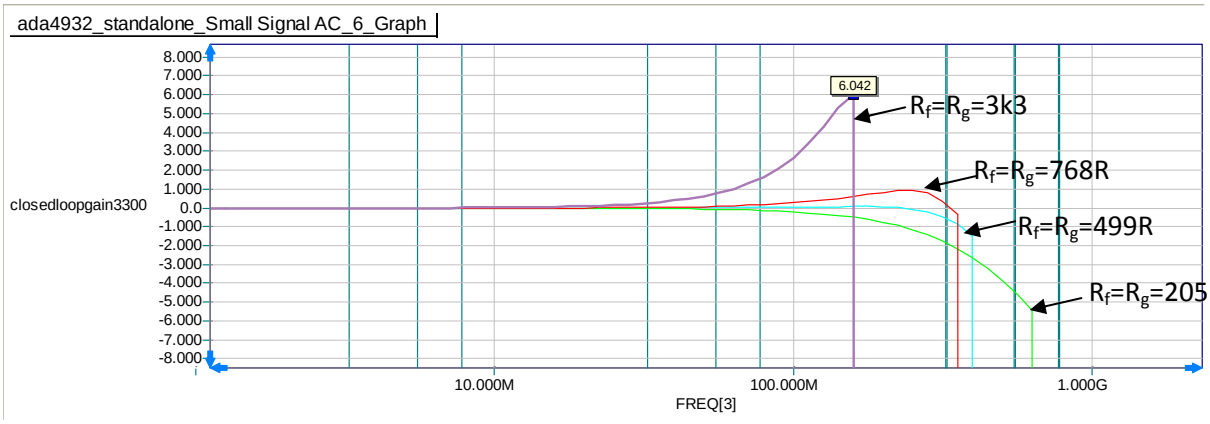
~~While improving system integrity this change would also increase cost of parts (est £55 extra per mezzanine based on £1.38 OneCall 250 off price for AD8030), increase power budget (estimate about 0.2A/mezzanine) and increase board size (hard to estimate, maybe additional 8x2cm area??) as well as taking time and design effort. So it should only be implemented if we are convinced it is really necessary. Appendix B shows some possible buffers if this option is needed.~~

~~An alternative would be to operate the diff amp outside the recommended feedback and gain resistor values, but given the problems this is causing on the prototype I would suggest that the best option is to leave the diff amp configured as suggested by Analog Devices.~~

[2] *Do we need higher bandwidth to keep up with the ADA4932 diff amp if it picks up noise from power rails or elsewhere outside bandwidth of preamp? (c.f. voltage buffers are 300MHz although partially because this comes with the part which can meet drive requirements).*

Section 7- Checking ADA4932 stability

Spice simulation of various feedback and gain resistors (closed loop gain) with Vin = 1.1 ±0.7V (plots show $20Log_{10}(V_{diffout}/V_{in})$)



Purple = 3300R; Red = 768R; Light Blue = 499R; Green = 205R

The closest equivalent plot in the data sheet is for 2Vpk-pk input:

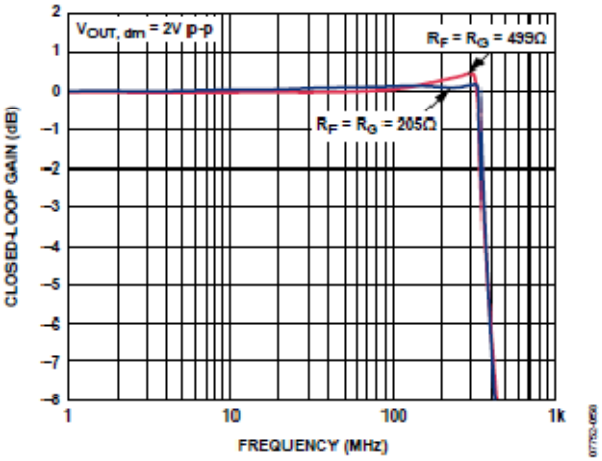
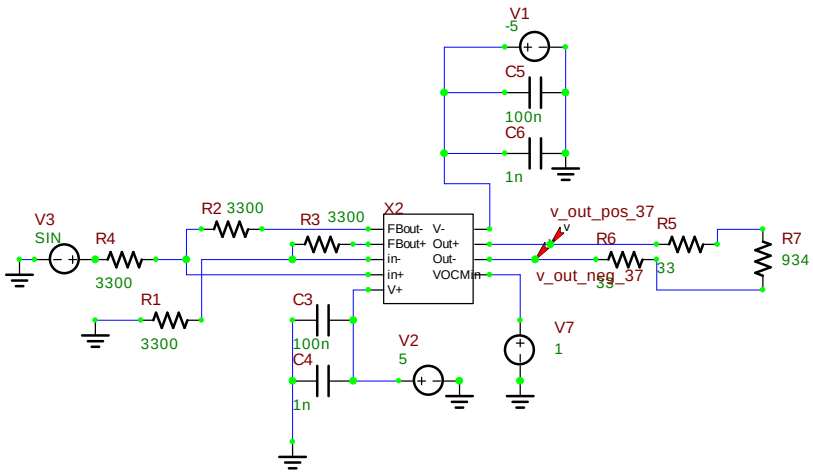
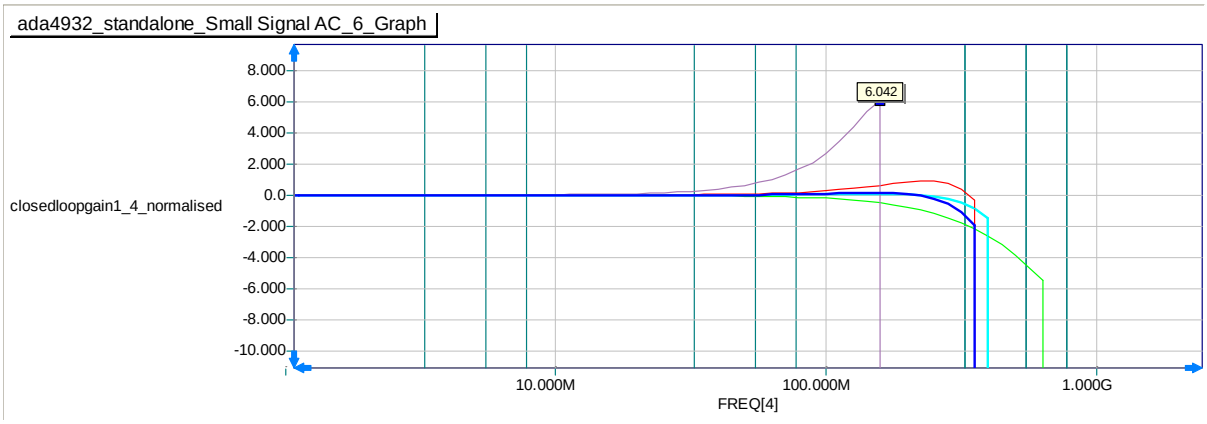


Figure 11. Large Signal Frequency Response for Various R_F and R_G



Simulation circuit (3k3 run)

Simulation with the gain 1.4 values of resistors R_f=768R R_g=549R (Vin = 1.1±0.7V)



Purple = 3300R; Red = 768R; Light Blue = 499R; Green = 205R, Dark Blue = gain 1.4 values (768/549)

This plot shows the normalised closed loop gain plot of the planned x1.4 gain in dark blue superimposed on the unity gain plots with various resistor values obtained earlier. The dark blue plot is pretty much flat until it drops away at 350MHz (499R/499R unity gain plot in light blue is very similar and flat until it drops away at 400MHz).

Section 8- Calculating input impedance:

From AD data sheet formulae:

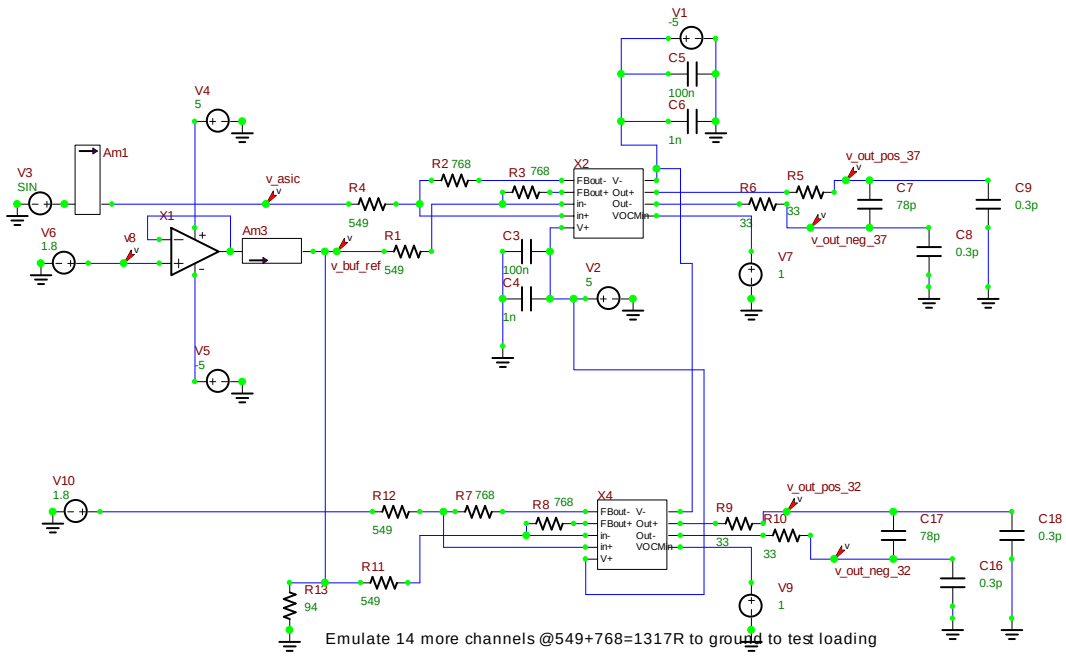
The input impedance between the 2 terminals on a balanced diff amp = 2 × R_G

The input impedance for one side (unbalanced single ended) = $\frac{R_G}{1-\frac{R_F}{2\times(R_G+R_F)}}$ which gives the following values:

R_F	R_G	Diff Z_{in}	SE Z_{in}
499R	499R	998R	665R
3k3	3k3	6k6	4k4
768R	549R	1098R	775R

I think that the SE impedance calculation should still be valid for calculating one leg of a balanced differential configuration when used in our configuration (which is more like 2 single ended configurations that 1 balanced input).

The input impedance is affected by the output common mode voltage of which a fraction feeds back to the diff amp inputs via R_F in a ratio determined by R_F and R_G. So the diff amp In+ and In- pins don't act as a virtual earth, but as a virtual fraction of V_{OCM} which changes the voltage drop across R_G. For the ASIC buffering this is more important than the calculated impedance because it controls the input current. For example no current is drawn when V_{ASIC}-V_{ref} = V_{OCM} × $\frac{R_G}{(R_F+R_G)}$ so in the case below we have no current when V_{ASIC}-V_{REF} = -1 x $\frac{549}{(768+549)}$ = -0.4V which matches simulations in section 6.



Section 9- Change to multiplexer ADC and gain change in associated buffer circuit

Reasons for changes-

1) to try to improve throughput/reduce inter-event gaps by using a faster ADC
2) to optimise the use of the ADC range.

ADC Change
The first change in this area is that the 16 bit ADC (500ksps) AD7686 should be replaced by a faster 16 bit ADC so that the inter event gap can be reduced and throughput improved.

Obvious candidates are the pin compatible AD devices (AD7980: 16 bits 1Msps; AD7982: 18 bits, 1Msps; AD7984: 18 bits, 1.33Msps).

The sequence of operation is that the ADC has an acquisition phase followed by a conversion phase (of variable length within defined limits). There is a busy output from the ADC to indicate that conversion is taking place. After conversion (during the next acquisition phase) the ADC data is read over a serial data connection using a VHDL state machine. The limits to the processing time are firstly the settling time of the ASIC output and buffer to 0.0015% (currently the buffer settles within 615ns) and secondly the ADC readout time (requires 17 clocks for the data and a few more for the state machine to test busy and start readout when it goes away). The ASIC mux output is changed on the ADC clock rising edge, so 615ns later (+ASIC settling time) the ADC may start conversion. In the AD7686 the conversion lasts between 0.5 and 1.6us- in the analysis we must assume 1.6us. The acquisition phase lasts 400ns and the fastest permissible clock for readout of the ADC data is 18ns (the state machine actually uses 20ns clock, so 17 readout clocks take 340ns leaving 3 clocks to start/end the readout sequence in the state machine). The ASIC output settling time takes place during the previous conversion time and so there is scope to reduce the conversion time down to about 715ns (allowing 615ns for the buffer plus 100ns for the ASIC output delay/switching). The acquisition phase can only be reduced if the ADC readout clock is speeded up. The limit on settling time (715ns) limits the ADC conversion speed and precludes the use of the 1.33MSPS AD7984 which has a maximum conversion time of 500ns- in this case the input would not be stable in time. The fastest possible parts are the 1MSPS parts (AD7980, AD7982) which have a maximum conversion time of 710ns which matches the settling time.

The AD7980 uses the same pseudo differential input as the AD7686 (in- must be within ±0.1V of 0V) whereas the 18 bit ADCs (AD7982, AD7984) are true differential inputs and would require a change of buffer/common mode circuit (AD8250). The AD7982, AD7984 data sheets recommend various analogue buffer drivers, but none of the recommended parts specifies a 0.0015% or better settling time (the AD8250 data sheet specifies a maximum time for 0.001% settling). The closest is the AD4941 which specifies only a typical time for settling to 0.005% (14 bits) of 300ns using 3V supplies; 600ns typ for 5V supplies and it has a minimum gain of 2. It is sold as an 18 bit ADC driver, but the AD4941 data sheet's list of typical applications has ADCs with 250-400ksps, not 1Msps. Therefore select AD7980 to avoid the need to redesign the input buffer to be differential since even the AD recommended differential ADC drivers are not fast enough. The best available buffer seems to be the AD8250 in the existing circuit which matches well with the AD7980.

Note- the AD7980 is available in both A and B grades- the B grade should be used because it has significantly better DNL and INL specs than both the A grade and the C grade AD7686 used in the prototype.

The acquisition time of the AD7980 is 290ns with conversion taking between 500ns and 710ns. The readout must happen during the 290ns acquisition time for the next input. The min SCK Period (CS

Mode) for Vio between 3 and 4.5V (we use 3.3V) is 12ns- assume we use 80MHz (12.5ns) then in the 290ns acquisition period there are 17 clocks for data readout (212.5ns) leaving 6 clocks for the state machine to recognise and clean up after readout (if a 12ns, 83.33Mhz clock is used this can becomes 7 extra clocks after a 204ns readout period).

The ASIC output and buffer must settle to 0.0015% within 710ns (i.e. prior to the acquisition phase) and the amplifier (if affected) must recover from the ADC switching between conversion and acquisition so that the value presented to the ADC is correct to 0.0015%.

The AD8250 specifies its settling time to 0.001% for a 10V step which is better than 16 bits accuracy and also a much larger step than the ASIC can make. The AD8250 remains a suitable part for the ADC buffering, especially as it can incorporate the 2.048V common mode voltage needed for the "pseudo differential" ADC input. Since the in- pin is actually grounded on the FEE card the ADC input is not really pseudo-differential; it is single ended with an offset to the middle of the reference voltage to allow a 0-4V ADC input to work with ±2V signals.

AD8250 buffer gain

The AD8250 driving the AD7686 ADCs is currently set to a gain of 1 and doesn't use the full ADC input range.

AD7686 allowable input range is 0 to V_{ref} (V_{ref} is set to 4.096±0.005V externally using ADR444; the allowable range is 0.5 to V_{dd} + 0.3V, i.e. 0.5 to 5.3V so this is a safe value, allowing for the ADR444 reference and ADC to both use the same 5V supply.) The in- pin is grounded so the "differential" input voltage is actually the single ended input applied to in+ by the AD8250 through a 1.8MHz low pass filter (33R , 2.7nF).

The AD8250 gain is programmed by 2 gain pins, A0, A1 and a /WR write signal (pins A0, A1 are effective directly is WR is set to -15V for transparent mode or else the level on pins A0, A1 is latched by a +5V to 0V transition on /WR. Power up default is 00 which is gain of 1.) At the moment in the circuit the gain is forced to 1 by holding /WR on a +5V supply. If more gain (e.g. gain 2) is required then /WR must be disconnected from +5V and connected to a controllable logic signal and also A0 needs to be disconnected from ground and connected either to +5V (to always have gain 2) or to a controllable logic signal to allow selection between gain 1 and 2 (gains 5 and 10 become possible too if A1 is also connected to a logic signal instead of ground). Logic levels here are defined as 0 for ±<2.1V and 1 for >2.8V.

The input to the AD8250 comes from the ASIC multiplex output (in-)and its associated sh_ref signal(in+) so the differential voltage is (ASIC sh_ref – Aout.) The ASIC sh_ref voltage is typically 1V for +ve charge (mux out voltages 1V to 2.4V giving differential voltages 0 to -1.4V). The sh_ref voltage is set to 2.4V for –ve charge (mux voltages 2.4V to 1V giving differential voltages of 0 to to +1.4V).

The AD8250 Vref pin is driven from a 2.048±0.003V reference (ADR440) which offsets the AD8250 output by 2V. So the AD8250 takes differential inputs in the range -1.4V to 0 and 0 to +1.4V, offsetting these by 2.048V to that 0 is in the ADC mid-scale, driving approx. 0.6V to 3.4V.

Only part of the ADC range is used because the AD8250 passes on the ASIC output with no gain so only 70% of the range is used. Ideally a gain of 1.4 would be applied in the AD8250, but it cannot do

that. The best method of obtaining a gain of 1.4 would be to set the AD8250 to gain of 2 and then use attenuation network on either output or input. It is better to put attenuation on the output than the input (lower noise) but the LPF and the output drive capability might cause a problem.

Check AD8250 output range (in schematics it runs from ±5V)- no useful data in specifications (±13.5V with ±15V supplies). Fig 32 shows output swings for other supplies (but note gain =10 and load = 2k). At 25C and 5V supplies the swing is to within 0.8V of -5V rail and 0.9 of +5V rail. Increasing gain to increase from 1.4 to 2V out changes the range from 0.6 to 3.4 and makes it 0 to 4.0V which is within the limits of the device. Fig 34 shows the effect of current on output swing- the present configuration can draw up to 15mA but the higher gain would be limited to 2mA. Check current load in simulation.

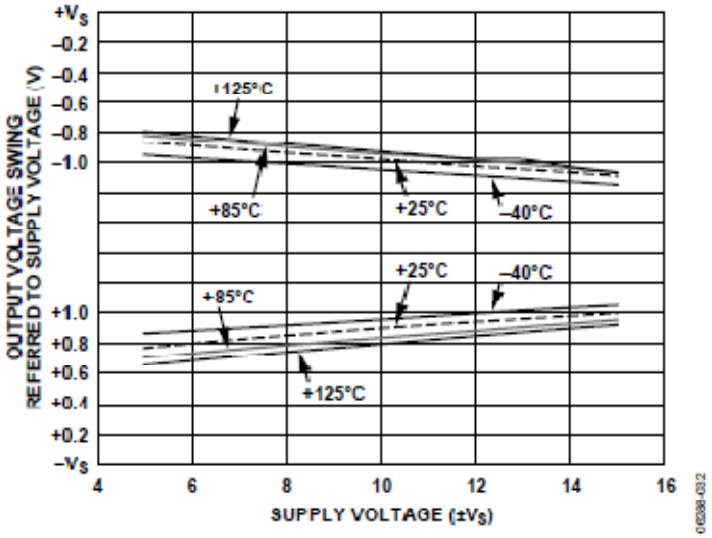


Figure 32. Output Voltage Swing vs. Supply Voltage, G = 10, R_L = 2 kΩ

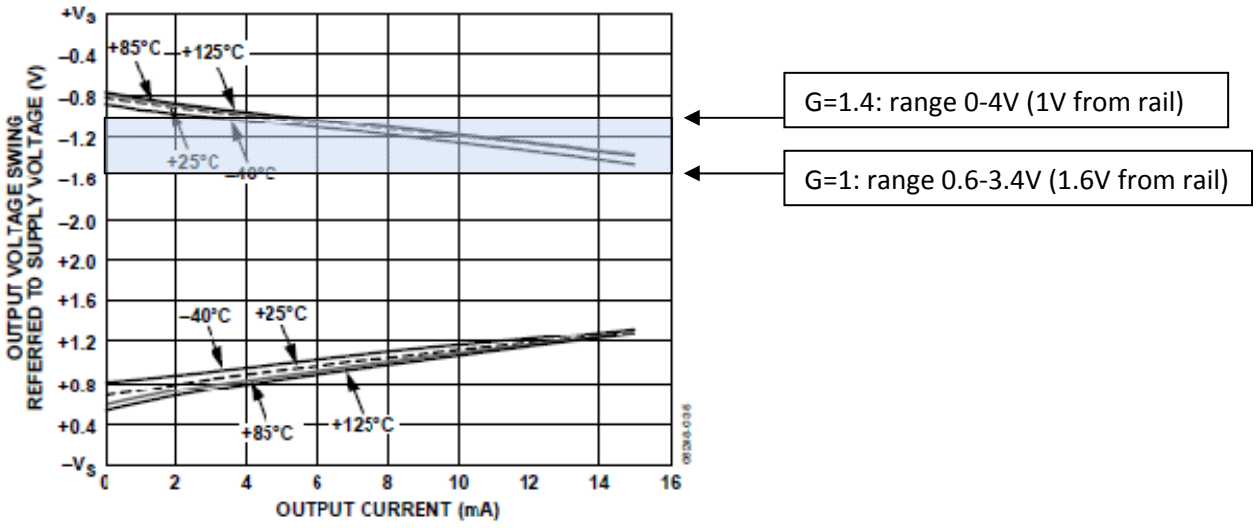
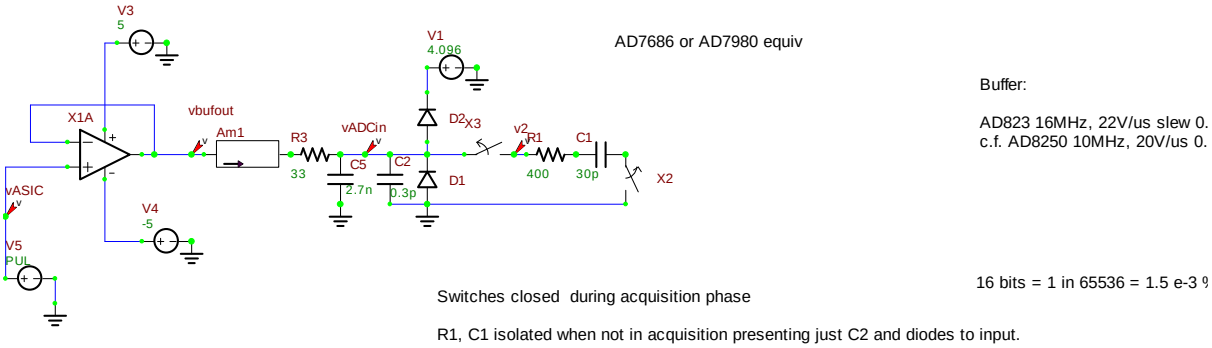


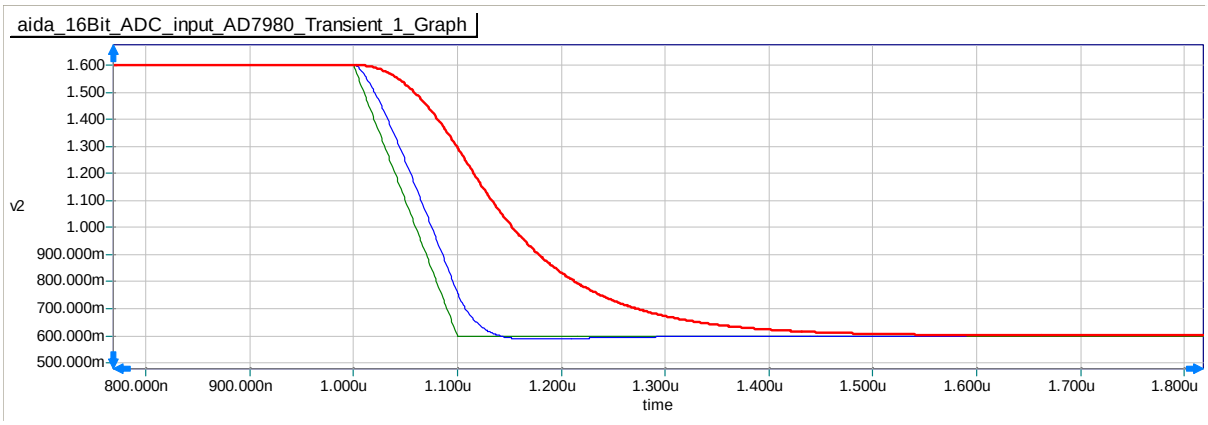
Figure 35. Output Voltage Swing vs. Output Current

There is no Spice model for the AD8250 (or the similar AD8251 and AD8253) so I simulated using an AD823 which was the closest match I found based on slew rate (22V/us compared to 20Vus in AD8250) and settling to 0.01% (650ns for 2V step on ±15V supplies compared to 580ns in AD8250) and bandwidth 16MHz (AD8250 10MHz).

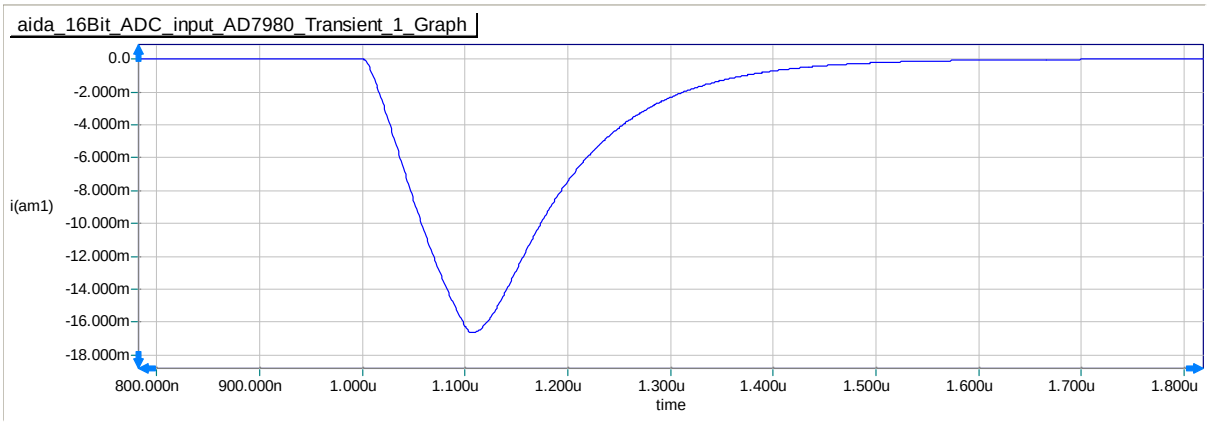
Low pass filter in front of the ADC is not for aliasing, just for noise reduction so changing sample rate should not affect the 33R, 2.7nF 1.8MHz LPF (R3, C5) ADC data sheet gives an equivalent circuit (400R and 30pF, R1, C1) which can be simulated with the AD823 buffer as below. (1V step 1.6-0.6V)



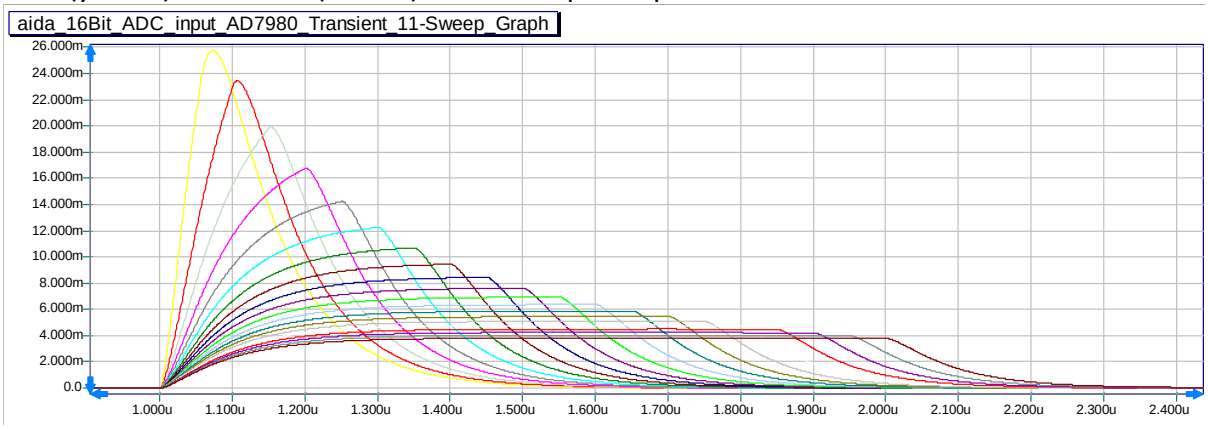
Plot showing Vasic (green), Vbufout in blue (before the filter) and V2 (at the ADC's sensing capacitor) in red (superimposed on Vadcin which is hidden below it).



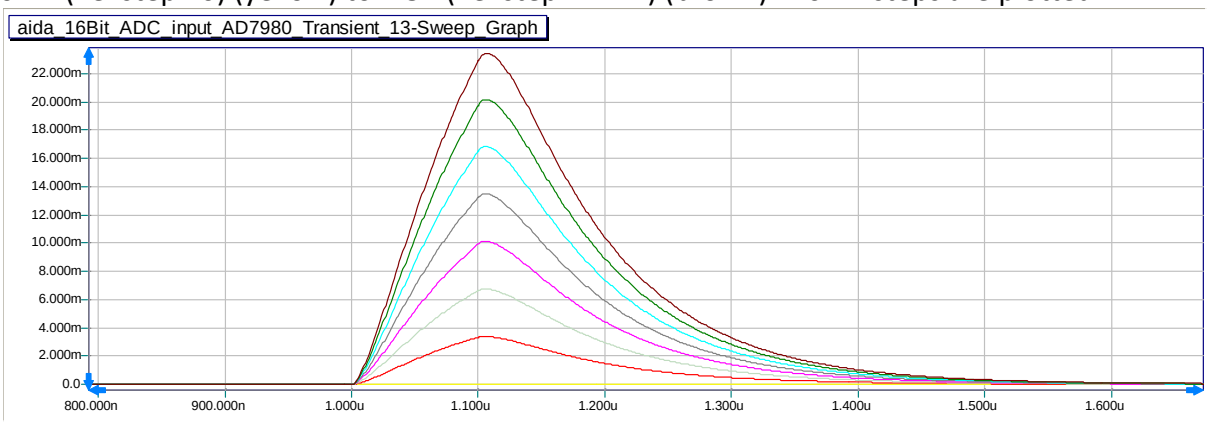
The plot below shows that the AD8250 must sink up to 16mA while tracking the input pulse (the current is proportional to size (and rise time) of the pulse; sink/source determined by its polarity).



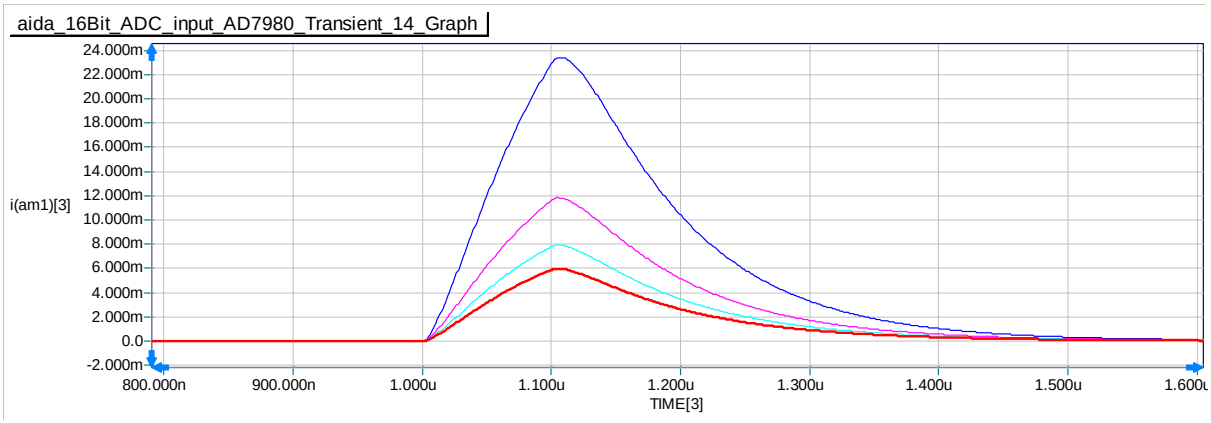
Plot of the effect of input rise time on current drawn from buffer amplifier (all input pulses are 0.4 to 1.8V- the maximum step size with gain =1.) Current sourced for rise times from 50ns (yellow) to 1000ns (brown) in 50ns steps are plotted.



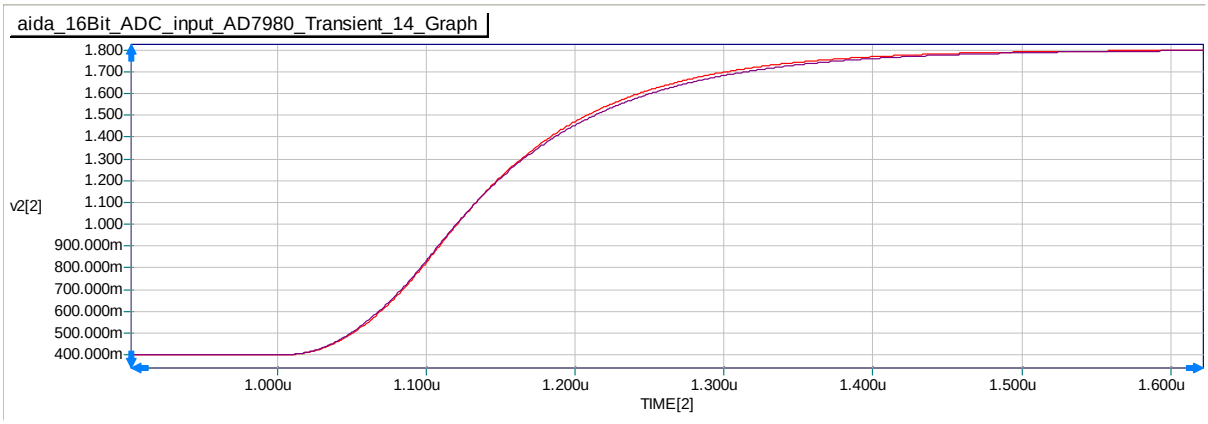
Plot of the effect of input pulse amplitude on current drawn from buffer amplifier (all input pulses have 100ns rise time). Current sourced for input pulses based on a 0.4V offset from 0.4V (i.e. step =0) (yellow) to 1.8V (i.e. step = 1.4V) (brown) in 0.2V steps are plotted.



Plot of the effect of RC filter values on current drawn from buffer amplifier (all input pulses have 100ns rise time, 1.4V amplitude). In all cases product of R3 and C5 was the same (89.1ns); what was varied was the R and C used to get the value. Current sourced for R=33, C=2.7nF is dark blue, R= 66, C = 1.35nF is purple, R=99, C=0.9nF is light blue , R=132, C=0.675nF is red.

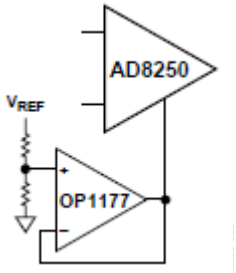


Plot showing the effect of the 2 extremes of RC combination on the value of V2 (at the ADC's sensing capacitor) (33R, 2.7nF is shown in red and 132R,0.675nF is shown in purple). Negligible difference.



My conclusion is that the AD8250 as it stands can't safely be changed to a higher gain because it will not be able to sink or source enough current when operating near the +5V rail, e.g. 16mA of current for 1V step. In the worst case it will need to sink 23mA for a full 1.8V to 0.4V step or source 23mA for full 0.4V to 1.8V step in 100ns which is outside the conditions characterised in the plots from the data sheet included above, but within the absolute maximum short circuit current output of 37mA. One way round this would be to change the RC values of R3 and C5 to keep the time constant the same but increase the resistor. The 66R, 1.35nF plot suggests a maximum current of only 12mA which is safely in the AD8250's characterised range. Values of 49.9R and 1.8nF are similar preferred values and reduce the resistance slightly too. In simulation they limit the worst case current to +15.6mA (0.4 to 1.8V step in 100ns) and -15.6mA for 1.8V to 0.4V in 100ns which are, in both cases within the AD8250's capabilities.

Further changes would be needed to implement a gain increase. These need to move the maximum output voltage away from the +5V power rail. A workaround would be to run the AD8250 off a more positive power rail (+12V?) which would mean that the output never went near the rail and so the higher gain configuration could be considered. (Patrick suggests an alternative workaround would be to reduce the reference voltages, e.g. to 3V and 1.5V- the ADR443 exists for 3V but another reference would be needed for 1.5V (lowest in the ADR44x range is 2.048V) The AD8250 data sheet fig 53 shows a potential divider of ADC Vref to ground buffered at the mid-point by OP1177.)



(New from here on in rev 6) **Notes on changing the references**
AD8250's Vref input is connected to one end of a resistor divider so the input must be driven by a low impedance driver, not an external resistor network which will interact with the precision internal resistor network, hence OP1177 buffer in AD8250 data sheet fig 53; AD8603 might also be suitable (recommended by AD for similar buffering with AD8270 ADC driver). The ADR443 would give a 3V reference and could be connected to a potential divider buffered by a low impedance unity gain follower to drive AD8250's Vref. In this case we'd need a pair of 0.1% resistors (adding errors in quadrature gives 0.141% voltage error which is of the same order as the ADR443A which has an initial accuracy spec of 4mV in 3V (0.1333%)). ADR443 can source up to 10mA and sink up to 5mA. AD7980 allows Vref to be in the range 2.4 to 5.1V and typically draws 0.33uA (no max specified). AD8250 draws typ 1uA for Vref = 0; it presents 20K impedance to 1.5V and so in our case it will draw 75uA.

Can't use the same ADR443 for ADC and for AD8250 (even though value is the same) because of the noise generated by the ADC on its Vref. In the circuit for the AD8250 reference aim for less than 1mA in potential divider e.g. 10k + 10k = 20k, 3V range = 0.15mA load (power 0.225mW/resistor). In both cases upgrade from ADR443A version on prototype to B version for better stability and lower noise if possible (NB B version only available in SOIC-8- some of the benefits appear to come from the larger package; A version MSOP8.)

Comparison of OP1177 and AD8603 buffers. The AD8603 is smaller (TSOT5 which is 2.9x2.8mm compared to MSOP-8 which is 3.2x5.5mm for OP1177). Electrically they are similar- both have input offsets of 50/60uV worst case. The OP1177 has better power supply rejection, lower voltage noise and lower thermal drift (0.7uV/C max compared to max 4.5uV/C (typ 1uV/C) in AD8603). ADR443A has 2ppm/C typical, 10ppm/C max drift; B version cuts this to 1typ, 3ppm/C max. 1ppm for 3V is 3uV, so max for B type is 9uV. Resistors will have larger temp coeff but should drift together as potential divider and hence not affect the output voltage. Conclusion- the temperature drift in the ADR443 is larger than the OP1177 and the B version is pretty much the same as the AD8603. 1 bit in 2^{16} over a 3 V range is 45.8uV, so thermal drift is all much less than 1 bit per degree C whichever buffer is used. Hence AD8603 is sufficient from thermal drift point of view. The noise from the ADR443B is specified as typically 1.4uV pk-pk from 0.1 to 10Hz; the ADR8603 is specified at 2.3uV typ, 3.5uV max in the same range whereas the OP1177 is only 0.4uV pk-pk typical. The AD8603 can run off a single supply whereas OP1177 needs dual rails.

Conclusion- OP1177 is slightly better from the noise point of view and so is slightly preferable to the AD8603 if there is room to fit it and its power supplies. However the AD8603 would be adequate, performing as well as the ADR443B in most respects (whereas the OP1177 outperforms the ADR443 for noise and thermal drift, hence reducing the overall noise at the AD8250 reference input compared to ADR443+AD8603).

A note on gain change
This configuration (ADR433B references used for AD7980B ADC and, via a potential divider, and OP1177 buffer, to AD8250 reference terminal) sets the ADC range to 3V and requires that the input signal from AD8250 to the ADC be in the range 0-3V (1.5V ±1.5V). This has the effect of increasing the gain because the AD8250 differential inputs are in the range -1.4V to 0 and 0 to +1.4V, offset now by 1.5V, not by 2.048V as in the prototype to that 0 is in the ADC mid-

scale, driving approx. 0.1V to 2.9V which is using 93% of the ADC range (previously only 70% was used). So the overall gain has been increased by reducing the ADC reference rather than by increasing the signal out of the AD8250.

Effect of lower Vref on ADC performance. NB- the AD7980B DNL is specified as typically ±0.4LSB, worst case ±0.9LSB for a Vref of 5V; dropping Vref to 2.5V degrades performance from a typical ±0.4 to ±0.55LSB. Scaling max/min at the same rate as typ we get ±1.24 LSB. Assuming that the DNL varies linearly with Vref we can extrapolate that with the new Vref of 3V we should have typical DNL which has 80% of the deterioration from 5V to 2.5V, i.e. typ ±0.52LSB and worst case ±1.17LSB. INL shows a smaller degradation when Vref is reduced (±0.6 to ±0.65LSB when Vref drops 5 to 2.5V so the same scaling gives ±0.64LSB for 3V).

SPECIFICATIONS

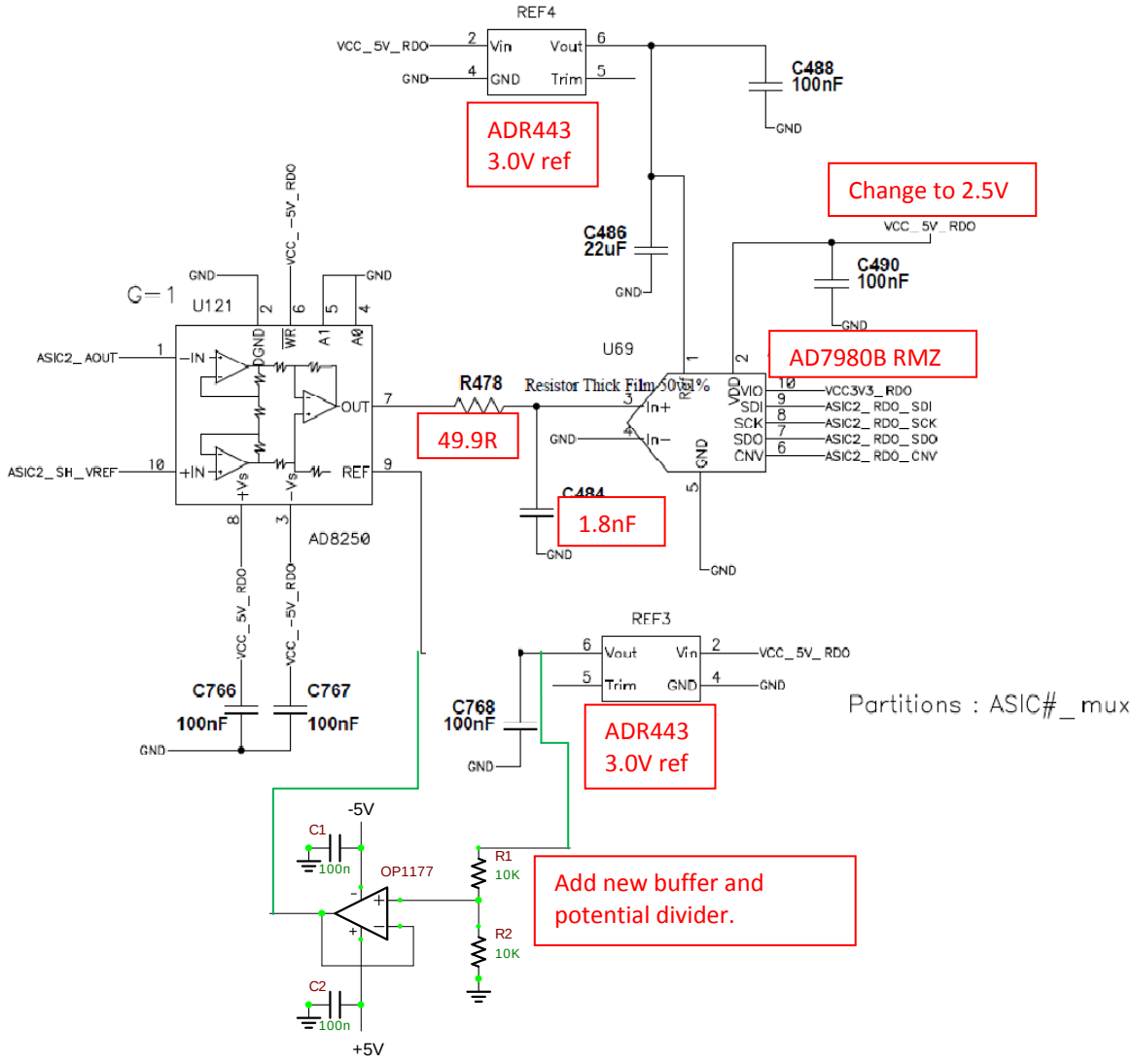
VDD = 2.5 V, VIO = 2.3 V to 5.5 V, V_{REF} = 5 V, T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

		A Grade			B Grade			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		16			16			Bits
ANALOG INPUT								
Voltage Range	IN+ − IN−	0		V_{REF}	0		V_{REF}	V
Absolute Input Voltage	IN+	−0.1		V_{REF} + 0.1	−0.1		V_{REF} + 0.1	V
	IN−	−0.1		+0.1	−0.1		+0.1	V
Analog Input CMRR	f_{IN} = 100 kHz		60			60		dB
Leakage Current @ 25°C	Acquisition phase		1			1		nA
Input Impedance			See the Analog Input section			See the Analog Input section		
ACCURACY								
No Missing Codes		16			16			Bits
Differential Linearity Error	REF = 5 V	−1.0	±0.5	+2.0	−0.9	±0.4	+0.9	LSB[1]
	REF = 2.5 V		±0.7			±0.55		LSB[1]
Integral Linearity Error	REF = 5 V	−2.5	±1.5	+2.5	−1.25	±0.6	+1.25	LSB[1]
	REF = 2.5 V		±1.65			±0.65		LSB[1]
Transition Noise	REF = 5 V		0.75			0.6		LSB[1]
	REF = 2.5 V		1.2			1.0		LSB[1]
Gain Error, T_{MIN} to T_{MAX}[2]			±2			±2		LSB[1]
Gain Error Temperature Drift			±0.35			±0.35		ppm/°C
Zero Error, T_{MIN} to T_{MAX}[2]		−1.0	±0.08	+1.0	−0.5	±0.08	+0.5	mV
Zero Temperature Drift			0.54			0.54		ppm/°C
Power Supply Sensitivity	VDD = 2.5 V ± 5%		±0.1			±0.1		LSB[1]

Summary of changes recommended in this section (revised circuit shown on next page):

1) Change ADC from AD7686 to AD7980B so as to increase the throughput (reduce signal processing time) to obtain the maximum performance possible given the AD8250 settling time to 0.001%. (Use the AD7980B rather than AD7980A to obtain best INL/DNL).
2) Increase effective gain of the ASIC mux output by reducing the ADC reference voltage rather than by increasing the AD8250 signal size. This has the advantage of increasing gain while keeping the AD8250 from trying to drive large transient currents to voltages near its power rails but the drawback of reducing 1 LSB from 61uV to 46uV, making noise sensitivity worse. Another advantage is that the AD8250 gain pins do not need to be controlled by FPGA.
3) Control the current sink/source requirements for AD8250 by a small change to the RC combination between the AD8250 and the ADC- currently 33R, 2.7nF; change to 49.9R (or 51R) and 1.8nF. This keeps the transient currents within ±16mA in simulation.



OP1177 shown running on ±5V rails; data sheet allows values down to ±2.5V but we need to be sure that the output of 1.5V is not affected by being close to rails. Fig 31 from OP1177 data sheet (below) shows that for low current (AD8250 will use less than 0.1mA) it's Ok to go within 0.7V of the rails so ±2.5V would be OK for outputs in the range ±1.8V. So OP1177 could use either ±2.5V or ±5V rails.

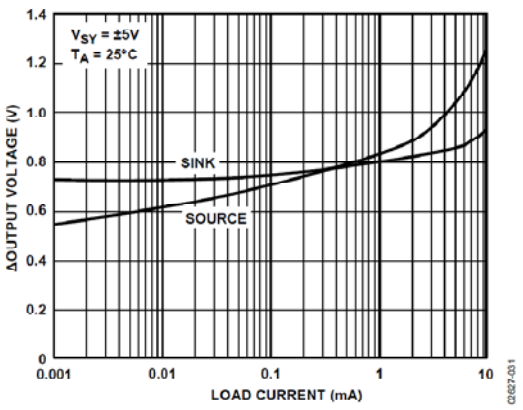


Figure 31. Output Voltage to Supply Rail vs. Load Current

Appendix A- Standard EIA Decade Values Table (100 to 1,000 Decade)

E6	E12	E24	E48	E96	E192	E6	E12	E24	E48	E96	E192	E6	E12	E24	E48	E96	E192
				100	100					215	215					464	464
			100		101				215		218				464		470
				102	102					221	221					475	475
		100			104			220			223			470			481
				105	105					226	226					487	487
			105		106				226		229				487		493
				107	107					232	232					499	499
	100				109		220				234		470				505
				110	110					237	237					511	511
			110		111				237		240				511		517
				113	113					243	243					523	523
		110			114			240			246			510			530
				115	115					249	249					536	536
			115		117				249		252				536		542
				118	118					255	255					549	549
100					120	220					258	470					556
				121	121					261	261					562	562
			121		123				261		264				562		569
				124	124					267	267					576	576
		120			126			270			271			560			583
				127	127					274	274					590	590
			127		129				274		277				590		597
				130	130					280	280					604	604
	120				132		270				284		560				612
				133	133					287	287					619	619
			133		135				287		291				619		626
				137	137					294	294					634	634
		130			138			300			298			620			642
				140	140					301	301					649	649
			140		142				301		305				649		657
				143	143					309	309					665	665
					145						312						673
				147	147					316	316					681	681
			147		149				316		320				681		690
				150	150					324	324					698	698
		150			152			330			328			680			706
				154	154					332	332					715	715
			154		156				332		336				715		723
				158	158					340	340					732	732
	150				160		330				344		680				741
				162	162					348	348					750	750
			162		164				348		352				750		759
				165	165					357	357					768	768
		160			167			360			361			750			777
				169	169					365	365					787	787
			169		172				365		370				787		796
				174	174					374	374					806	806
150					176	330					379	680					816
				178	178					383	383					825	825
			178		180				383		388				825		835
				182	182					392	392					845	845
		180			184			390			397			820			856
				187	187					402	402					866	866
			187		189				402		407				866		876
				191	191					412	412					887	887
	180				193		390				417		820				898
				196	196					422	422					909	909
			196		198				422		427				909		920
				200	200					432	432					931	931
		200			203			430			437			910			942
				205	205					442	442					953	953
			205		208				442		448				953		965
				210	210					453	453					976	976
					213						459						988

Appendix B Possible buffers for mezzanine (now obsolete as ASIC can drive 1.3mA)

Some possible buffer amplifier parts are shown in the table below.

Spice simulation of AD8034 (a typical part) shows that the Vref crosstalk is unaffected by using a buffer to drive the ASIC preamp output.

Part	Amp per pkg	Package	BW G=1 small signal	V_s range	Quiescent current	Noise nV/√Hz	I_out	V_out
AD8034 @ V_s=5V	2	SOT23-RJ8 (3x3mm)	80MHz	5-24V (single or dual)	3.3mA typ 3.5mA max/amp	11	20 mA within 0.5V of V_s; 1mA for 0.1V	0.16-4.83V min
AD8030/ AD8040 @ V_s=3V	2/4	SOT23-RJ8 (3x3mm) TSSOP-14 (6.4 x 5.1mm)	112MHz	2.7-12V (single or dual)	1.3mA typ 1.4mA max/amp	16.5	Not specified short cct 80/40mA *(selection table says 5mA)*	Within 0.09V± R_L=1k
ADA4851-2 or -4 @ V_s=3V	2/4	8MSOP 3.2x5.2mm TSSOP-14 (6.4 x 5.1mm)	130MHz	2.7-12V (single or dual)	2.4mA typ 2.7mA max/amp	10	Not specified short cct 90/70mA	0.06 to 2.89V min R_L=1k
ADA4850-2 @ V_s=3V	2	LFCSP 3x3mm	160MHz	2.7-6V (single or dual)	2.4mA typ 2.8mA max/amp	10	Not specified short cct 105/74mA	0.06 to 2.83V min R_L=1k
AD8652 @ V_s=2.7V	2	8MSOP 3.2x5.2mm	50MHz (41V/us slew)	2.7-5.5V single	9mA typ 10mA max per amp	4.5	40mA typ	30mV to 2.67V (I_L=0.25mA)
AD8606 @ V_s=2.7V	2	WLCSP-CB8-1 (1.48 x1.825mm)	9MHz (5V/us slew**)	2.7-5.5V single	1.15mA typ 1.4mA max	8 typ 12 max	±30mA typ	40mV to 2.6V (I_L=1mA)

Key features of the parts are highlighted in the table where they differ significantly from the others.

*** in simulations we observe that the 5V/us slew rate means that a 4MHz sine wave from 0.4 to 1.8V is attenuated and turned into a triangular wave by the 8605 (4MHz triangular waveform, 1.4V pk to pk would need a slew rate of 1.4V in 0.125us = 11.2V/us; sine wave has greater dV/dt than triangle in some places.) Cutting amplitude from ±0.7V to ±0.2V results in a recognisable sine wave out although slightly attenuated (20mV away from max/min); ±0.1V is better with only 5mV attenuation at max/min. Therefore AD8606 is only suitable if the ASIC output swing is limited to 200mV typ, 400mV max at the fastest rise time(90ns).*

AD8029/8030 and ADA4850, ADA4851 have models incompatible with BBspice so can't be simulated except standalone in the Nat Semi/ADI spice program which can't simulate ADA4932.

Rejected AD8039 (output can't go below 0.9V).

Appendix C (was Section 5- Operating at lower supply voltages- section probably obsolete now (rev 3 onwards))moved to appendix C

~~The board level power supply design will be easier if the +5V supply is dropped to +4.5V. This section investigates possible effects.~~

~~1) Data sheet analysis~~

~~AD8055 output swings up to ±3.1V (typ) ±2.9V (min) with 5V supplies- assuming it works to within the same margins of the supply (1.9V typ, and 2.1V min) then with 4.5V the limits would be 2.6V typ and 2.4V min. The maximum output required is 2.0V (max possible Vref) which is 0.4V away from the worst case limit. Since it works on dual supplies there is no problem for values near 0V.~~

~~ADA4932 works to within 1.02V (typ) or 1.15V (min) of its power rails so for 4.5V the maximum output in the worst case is 3.35V. The maximum input to the FADC which follows the ADA4932 is 2V so the output should work perfectly.~~

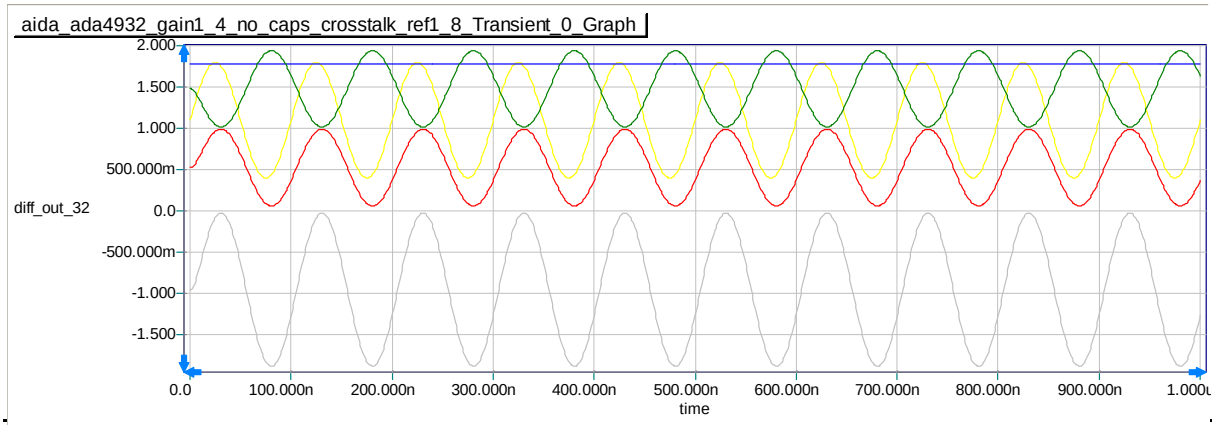
~~Conclusion of the data sheet analysis is that a drop from +5V to +4.5V in the power rail is OK.~~

~~Dropping further to 4V would cause a possible problem if the AD8055 Vref buffer amplifier is on the worst case (2.1V below power rail) i.e. with a maximum V_{out} of 1.9V for 4V power rails- in this case the ASIC Vref adjustment range would be curtailed from its normal 1.6 to 2.0V to 1.6-1.9V. So to be safe the supply should be kept to 4.1V as an absolute minimum, preferably 4.5V to avoid running the AD8055 amplifier on the edge of its performance window. There are no such problems for ADA4932 which would run easily on a 4V rail in this application.~~

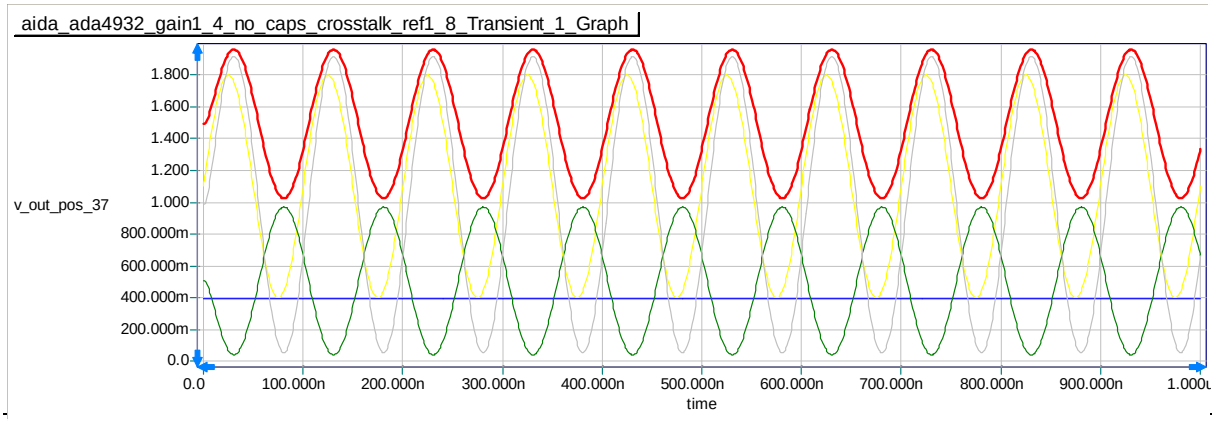
~~2) Simulation~~

~~The crosstalk simulation exercises the circuit right up to the limits of the ASIC output (range 0.4 to 1.8V or 1.8V to 0.4V depending on the charge polarity) so this is used for the analysis with power rail voltages dropped from ±5V to ±4V (worse than the suggested change). No clipping is observed in the simulations results below.~~

~~Plot with Vref = 1.8V~~



~~Plot with Vref = 0.4V~~



~~In both plots above the yellow trace is ASIC preamp input (0.4 to 1.8V); blue trace is Vref (0.4V or 1.8V), red trace is Vout+; green trace is Vout- and silver trace is Vdiff.~~

~~Conclusion~~

~~Operating with supplies at +4.5V/ 5V (or even ±4.5V) instead of ±5V should be OK.~~

~~Operating at 4.0V would involve replacing the AD8055 and probably would require 2 buffers per ASIC to get enough current from a different (rail to rail) op amp.~~