AIDA Update

presented by

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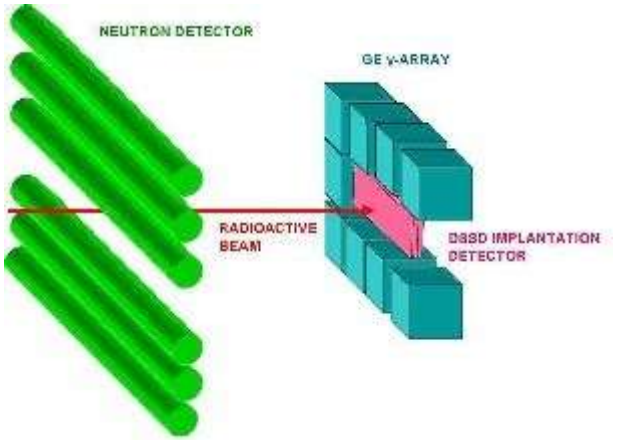
AIDA: Introduction

Advanced Implantation Detector Array (AIDA)

UK collaboration: *University of Edinburgh, University of Liverpool, STFC Daresbury Laboratory & STFC Rutherford Appleton Laboratory*



- SuperFRS
- Exotic nuclei ~ 50 – 200MeV/u
- Implant – decay correlations
- Multi-GeV implantation events
- Subsequent low-energy decays
- Tag events for gamma and neutron detector arrays

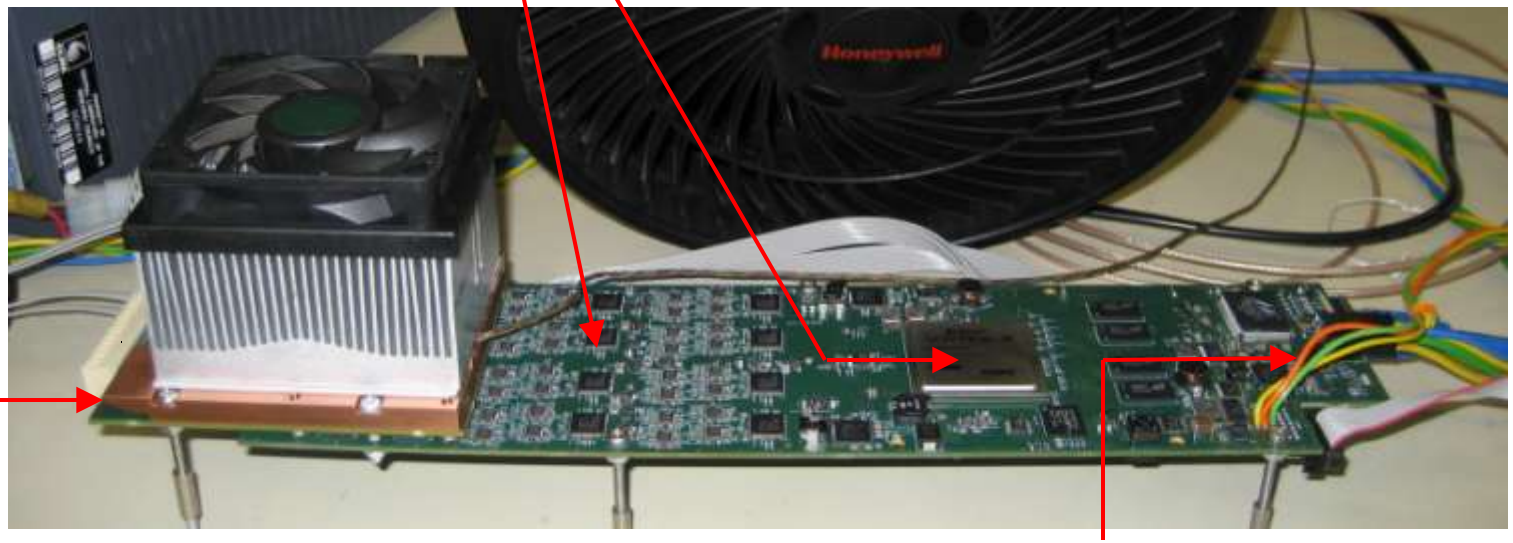
Detector: multi-plane Si DSSD array
wafer thickness 1mm
8cm x 8cm (128x128 strips) *or* 24cm x 8cm (384x128 strips)

Instrumentation: ASIC
low noise (<12keV FWHM), low threshold (0.25% FSR)
20GeV FSR *plus* (20MeV FSR *or* 1GeV FSR)
fast overload recovery (~μs)
spectroscopy performance
time-stamping

AIDA Hardware

Mezzanine:
4x 16 channel ASICs
Cu cover
EMI/RFI/light screen
cooling

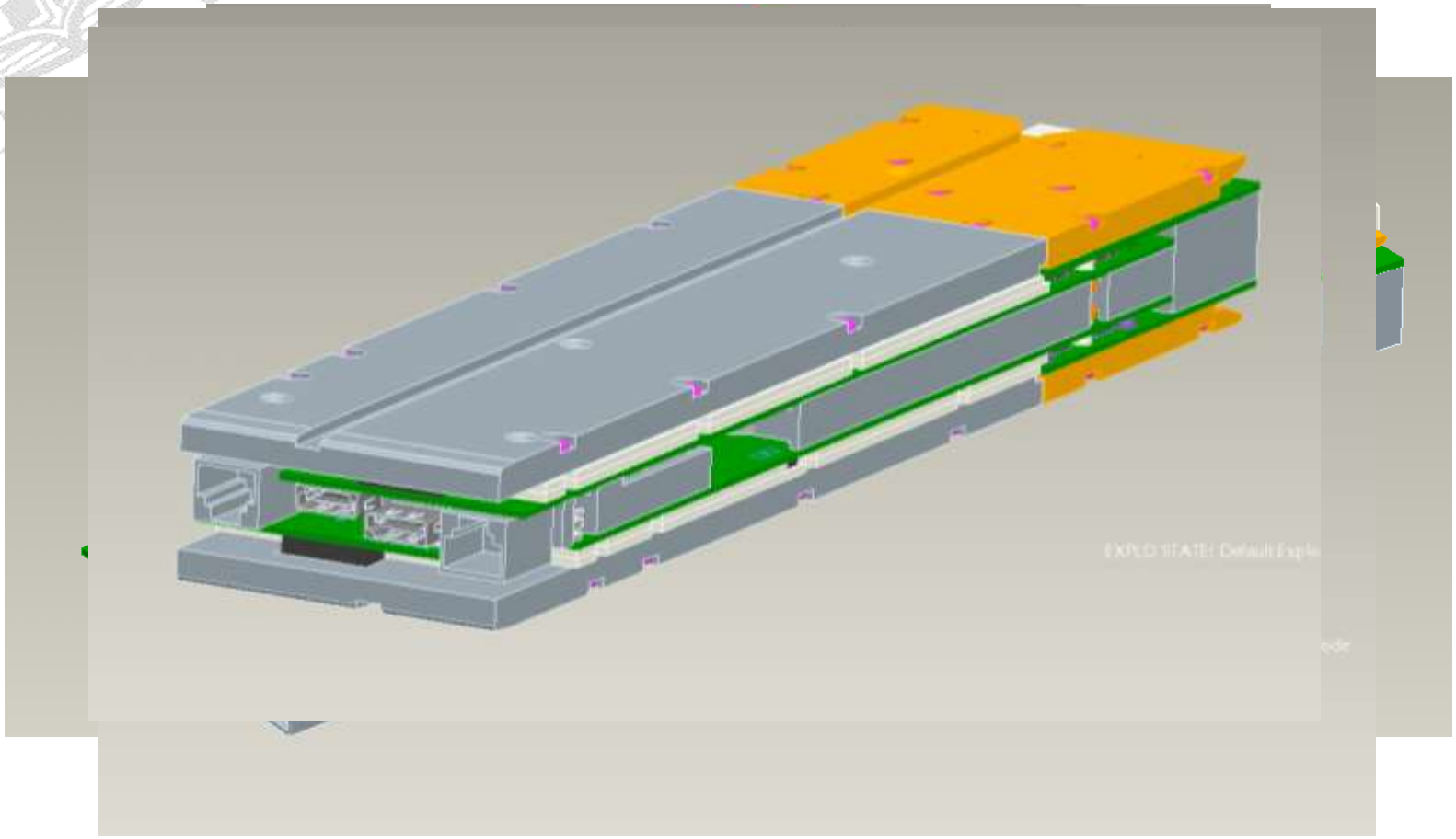
FEE:
4x 16-bit ADC MUX readout (not visible)
8x octal 50MSPS 14-bit ADCs
Xilinx Virtex 5 FPGA
PowerPC 40x CPU core/Linux OS – DAQ



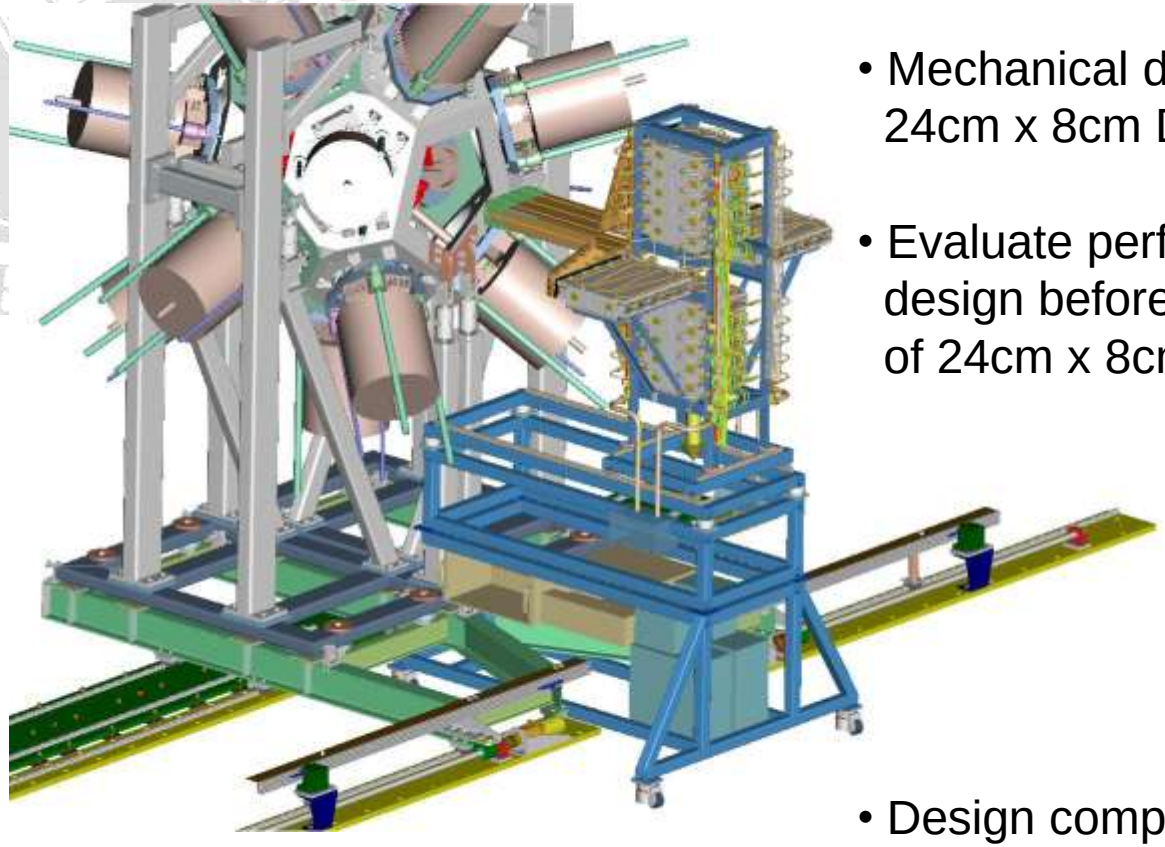
FEE width: 8cm
Prototype – air cooling
Production – recirculating coolant

Gbit ethernet, clock, JTAG ports
Power

FEE Assembly Sequence



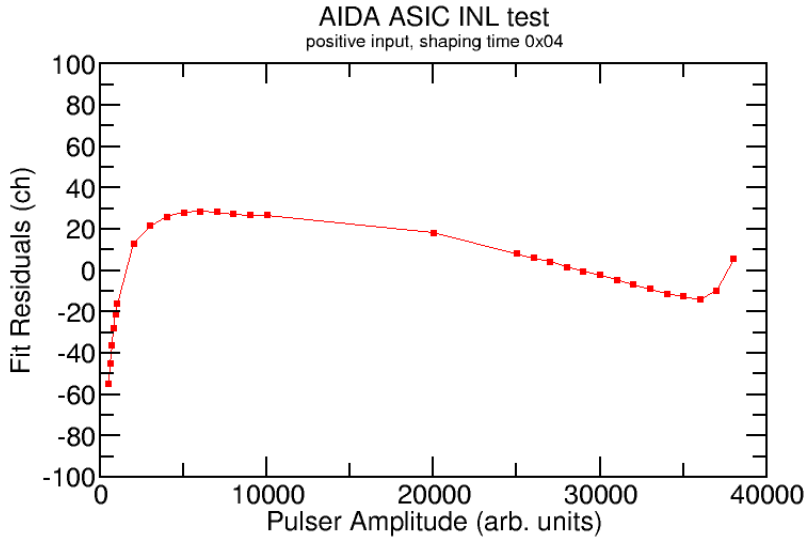
AIDA Mechanical



- Mechanical design for 8cm x 8cm and 24cm x 8cm DSSSDs is complete
- Evaluate performance of 8cm x 8cm design before proceeding to manufacture of 24cm x 8cm design
- Design compatible with BELEN, TAS, MONSTER , RISING, FATIMA etc.

- Design drawings (PDF) available
  http://www.eng.dl.ac.uk/secure/np-work/AIDA/

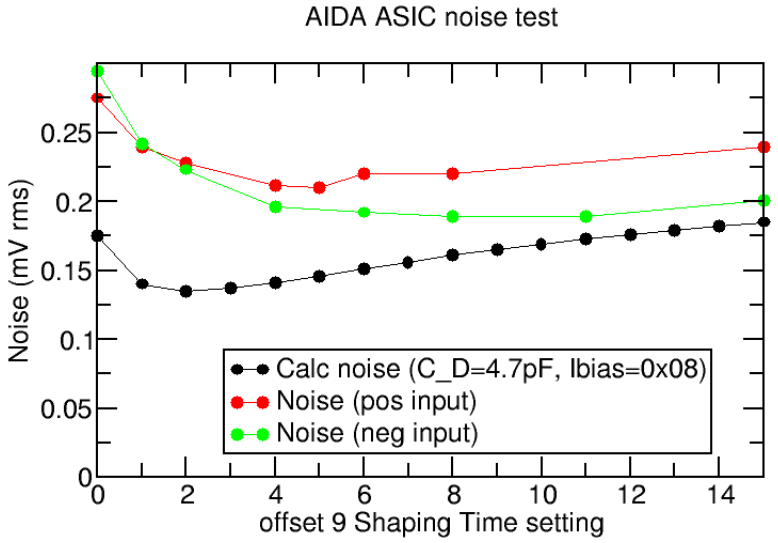
Bench Tests of *Prototype* Hardware



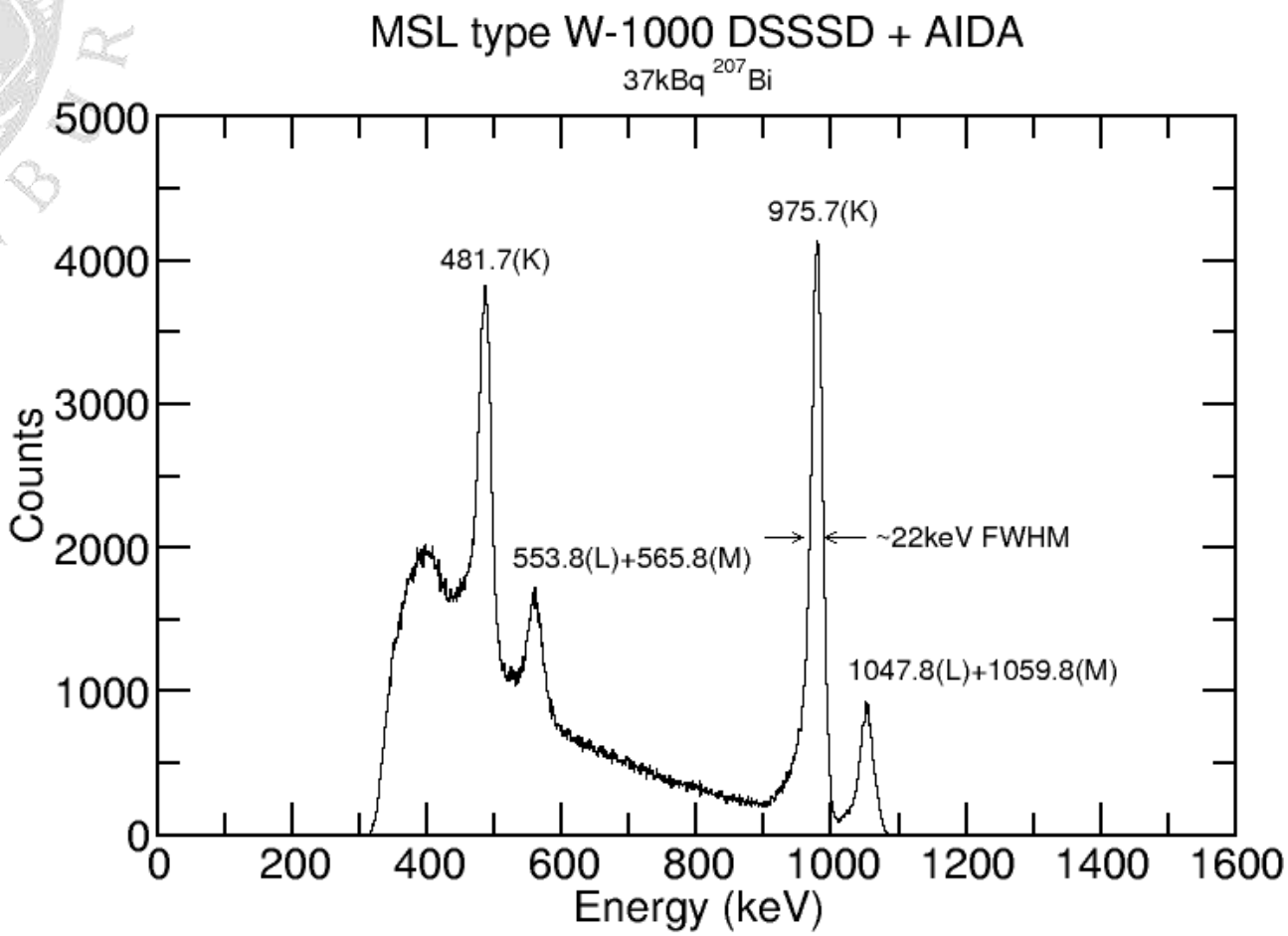
Tests with pulser demonstrating integral non-linearity and noise performance of 20MeV range

INL < 0.1% (> 95% FSR)

0.15mV rms ~ 2.5keV rms Si



Tests with AIDA *Production* Hardware

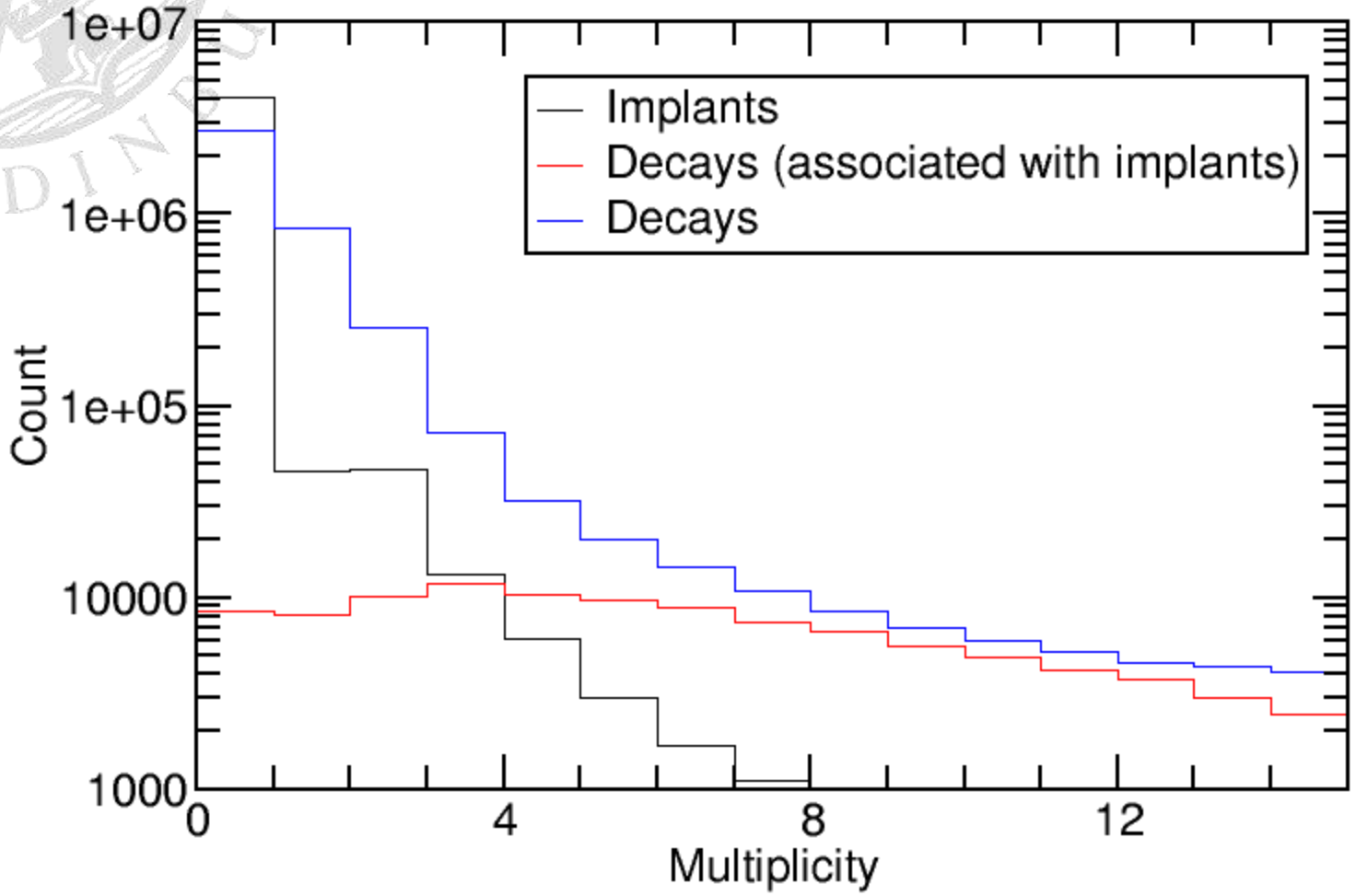


- Realistic input loading C_D ~ 60pF, I_L ~ 60nA
- Expectation ~12keV FWHM

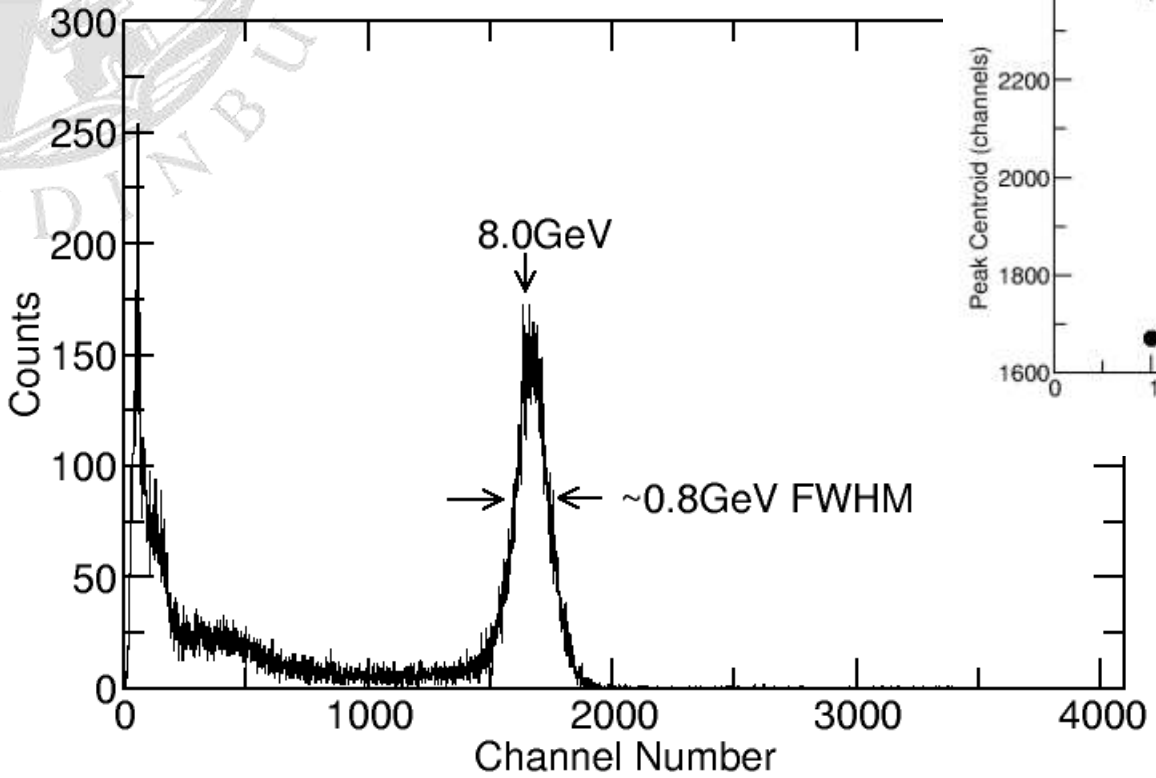
GSI Commissioning Test – August 2011

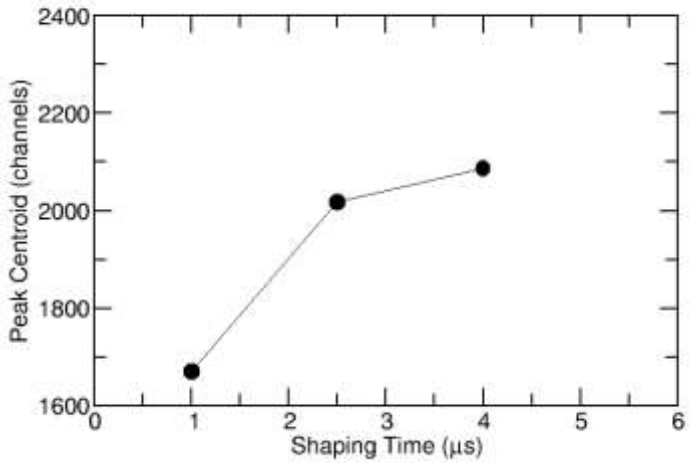
- SIS 250MeV/u ^{209}Bi
- Beam delivery direct to HTC
- From exit port
  - + ~1.0m air
  - + ~2mm Al (degrader)
  - + ~0.9m air
  - + *1x MSL type W-1000 DSSSD*
    - cheap alternative to type BB18 …
- Test of response of 20GeV range
- No rejection of lighter, lower energy ions generated by passage of beam through exit port/degrader

Event Multiplicity

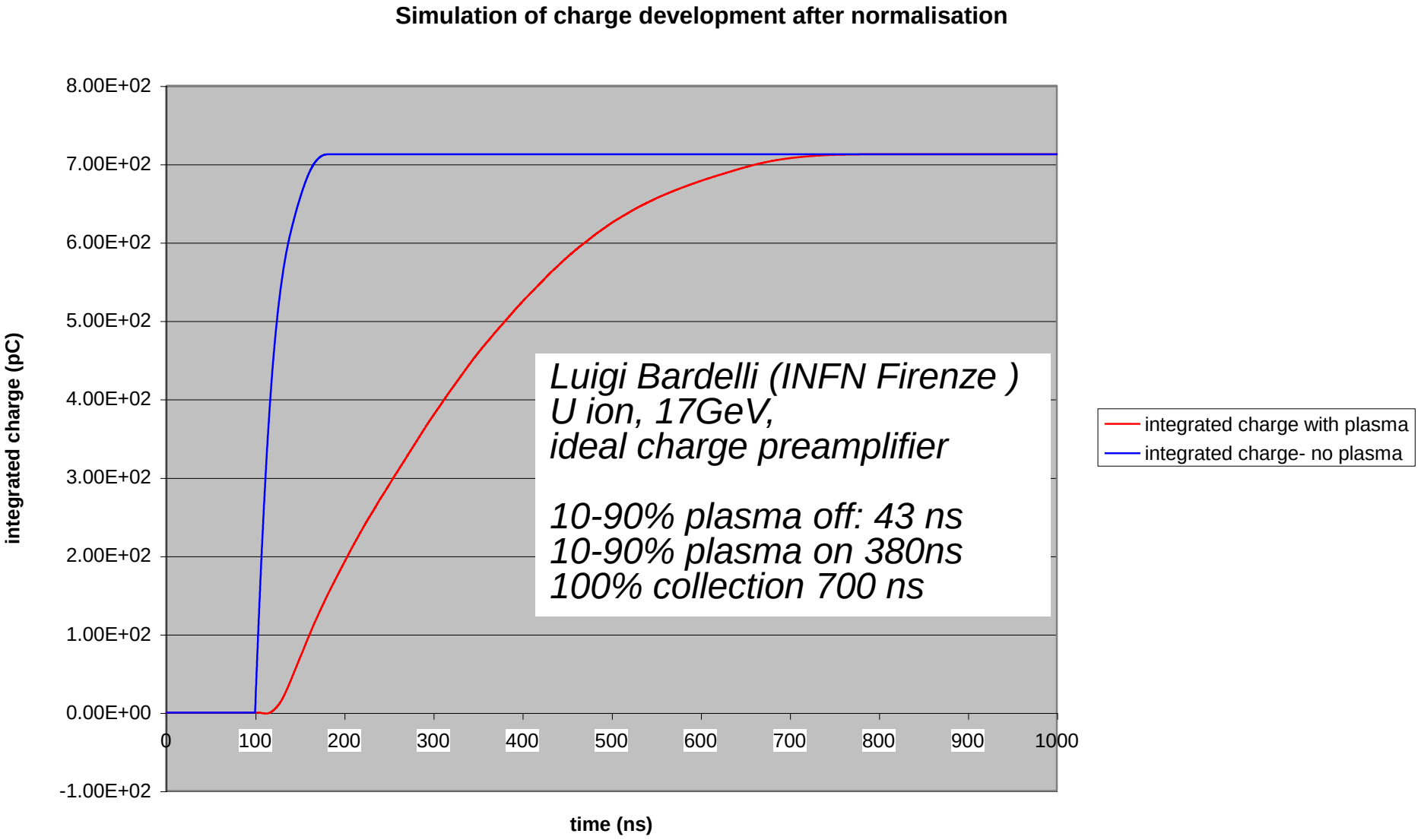


High Energy Implantation Events

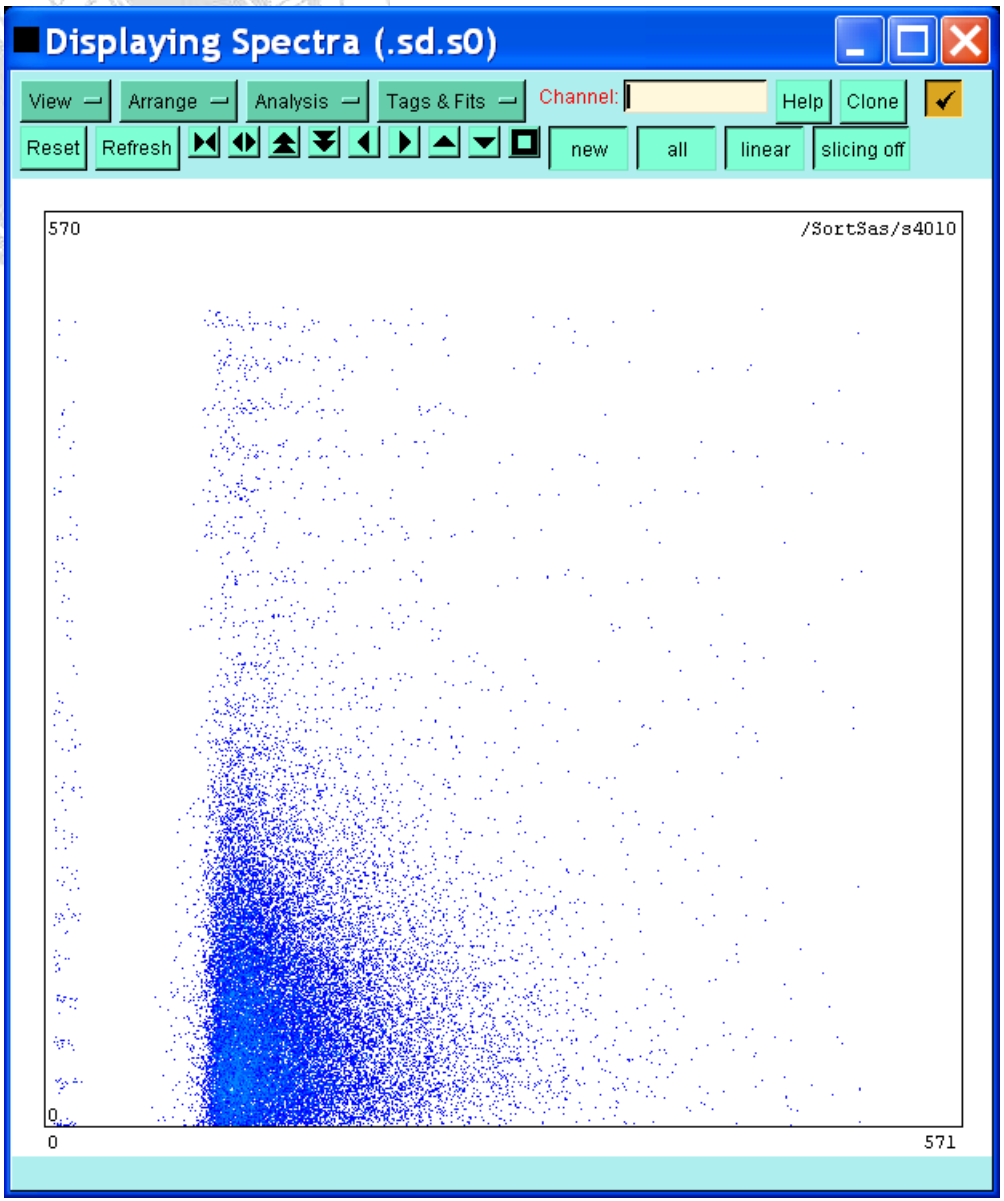




- Significant ballistic deficit effects
- Confirms Bardelli model and previous TAMU observations
- Implies preamp risetime for high energy heavy-ions >500ns
  (cf. intrinsic preamp risetime ~90ns)


Simulation of charge development after normalisation
integrated charge (pC)
8.00E+02
7.00E+02
6.00E+02
5.00E+02
4.00E+02
3.00E+02
2.00E+02
1.00E+02
0.00E+00
-1.00E+02
0
100
200
300
400
500
600
700
800
900
1000
time (ns)
Luigi Bardelli (INFN Firenze)
U ion, 17GeV,
ideal charge preamplifier
10-90% plasma off: 43 ns
10-90% plasma on 380ns
100% collection 700 ns
integrated charge with plasma
integrated charge- no plasma

Implant Decay Correlations

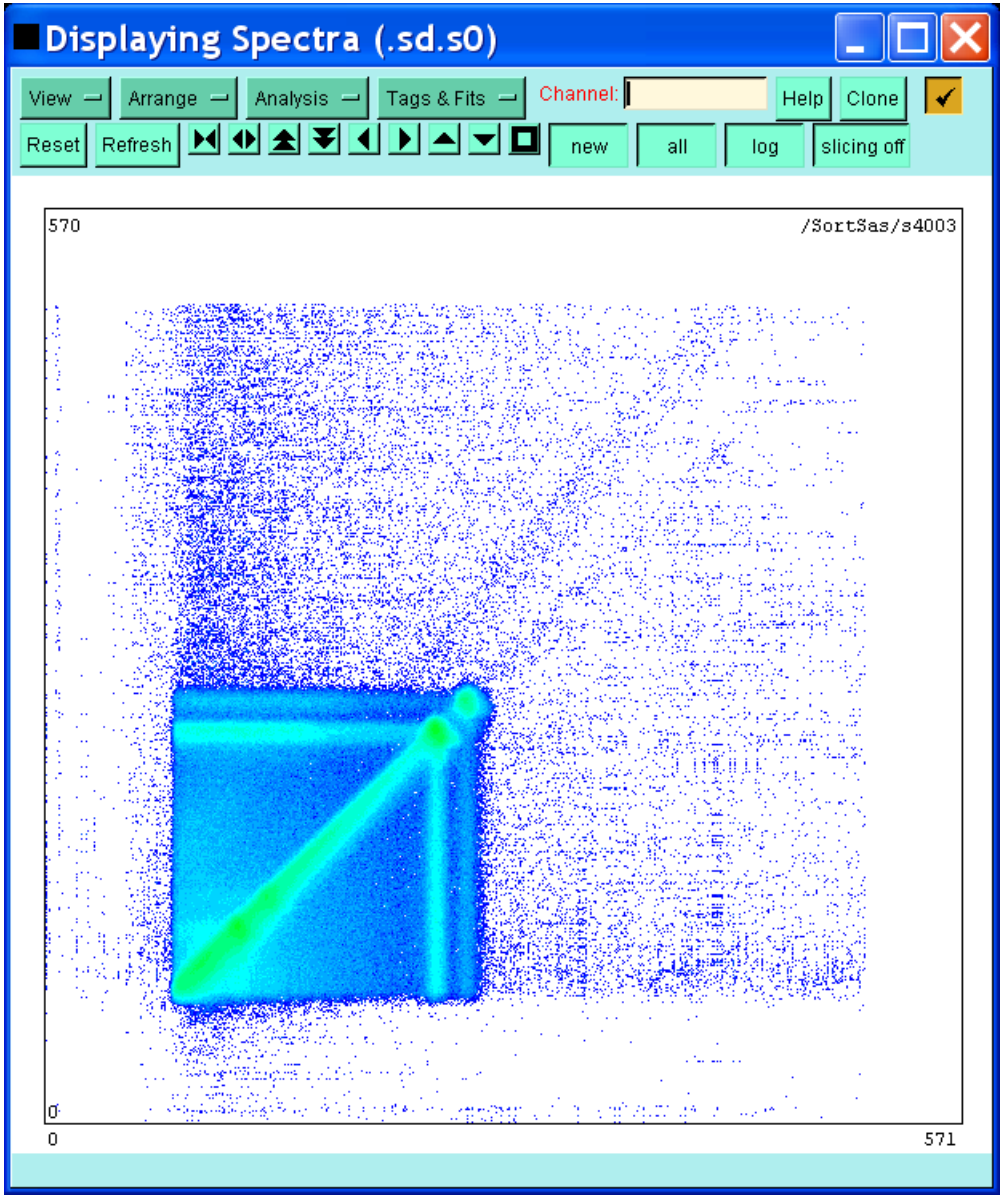


y-scale 1ms/channel
x-scale 4keV/channel

decay time = t_{xy}(decay)-t_{xy}(implant)

Expect random correlations only

E(p+n strips) versus E(n+n strips) - decay events



AIDA: status

- DSSSD with sub-contractor (MSL)
  - *12+ 8cm x 8cm production detectors delivery November 2011*

- Production hardware (ASIC, FEE Mezzanine PCB, FEE PCB) has been delivered by sub-contractors

- ASIC + FEE Mezzanine module assembly
  - *12 complete*
  - *65+ queued*

- FEE PCB QA acceptance tests
  - *50 complete*
  - *20 queued*
  - *8 with faults requiring further testing*

- Mechanical design and infrastructure (HV, PSUs, cooling etc.)
  - *detector HV, FEE PSUs, cooling & FEE crates delivered*
  - *support assembly University of Liverpool workshop*

AIDA: outlook

- AIDA production hardware was available for commissioning on schedule in 2011/Q3

- Performance of 20GeV & 1GeV ranges meets specification
  - *need to optimise DSSSD-FEE coupling for 20MeV range*
  - *progress very encouraging*

- Basic data merge with MBS successfully demonstrated during AIDA+LYCCA test May 2011 (based on common scaler clocked by MBS)
  - *further work required to extend from 1 FEE to multiple FEE cards*

- Continuing FEE development work in progress
  - *DSP (e.g. digital CFD, MWD)*
  - *timestamp distribution hardware (MACB designed)*

- DAQ software development work in progress
  - *migrating interface from Tcl/Tk to XML/SOAP (web-based)*
  - *control and management of multiple FEE modules*
  - *timestamp-ordered data merge*

Bottom line – AIDA is ready and needs to be scheduled on FRS