

Advanced Implantation Detector Array (AIDA)
Second BRIKEN Workshop
RIKEN 30-31 July 2013

presented by
Tom Davinson
on behalf of the AIDA collaboration
(Edinburgh – Liverpool – STFC DL & RAL)

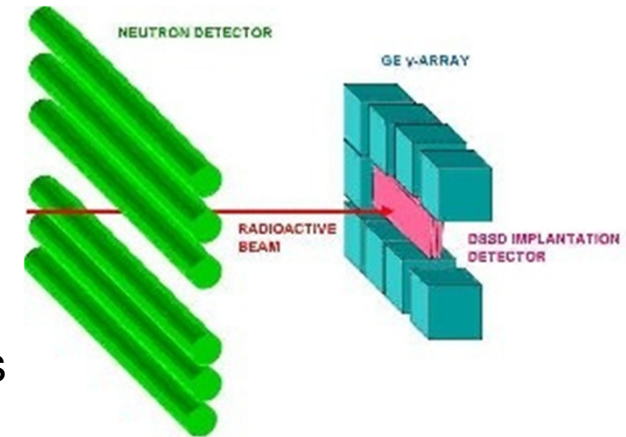
Tom Davinson
School of Physics & Astronomy
The University of Edinburgh

AIDA: Introduction

Advanced Implantation Detector Array (AIDA)

UK collaboration: *University of Edinburgh, University of Liverpool, STFC Daresbury Laboratory & STFC Rutherford Appleton Laboratory*

- SuperFRS
- Exotic nuclei $\sim 50 - 200\text{MeV/u}$
- Implant – decay correlations
- Multi-GeV implantation events
- Subsequent low-energy decays
- Tag events for gamma and neutron detector arrays



Detector: multi-plane Si DSSD array

wafer thickness 1mm

8cm x 8cm (128x128 strips) *or* 24cm x 8cm (384x128 strips)

Instrumentation: ASIC

low noise ($<12\text{keV}$ FWHM), low threshold (0.25% FSR)

20GeV FSR *plus* (20MeV FSR *or* 1GeV FSR)

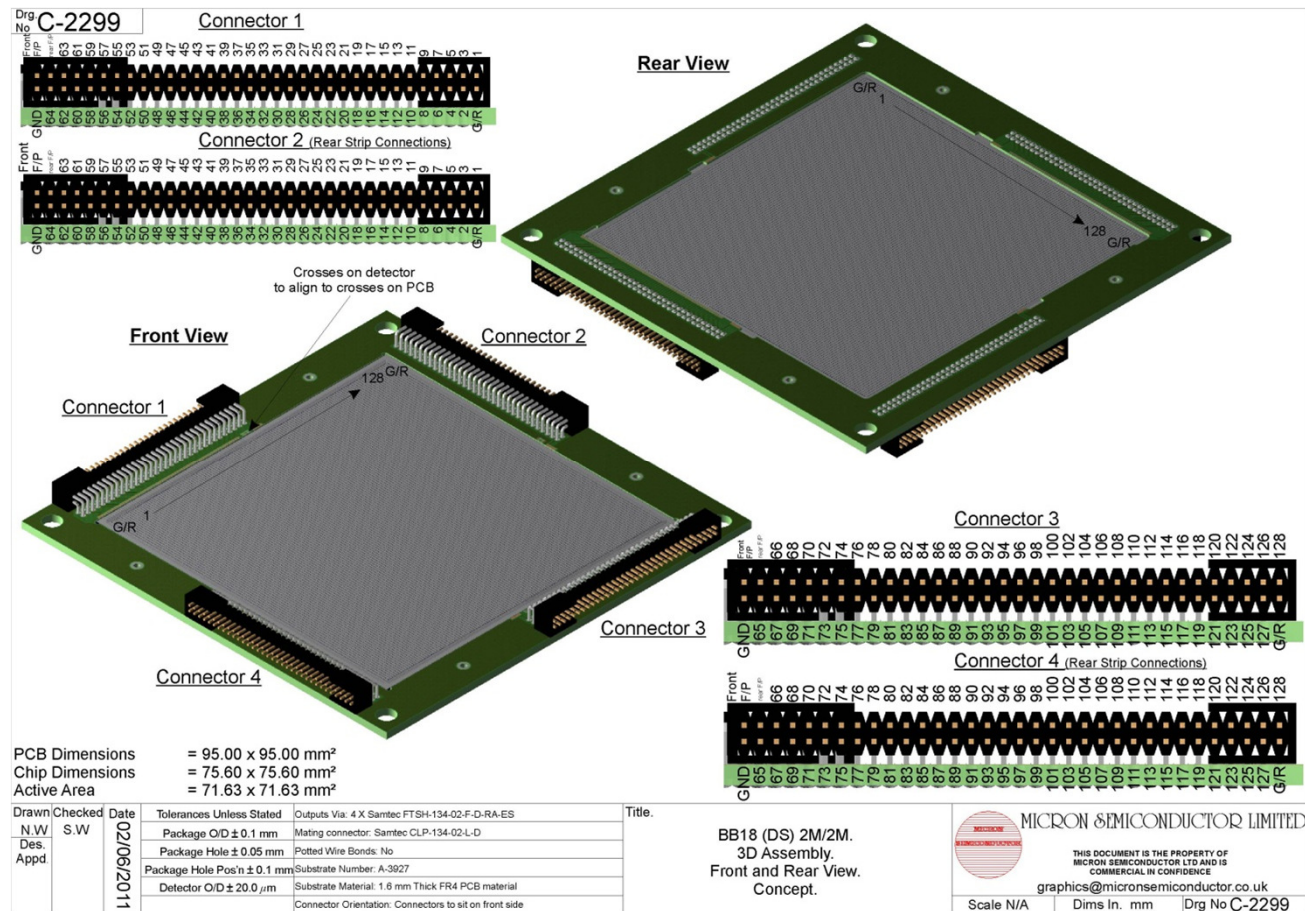
fast overload recovery ($\sim\mu\text{s}$)

spectroscopy performance

time-stamping

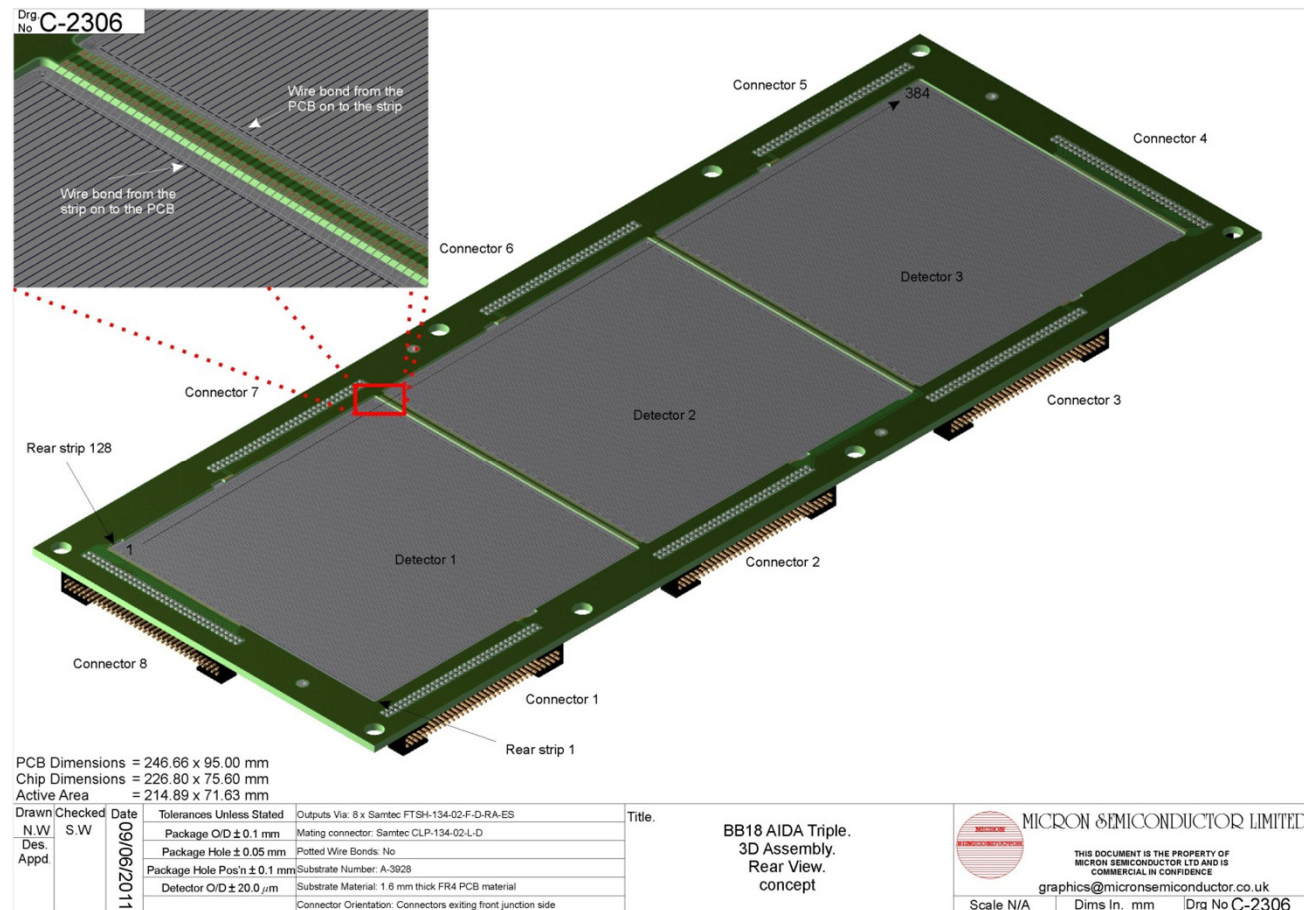
MSL type BB18

128 x 128 strips (16384 pixels)
multi-guard ring
0.560mm strip pitch
1mm wafer thickness



MSL type BB18

384 x 128 strips (49152 pixels)
multi-guard ring
0.560mm strip pitch
1mm wafer thickness



AIDA Hardware

Each FEE64 card acts as an independent DAQ

Each data word encoded with 48-bit timestamp

Data merged at network switch and time-ordered by Linux workstation

Mezzanine:

4x 16 channel ASICs

Cu cover

EMI/RFI/light screen
cooling

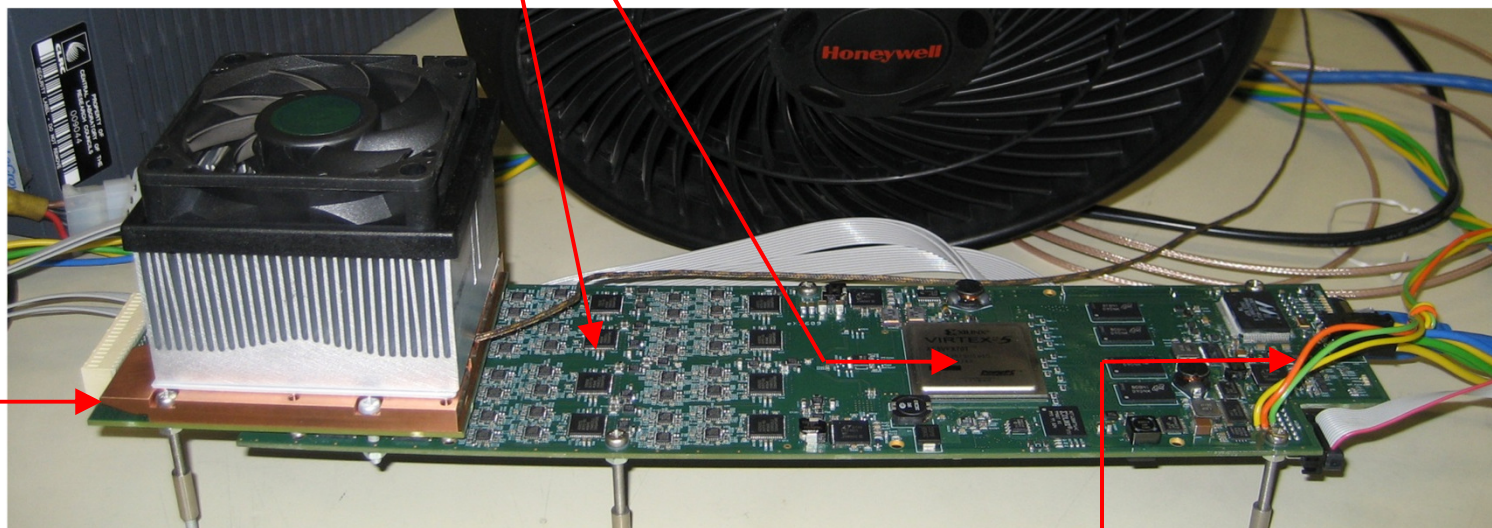
FEE:

4x 16-bit ADC MUX readout (not visible)

8x octal 50MSPS 14-bit ADCs

Xilinx Virtex 5 FPGA

PowerPC 40x CPU core/Linux OS – DAQ



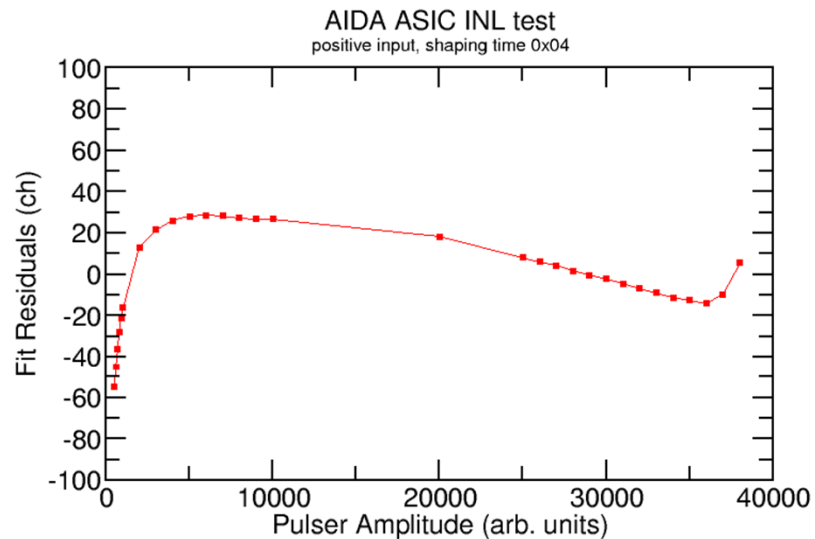
FEE width: 8cm

Prototype – air cooling

Production – recirculating coolant

Gbit ethernet, timestamp, JTAG ports
Power

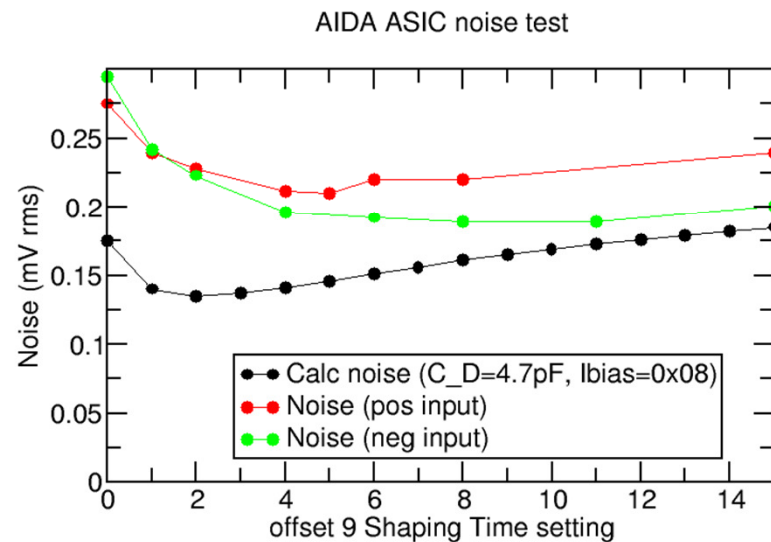
Bench Tests of *Prototype* Hardware



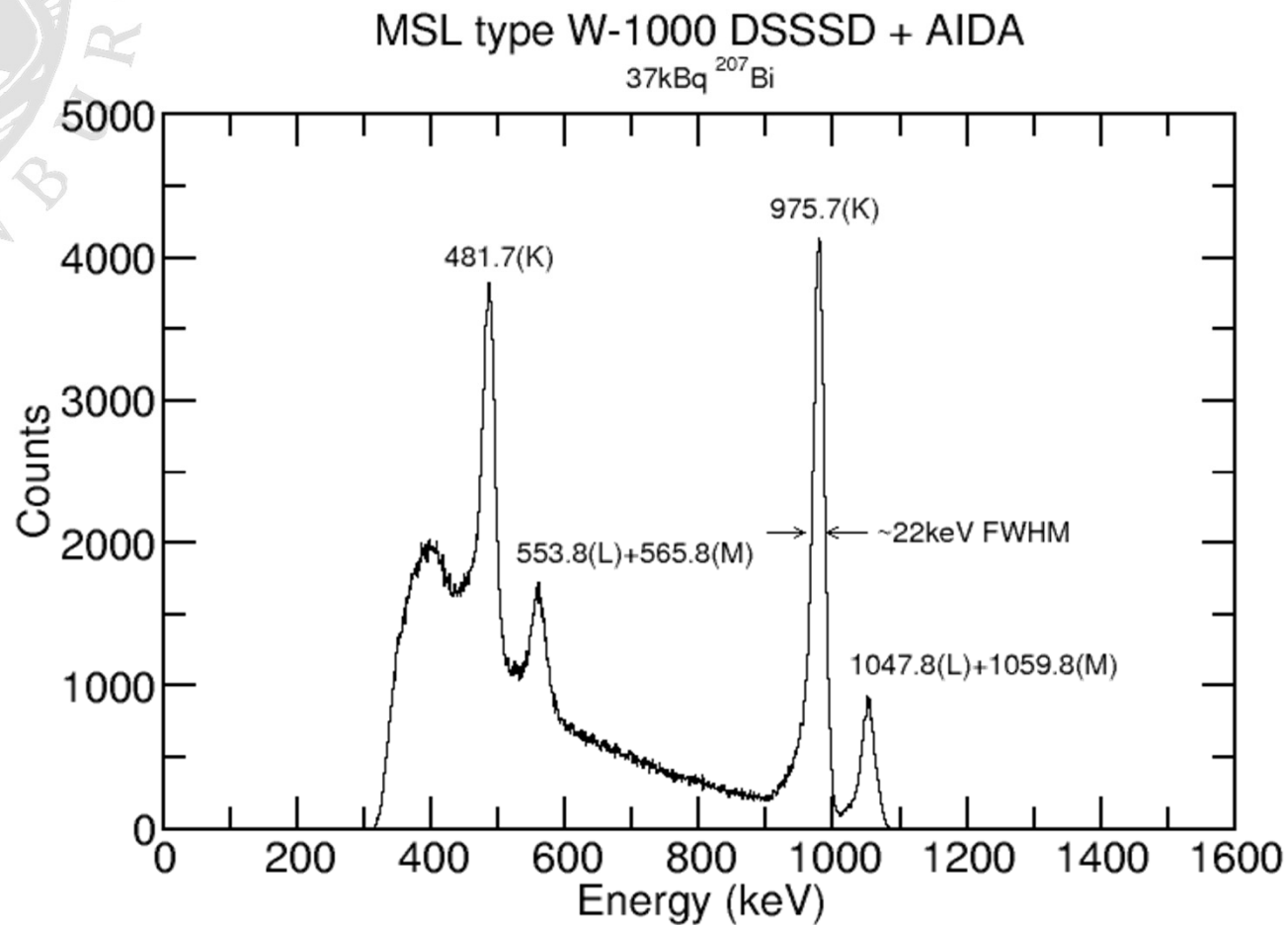
0.15mV rms ~ 2.5keV rms Si

*Tests with pulser demonstrating
integral non-linearity and noise
performance of 20MeV range*

INL < 0.1% (> 95% FSR)

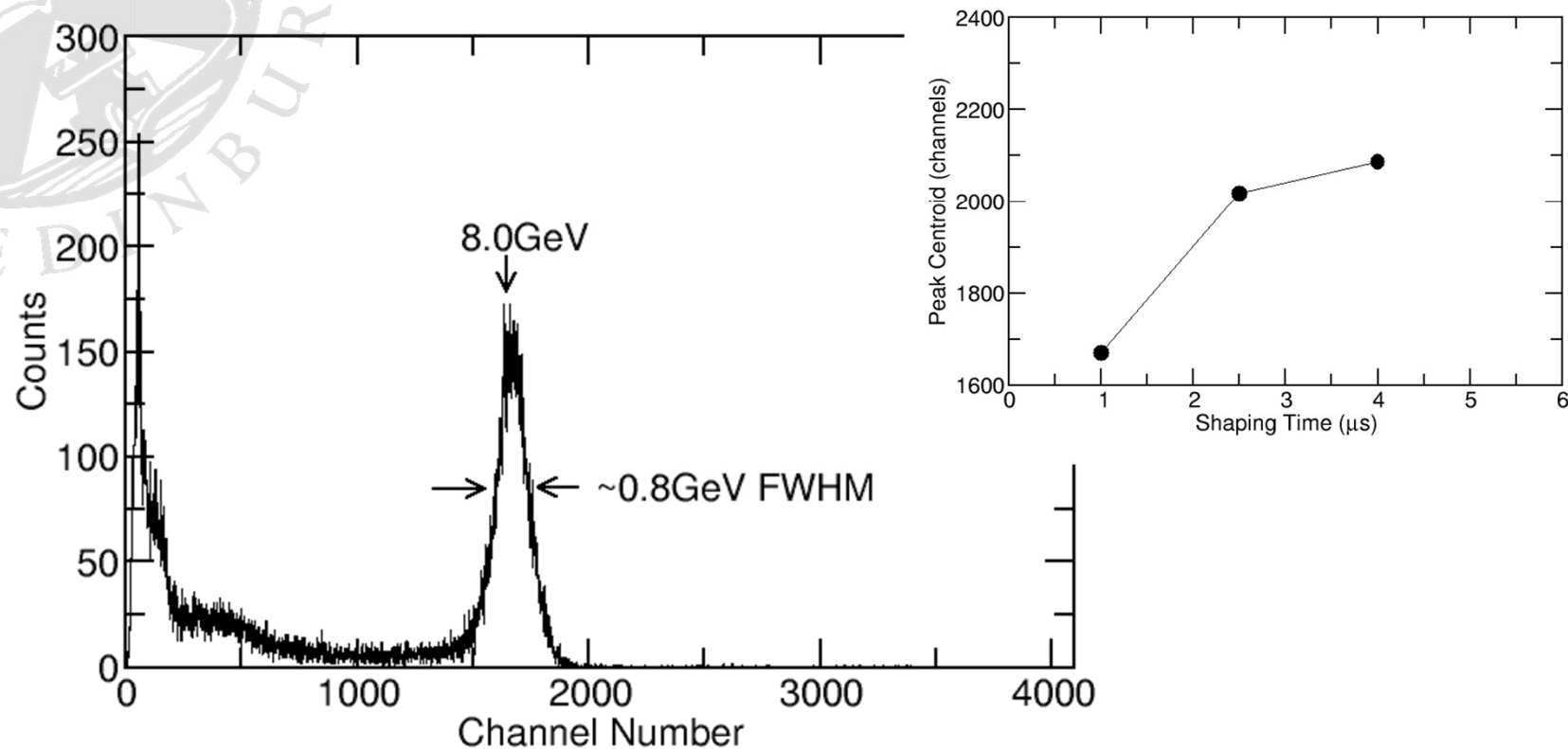


Tests with AIDA *Production* Hardware: 20MeV range



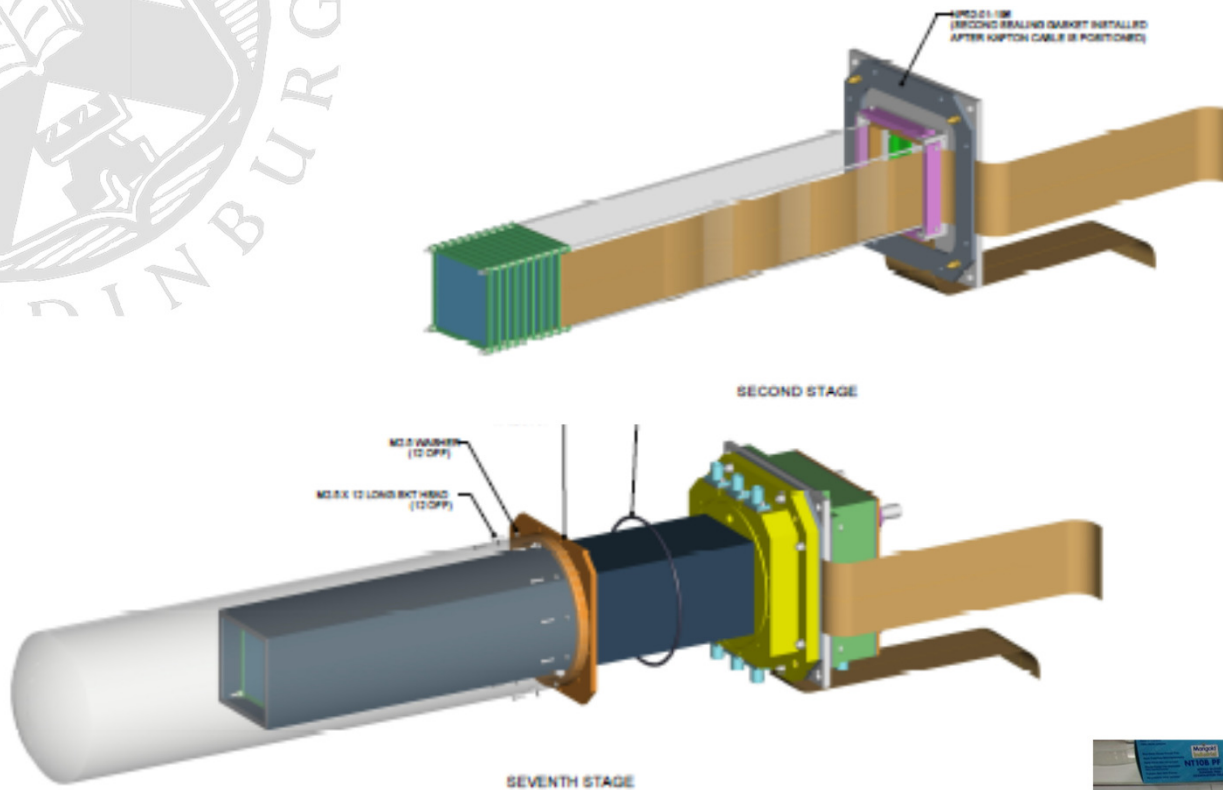
- Realistic input loading $C_D \sim 60\text{pF}$, $I_L \sim 60\text{nA}$
- Expectation $\sim 12\text{keV}$ FWHM

Tests with AIDA *Production* Hardware: 20GeV range



- SIS 250MeV/u ^{209}Bi
- Beam delivery direct to HTC
- Significant ballistic deficit effects
- Confirms Bardelli model and previous TAMU observations
- Implies preamp risetime for high energy heavy-ions >500ns
(*cf. intrinsic preamp risetime ~90ns*)

8cm x 8cm AIDA Enclosure



DSSSD - instrumentation via Kapton PCB

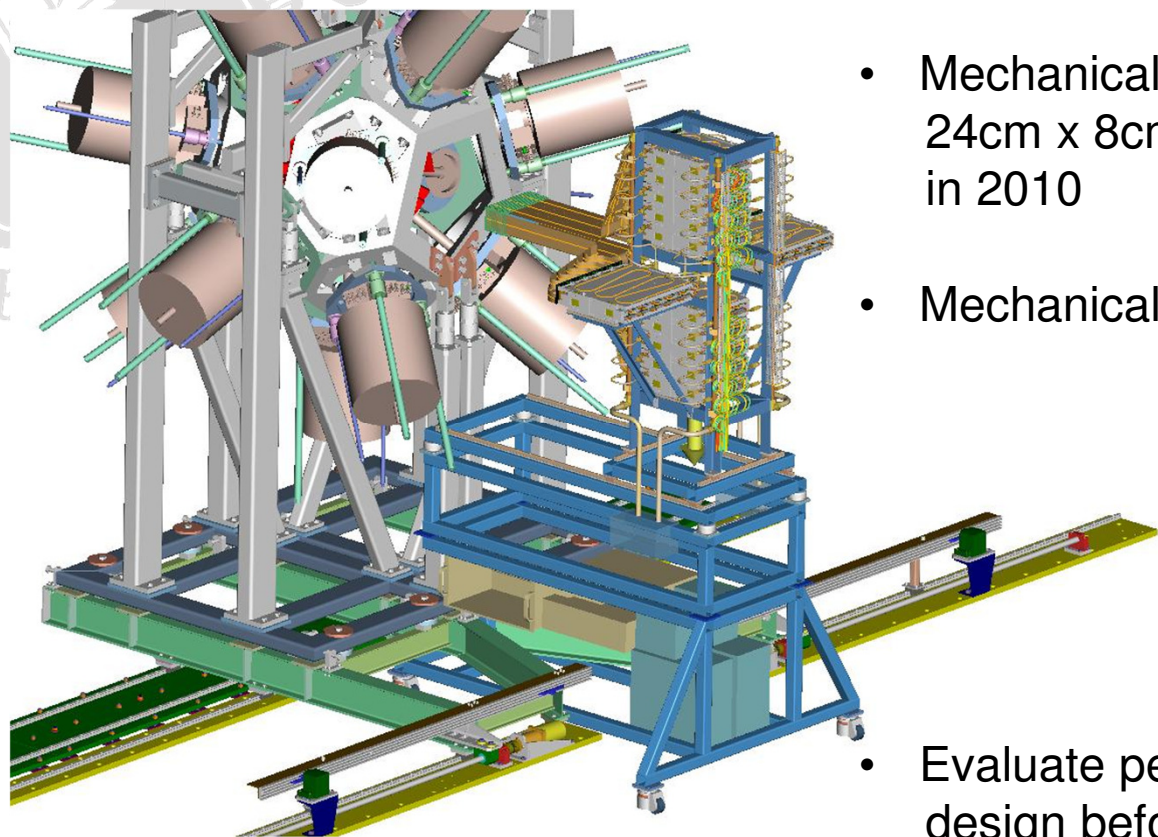
- *minimal package size*
- *minimal material budget*
- *lifetime maximisation*
- *performance impact*

Package size 10cm x 10cm

Snout length 568mm



AIDA Mechanical



- Mechanical design for 8cm x 8cm and 24cm x 8cm DSSSDs was completed in 2010
- Mechanical support assembly completed
- Evaluate performance of 8cm x 8cm design before proceeding to manufacture of 24cm x 8cm design
- Design compatible with BELEN, TAS, MONSTER, RISING, FATIMA etc

- Design drawings (PDF) available
<http://www.eng.dl.ac.uk/secure/np-work/AIDA/>

AIDA: status

- DSSSD with sub-contractor (MSL)
 - 8cm x 8cm & 24 x 8cm mechanical samples
 - 4x 8cm x 8cm prototypes delivered
 - 8x 8cm x 8cm wafers + additional 0.5 μ m passivation
 - 4x 8cm x 8cm wafers on order for 2014/Q1
- Production hardware (ASIC, FEE Mezzanine PCB, FEE PCB) delivered by sub-contractors
- FEE64 Mezzanine assembly
 - 78 completed and delivered
- FEE64 PCB
 - 50 OK
 - 19 (1 of 64) channels noisy, otherwise OK
 - 6 with faults requiring further tests
- FEE module assembly
 - 32 complete and tested OK
 - *8x 8cm x 8cm DSSD stack requires 16x FEE modules*

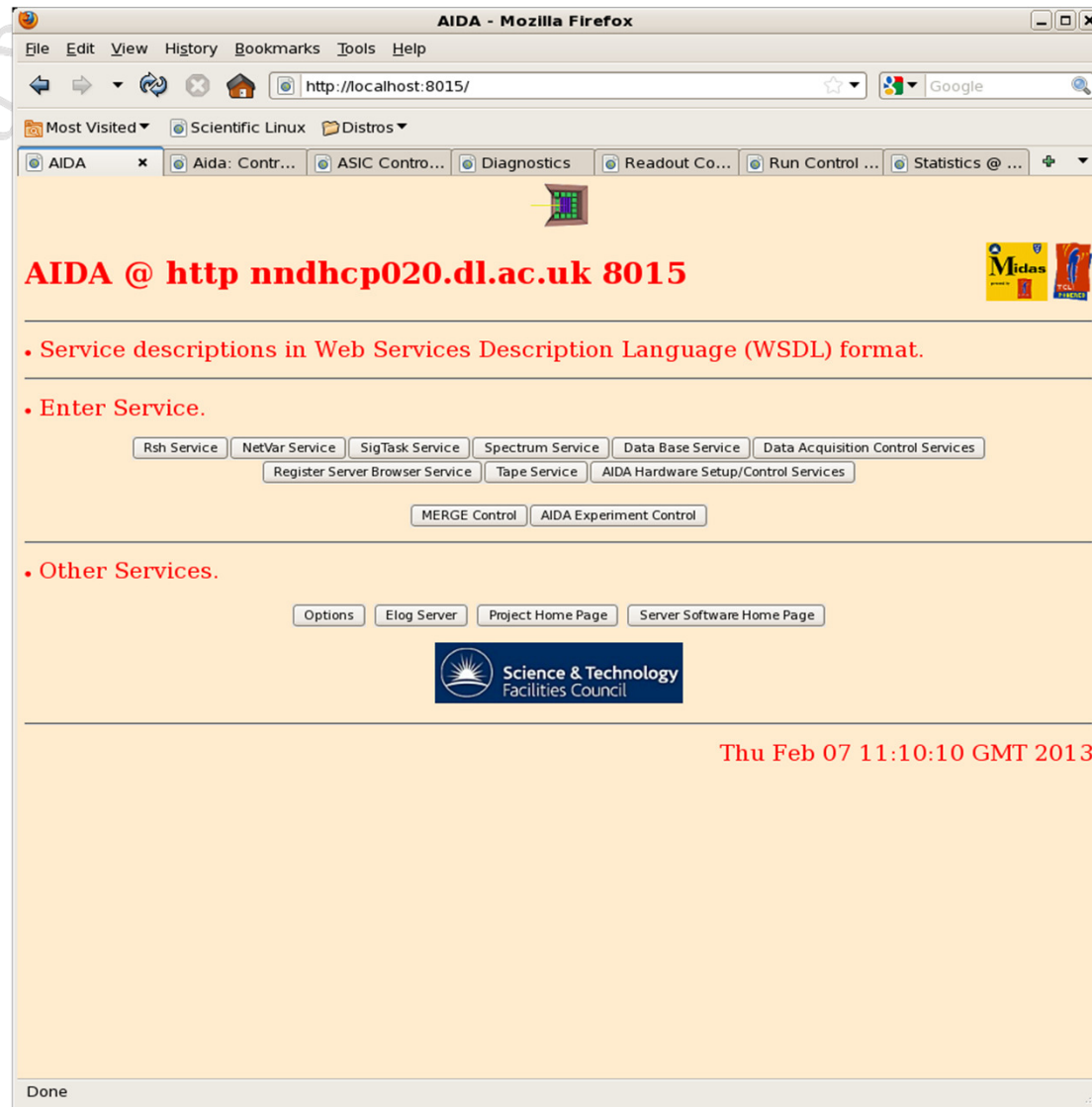
AIDA: status

- MACB timestamp distribution system for FEE modules
 - delivery complete
- Mechanical design and infrastructure (HV, PSUs, cooling etc.)
 - detector HV, FEE PSUs, cooling & FEE crates delivered
 - support assembly completed

AIDA: outlook

- AIDA production hardware was available for commissioning on schedule in 2011/Q3
- Performance of 20GeV & 1GeV ranges meets specification
 - *need to optimise DSSSD-FEE coupling for 20MeV range*
 - *progress very encouraging*
- Basic data merge with MBS successfully demonstrated during AIDA+LYCCA test May 2011
 - *further work required*
- Continuing FEE firmware development work in progress
 - *DSP (64 channel digital CFD being tested)*
- DAQ software development work in progress
 - interface migrated from Tcl/Tk to XML/SOAP (web-based)
 - control and management of multiple FEE modules
 - timestamp-ordered data merge (GREAT format)

AIDA: homepage



AIDA: DAQ main menu

Aida: Control @ mndhcp020.dl.ac.uk client address is 127.0.0.1

Select Hardware FEE64 Act on ALL FEE64 modules? ☒

Local Controls ASIC Control FADC Align & Control Timestamp Control Master Timestamp Control MBS status & control Data Readout

LED Controls Waveform capture controls Temperatures

ADC Control Hardware Diagnostics

Save/Restore Settings Perform TimeStamp RESYNC Power Relay Control

[FEE64 system software interface documentation](#)

System functions (Expert users only for test/debugging purposes!!!) Select required function

Empty Log Window Send Log Window to ELog Reload Reset Show Variables Show Log Window Enable Logging

Last Updated: February 19, 2013 09:43:08

Done

AIDA: experiment control

Run Control @ nndhpc020.dl.ac.uk - Mozilla Firefox

File Edit View History Bookmarks Tools Help

http://localhost:8015/DataAcquisitionControl/DataAcquisitionContro

Most Visited Scientific Linux Distro

AIDA Aida: Contr... ASIC Contro... Diagnostics Readout Co... Run Co... Statistics @ ...

Data Acquisition Run Control @ http nndhpc020.dl.ac.uk 8015 client address is 127.0.0.1

Acquisition Servers nnaida8 Act on ALL Data Acquisition Servers? ☒

RESET **STOP**

nnaida12	going	H	nnaida11	going	H	nnaida10	going	H	nnaida9	going	H
nnaida8	going	H	nnaida7	going	H	nnaida6	going	H	nnaida4	going	H

Histogramming Data transfer

System functions (Only use if you know what they do!!!)

Last Updated: February 18, 2013 15:02:57

[Home](#) [Service Definition](#)

Done

Note – illustrates configuration controlling 8x FEE64 cards

AIDA: DAQ statistics

Statistics @ nndhcp020.dl.ac.uk - Mozilla Firefox

File Edit View History Bookmarks Tools Help

http://localhost:8015/DataAcquisitionControl/DataAcquisitionStats.tr

Most Visited Scientific Linux Distro

AIDA Aida: Contr... ASIC Contro... Diagnostics Readout Co... Run Control ... Statistic...

Data Acquisition Statistics @ http nndhcp020.dl.ac.uk 8015 client address is 127.0.0.1

Acquisition Servers nnaida4 Current Acquisition Server nnaida4 Show ALL Data Acquisition Servers?

Counters

Poll	1055208436	Empty events	0	Histogram increments	61243633	Transmit buffers	0
Transmit data	0	Null events	0	FIFO empty	0	No Data	0
FIFO part full	0	Bad Data	0	Event not accepted	0	TX2 buffers	0
Good Events	88230460	Transfer Error	0	Transfer Wait	0	Disc data blocks	0
TX2 data	0	TX2 errors	0	TX2 wait	0	AIDA data	162817984
ASIC data blocks	0	AIDA ASIC events	0	AIDA errors	0	AIDA Time Warp	0
SYNC Time Warp	150	ASIC data	0	DISC data	0	AIDA bad data #4	0
AIDA bad data #1	0	AIDA bad ASIC	0	AIDA bad range	0	AIDA PAUSE	4544
AIDA bad data #5	0	Discriminator data	78926068	AIDA SYNC	111168700	MBS Scaler H	0
AIDA RESUME	4544	MBS Scaler L	0	MBS Scaler M	0	WAVE DMA Blocks	2022
ASIC Events	88230460	WAVE Events	403810	ASIC DMA Blocks	1347	WAVE item skipped	805936
WAVE event empty	3160	WAVE not accepted	3160	WAVE good events	29137634	WAVE SYNC	28733821
WAVE buffer too short	1578	WAVE format error #1	0	WAVE format error #2	4		
WAVE PAUSE	3	WAVE RESUME	0				

Rates

Poll	12858	Empty events	0	Histogram increments	12706	Transmit buffers	0
Transmit data	0	Null events	0	FIFO empty	0	No Data	0
FIFO part full	0	Bad Data	0	Event not accepted	0	TX2 buffers	0
Good Events	12858	Transfer Error	0	Transfer Wait	0	Disc data blocks	0
TX2 data	0	TX2 errors	0	TX2 wait	0	AIDA data	35196
ASIC data blocks	0	AIDA ASIC events	0	AIDA errors	0	AIDA Time Warp	0
SYNC Time Warp	0	ASIC data	0	DISC data	0	AIDA bad data #4	0
AIDA bad data #1	0	AIDA bad ASIC	0	AIDA bad range	0	AIDA PAUSE	4
AIDA bad data #5	0	Discriminator data	15628	AIDA SYNC	600	MBS Scaler H	0
AIDA RESUME	4	MBS Scaler L	0	MBS Scaler M	0	WAVE DMA Blocks	0
ASIC Events	12858	WAVE Events	0	ASIC DMA Blocks	1	WAVE item skipped	0
WAVE event empty	0	WAVE not accepted	0	WAVE good events	0	WAVE SYNC	0
WAVE buffer too short	0	WAVE format error #1	0	WAVE format error #2	0		
WAVE PAUSE	0	WAVE RESUME	0				

Empty Log Window Send Log Window to ELog Reload Reset Show Variables Show Log Window Enable Logging

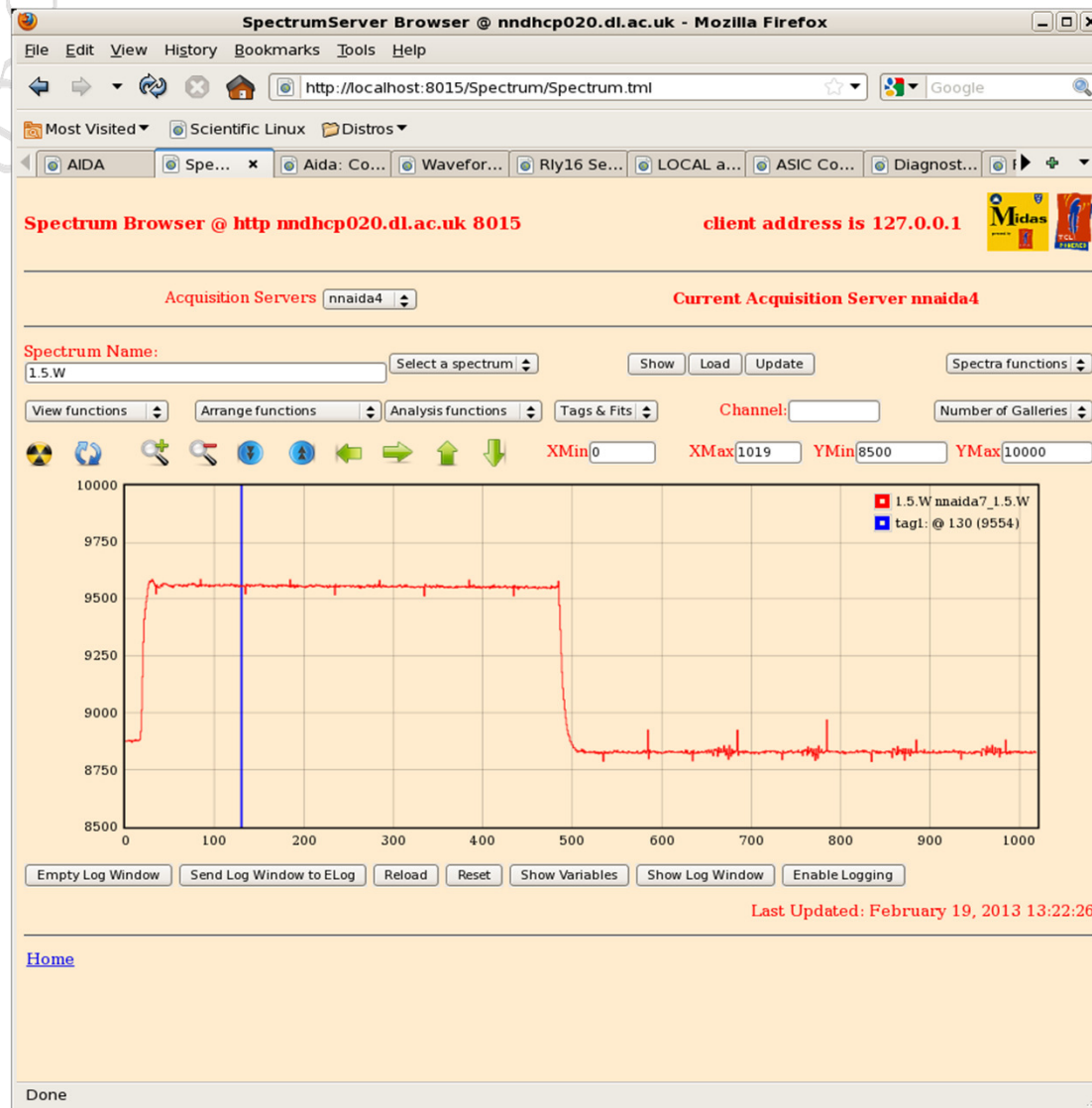
Zero Statistics Update Once AutoUpdate On

Last Updated: February 19, 2013 11:54:34

[Home](#)

Done

AIDA: preamplifier waveform capture



Data from AD9228 Octal, 50MSPS, 14-bit ADC

AIDA: Support Assembly



*'All up' tests in T4 laboratory STFC Daresbury Laboratory
Note Julabo Recirculating Chiller to side of assembly*

AIDA: MACB



Timestamping hardware with HDMI cabling to AIDA FEE modules

AIDA: FEE Power Supply



*Power Supply Unit (bottom) controlled by Relay unit (top).
Note Raspberry Pi on top of Relay Unit which provides remote control via web*

AIDA: Relay Control

Rly16 Service @ nnrpi1 - Mozilla Firefox

File Edit View History Bookmarks Tools Help

http://193.62.115.7:8015/AIDA/Rly16/

Most Visited Scientific Linux Distros

AIDA Aida: Co... Rly1... LOCAL a... ASIC Co... Diagnost... Readout ... Run Con...

Rly16 Control @ http nnrpi1 8015 **client address is 193.62.115.20**

Port: /dev/ttyUSB0 Version: 0901 DC: 12.2V

Switch ON Switch OFF

Relay 1 Relay 2 Relay 3 Relay 4 Relay 5 Relay 6 Relay 7 Relay 8

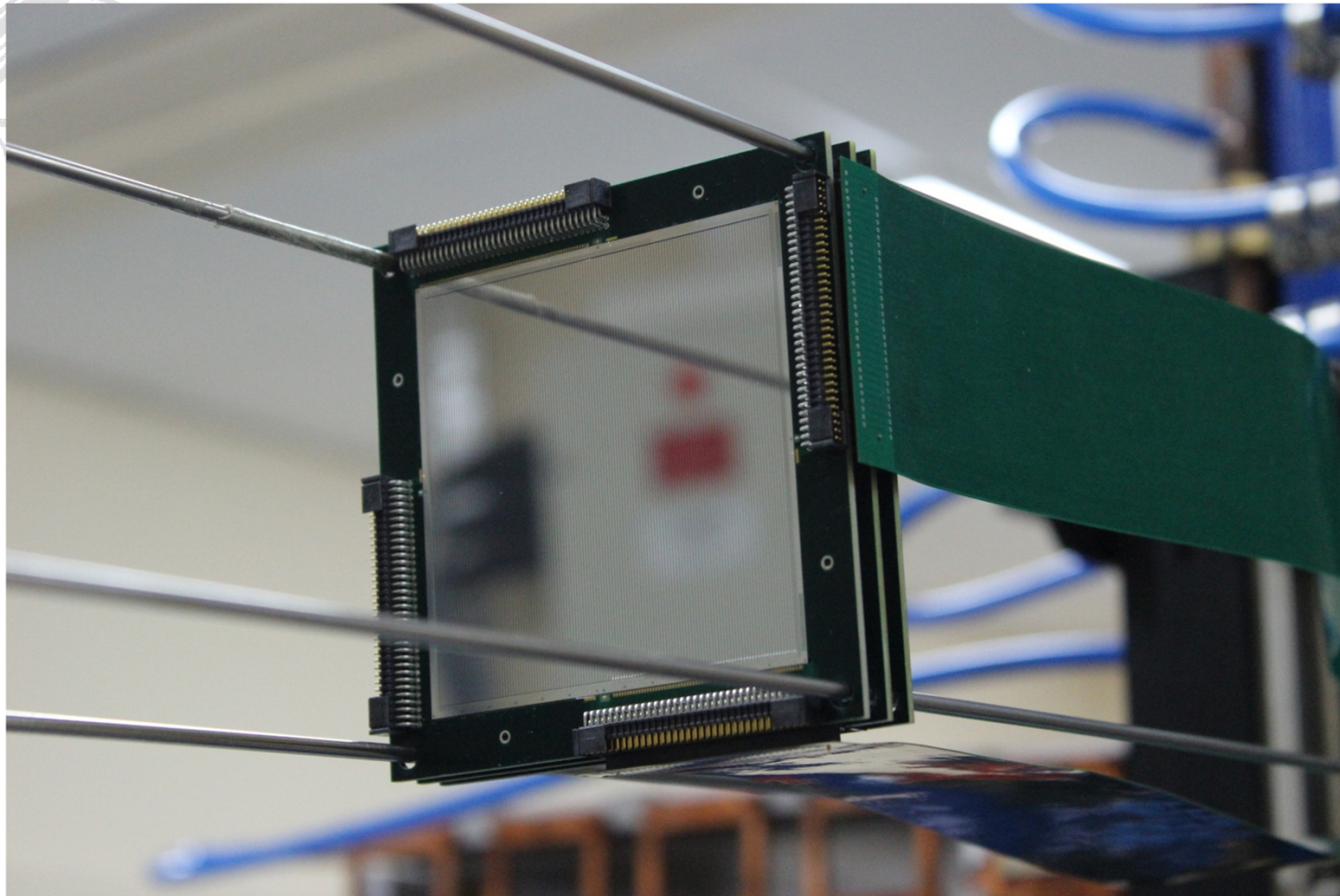
Switch ALL On Switch ALL Off

Empty Log Window Send Log Window to ELog Reload Reset Show Variables Show Log Window Enable Logging

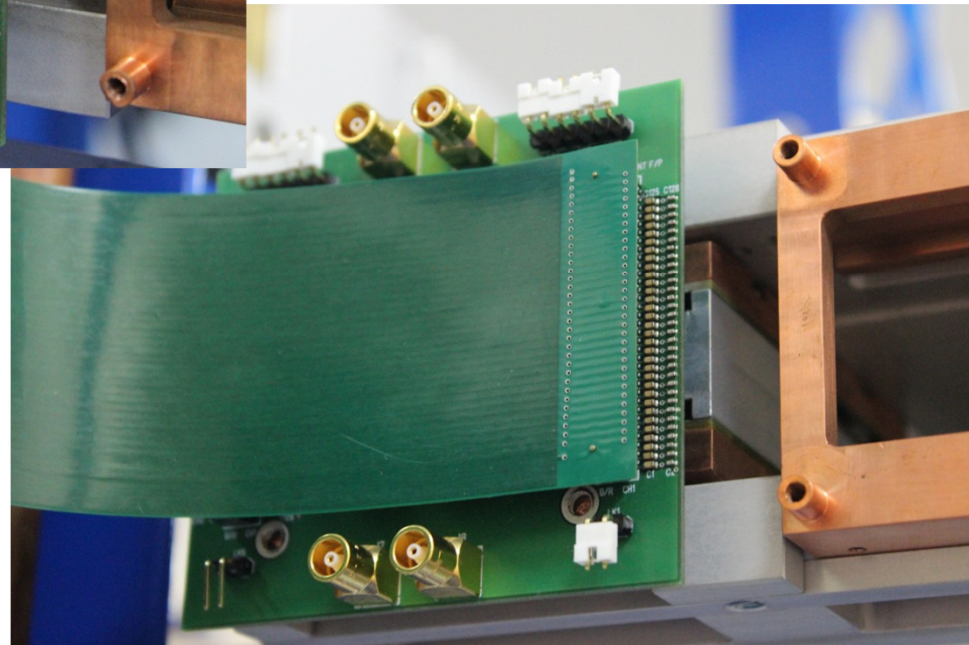
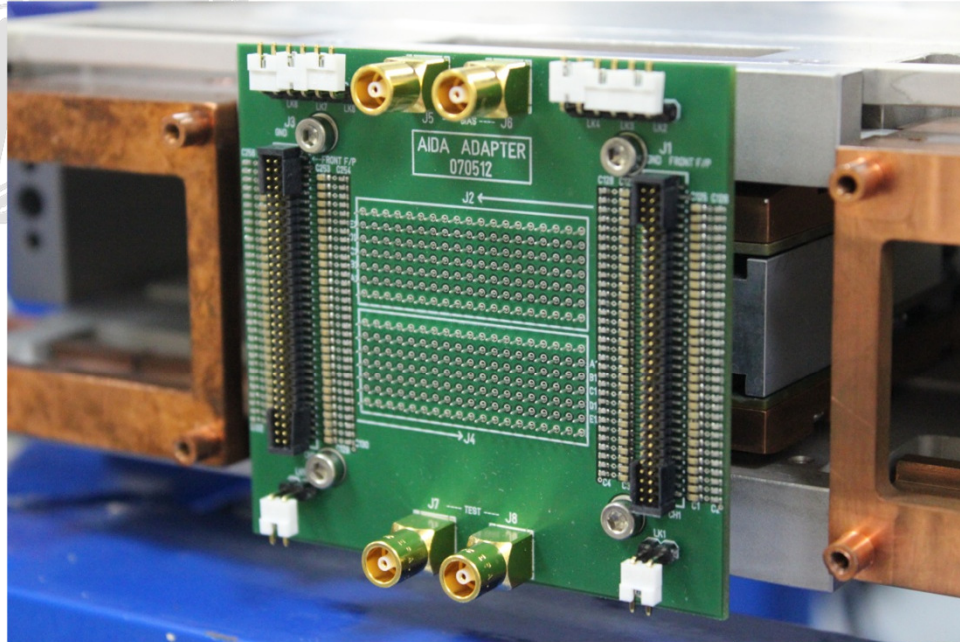
Last Updated: February 19, 2013 11:58:36

Done

AIDA: MSL type BB18-1000 + Kapton cabling



AIDA: Adaptor PCB with Kapton Cabling



Acknowledgements

My thanks to:

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University of Brighton

O. Roberts

GSI

F. Amek, L. Cortes, J. Gerl, E. Merchan, S. Pietri *et al.*

AIDA: Project Partners

- The University of Edinburgh (lead RO)

Phil Woods et al.

- The University of Liverpool

Rob Page et al.

- STFC DL & RAL

John Simpson et al.

Project Manager: *Tom Davinson*

Further information: <http://www.ph.ed.ac.uk/~td/AIDA>

TDR - November 2008:

http://www.ph.ed.ac.uk/~td/AIDA/Design/aida_tdr.pdf