Advanced Implantation Detector Array (AIDA)

Second BRIKEN Workshop

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presented by

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on behalf of the AIDA collaboration

(Edinburgh – Liverpool – STFC DL & RAL)

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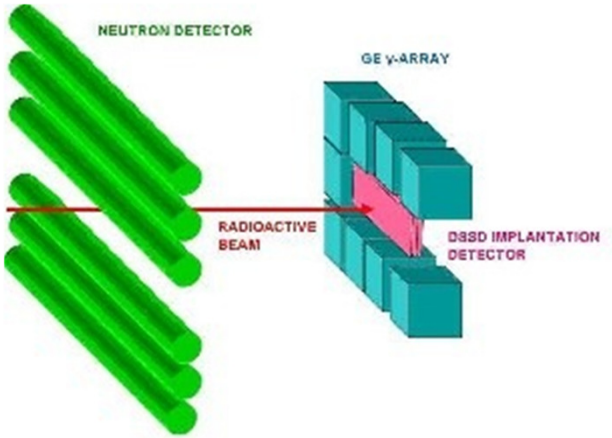
AIDA: Introduction

Advanced Implantation Detector Array (AIDA)

UK collaboration: *University of Edinburgh, University of Liverpool, STFC Daresbury Laboratory & STFC Rutherford Appleton Laboratory*

- SuperFRS
- Exotic nuclei ~ 50 – 200MeV/u
- Implant – decay correlations
- Multi-GeV implantation events
- Subsequent low-energy decays
- Tag events for gamma and neutron detector arrays

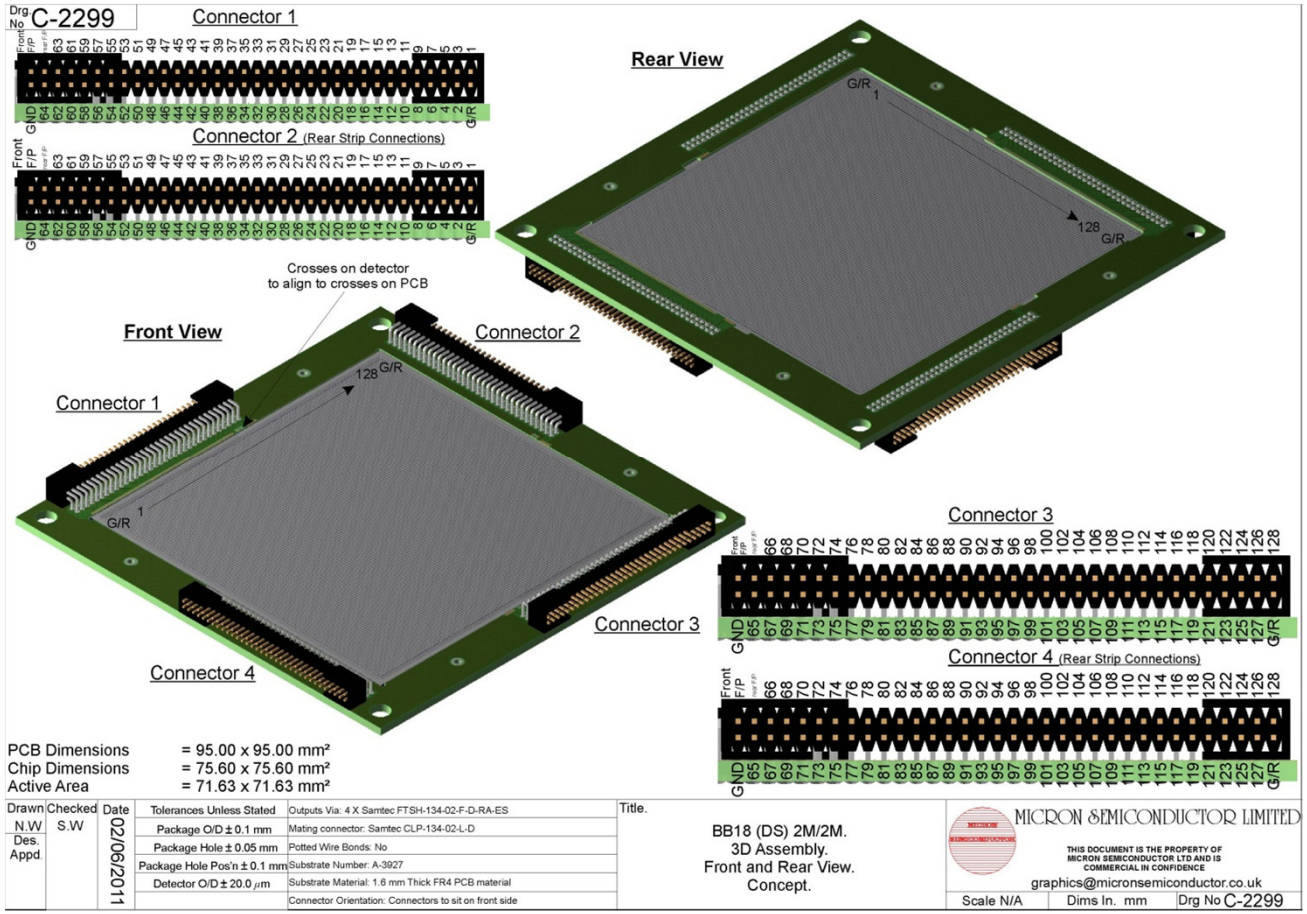


Detector: multi-plane Si DSSD array
wafer thickness 1mm
8cm x 8cm (128x128 strips) *or* 24cm x 8cm (384x128 strips)

Instrumentation: ASIC
low noise (<12keV FWHM), low threshold (0.25% FSR)
20GeV FSR *plus* (20MeV FSR *or* 1GeV FSR)
fast overload recovery (~μs)
spectroscopy performance
time-stamping

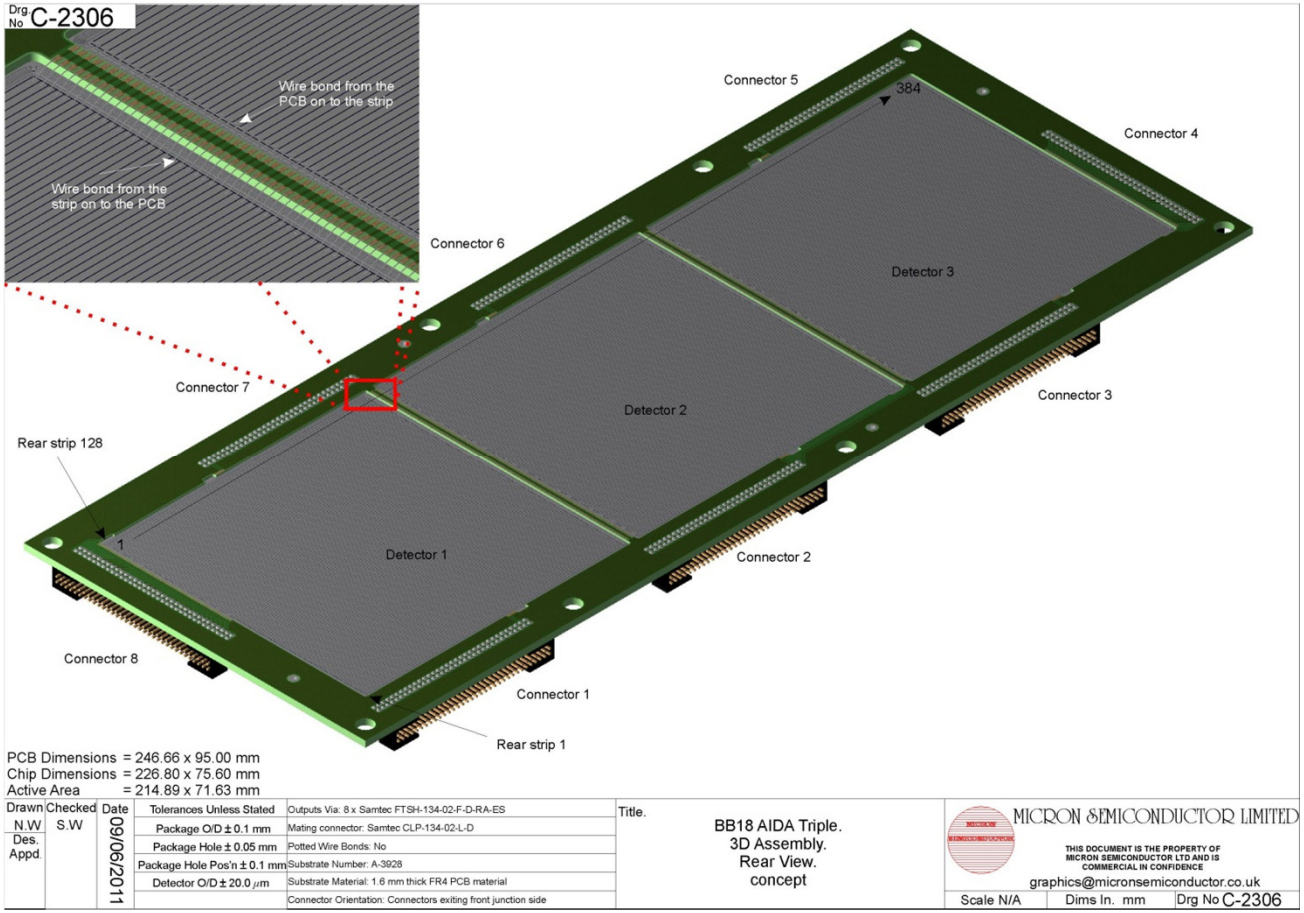
MSL type BB18

128 x 128 strips (16384 pixels)
multi-guard ring
0.560mm strip pitch
1mm wafer thickness



MSL type BB18

384 x 128 strips (49152 pixels)
multi-guard ring
0.560mm strip pitch
1mm wafer thickness

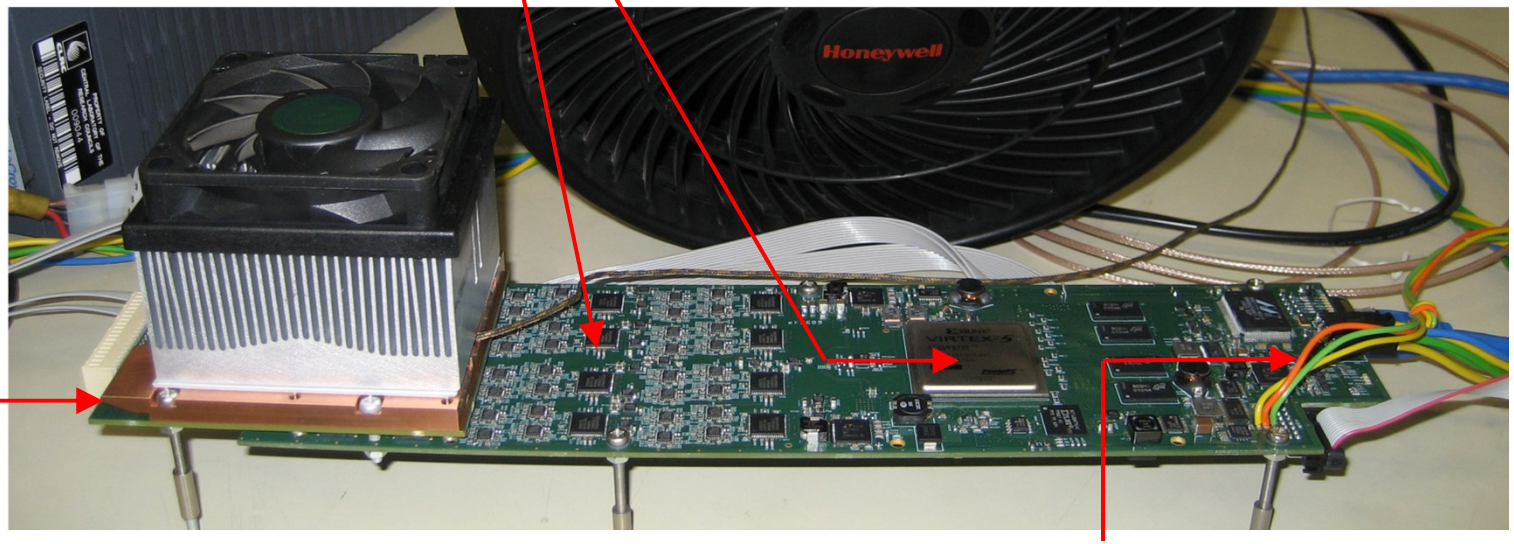


AIDA Hardware

Each FEE64 card acts as an independent DAQ
Each data word encoded with 48-bit timestamp
Data merged at network switch and time-ordered by Linux workstation

Mezzanine:
4x 16 channel ASICs
Cu cover
EMI/RFI/light screen
cooling

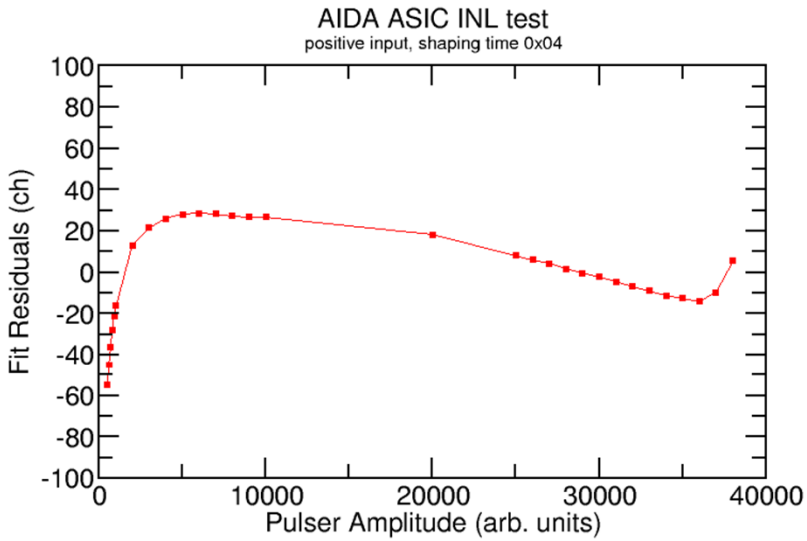
FEE:
4x 16-bit ADC MUX readout (not visible)
8x octal 50MSPS 14-bit ADCs
Xilinx Virtex 5 FPGA
PowerPC 40x CPU core/Linux OS – DAQ



FEE width: 8cm
Prototype – air cooling
Production – recirculating coolant

Gbit ethernet, timestamp, JTAG ports
Power

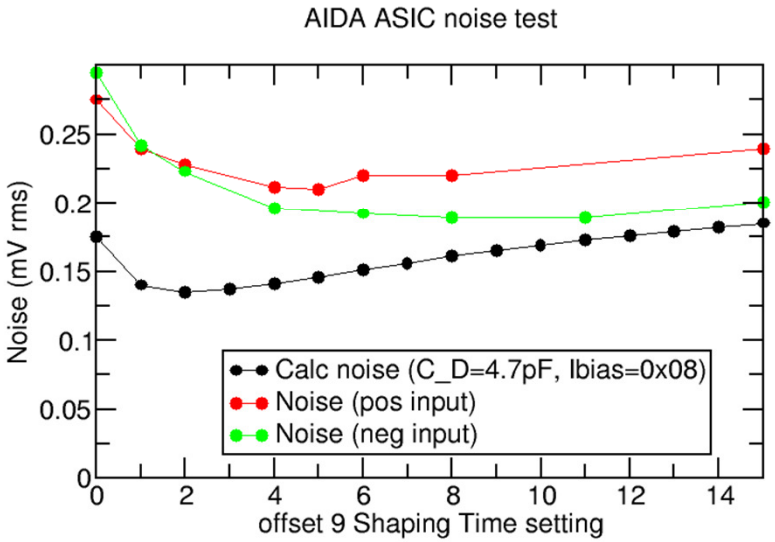
Bench Tests of *Prototype* Hardware



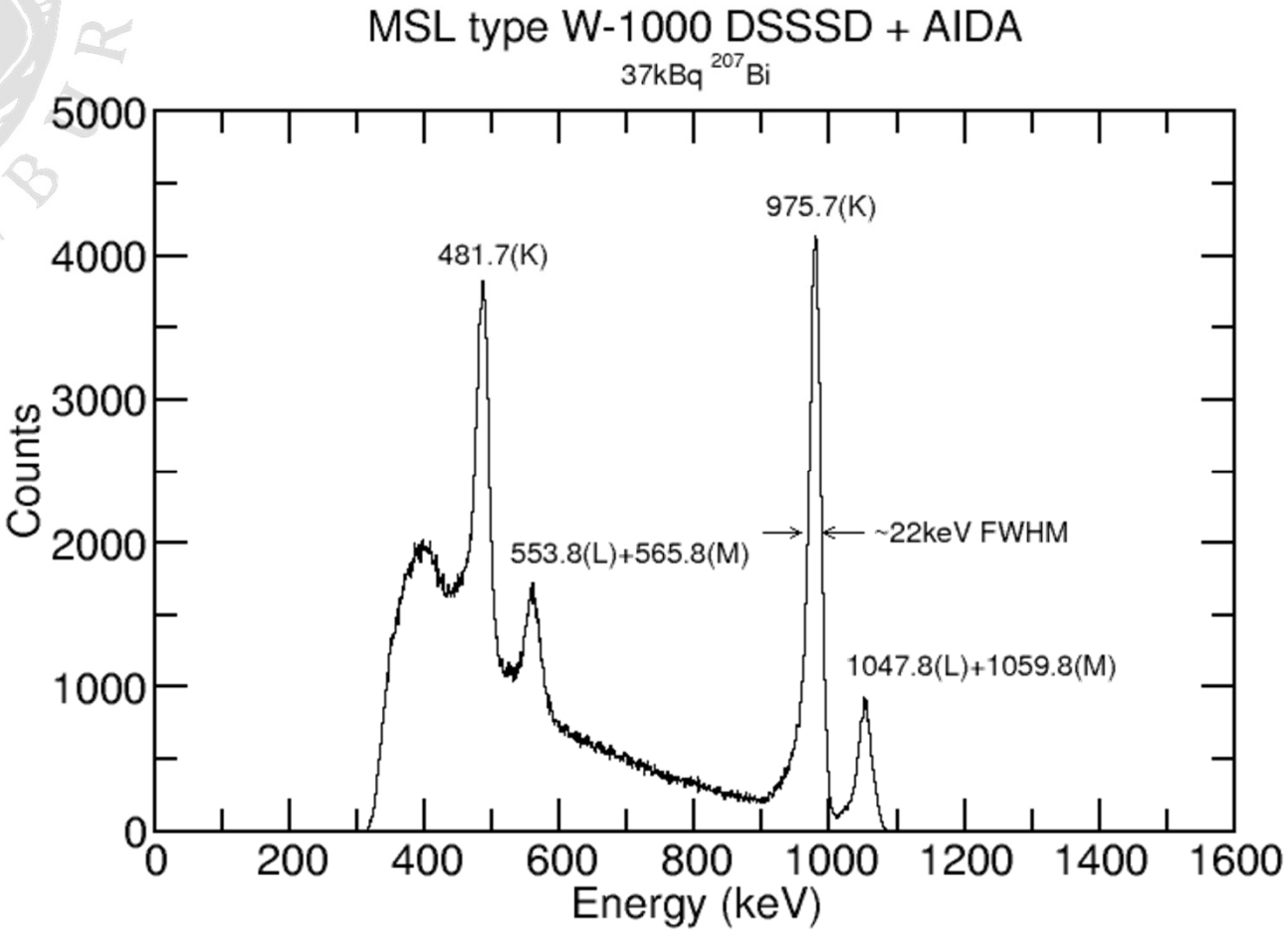
Tests with pulser demonstrating integral non-linearity and noise performance of 20MeV range

INL < 0.1% (> 95% FSR)

0.15mV rms ~ 2.5keV rms Si

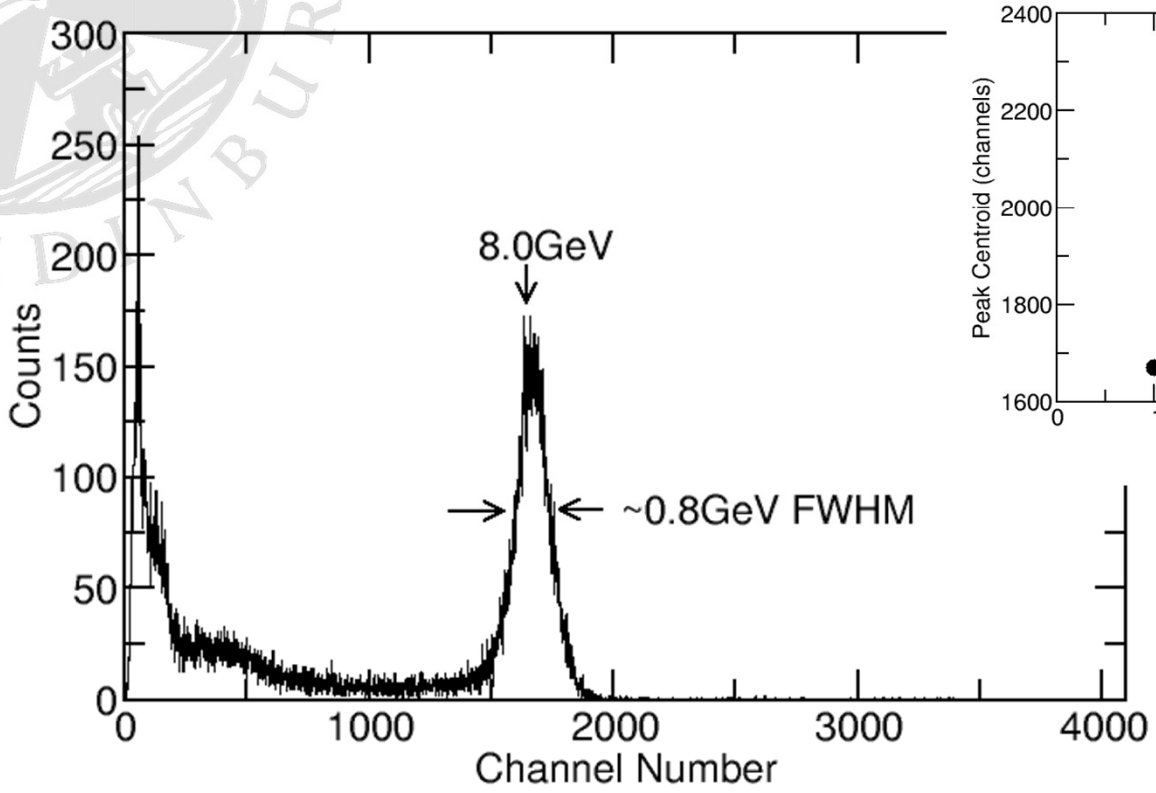


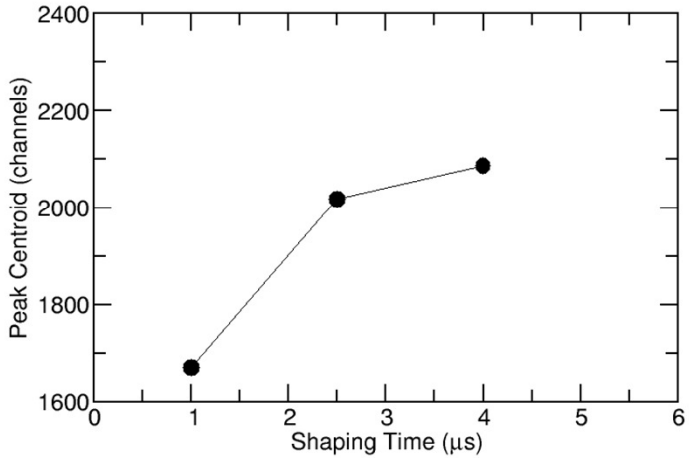
Tests with AIDA *Production* Hardware: 20MeV range



- Realistic input loading C_D ~ 60pF, I_L ~ 60nA
- Expectation ~12keV FWHM

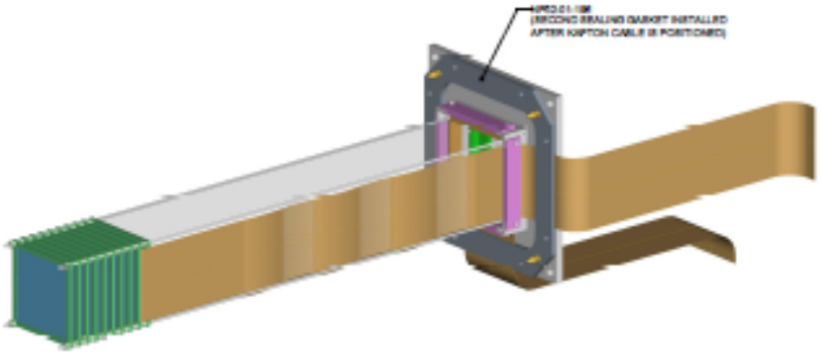
Tests with AIDA *Production* Hardware: 20GeV range



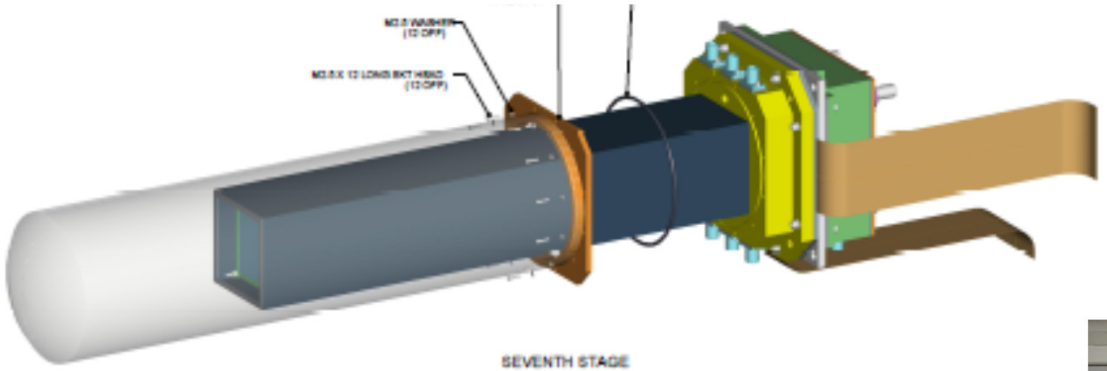


- SIS 250MeV/u ^{209}Bi
- Beam delivery direct to HTC
- Significant ballistic deficit effects
- Confirms Bardelli model and previous TAMU observations
- Implies preamp risetime for high energy heavy-ions >500ns
  (cf. intrinsic preamp risetime ~90ns)

8cm x 8cm AIDA Enclosure



SECOND STAGE



SEVENTH STAGE

DSSSD - instrumentation via Kapton PCB

- minimal package size

- minimal material budget

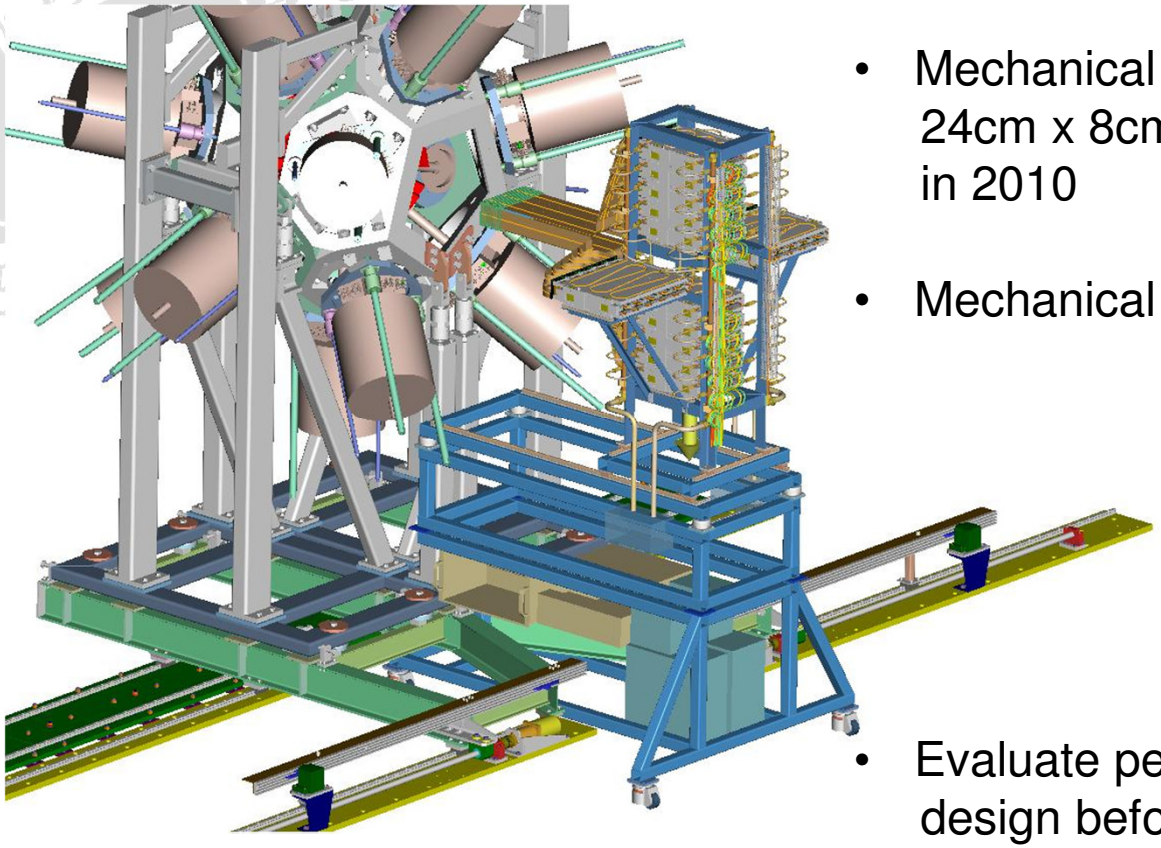
- lifetime maximisation

- performance impact

Package size 10cm x 10cm

Snout length 568mm

AIDA Mechanical



- Mechanical design for 8cm x 8cm and 24cm x 8cm DSSSDs was completed in 2010
- Mechanical support assembly completed
- Evaluate performance of 8cm x 8cm design before proceeding to manufacture of 24cm x 8cm design
- Design compatible with BELEN, TAS, MONSTER , RISING, FATIMA etc

- Design drawings (PDF) available
  http://www.eng.dl.ac.uk/secure/np-work/AIDA/

AIDA: status

- DSSSD with sub-contractor (MSL)
  - 8cm x 8cm & 24 x 8cm mechanical samples
  - 4x 8cm x 8cm prototypes delivered
  - 8x 8cm x 8cm wafers + additional 0.5µm passivation
  - 4x 8cm x 8cm wafers on order for 2014/Q1

- Production hardware (ASIC, FEE Mezzanine PCB, FEE PCB) delivered by sub-contractors

- FEE64 Mezzanine assembly
  - 78 completed and delivered

- FEE64 PCB
  - 50 OK
  - 19 (1 of 64) channels noisy, otherwise OK
  - 6 with faults requiring further tests

- FEE module assembly
  - 32 complete and tested OK
  - *8x 8cm x 8cm DSSD stack requires 16x FEE modules*

AIDA: status

- MACB timestamp distribution system for FEE modules
  - delivery complete

- Mechanical design and infrastructure (HV, PSUs, cooling etc.)
  - detector HV, FEE PSUs, cooling & FEE crates delivered
  - support assembly completed

AIDA: outlook

- AIDA production hardware was available for commissioning on schedule in 2011/Q3

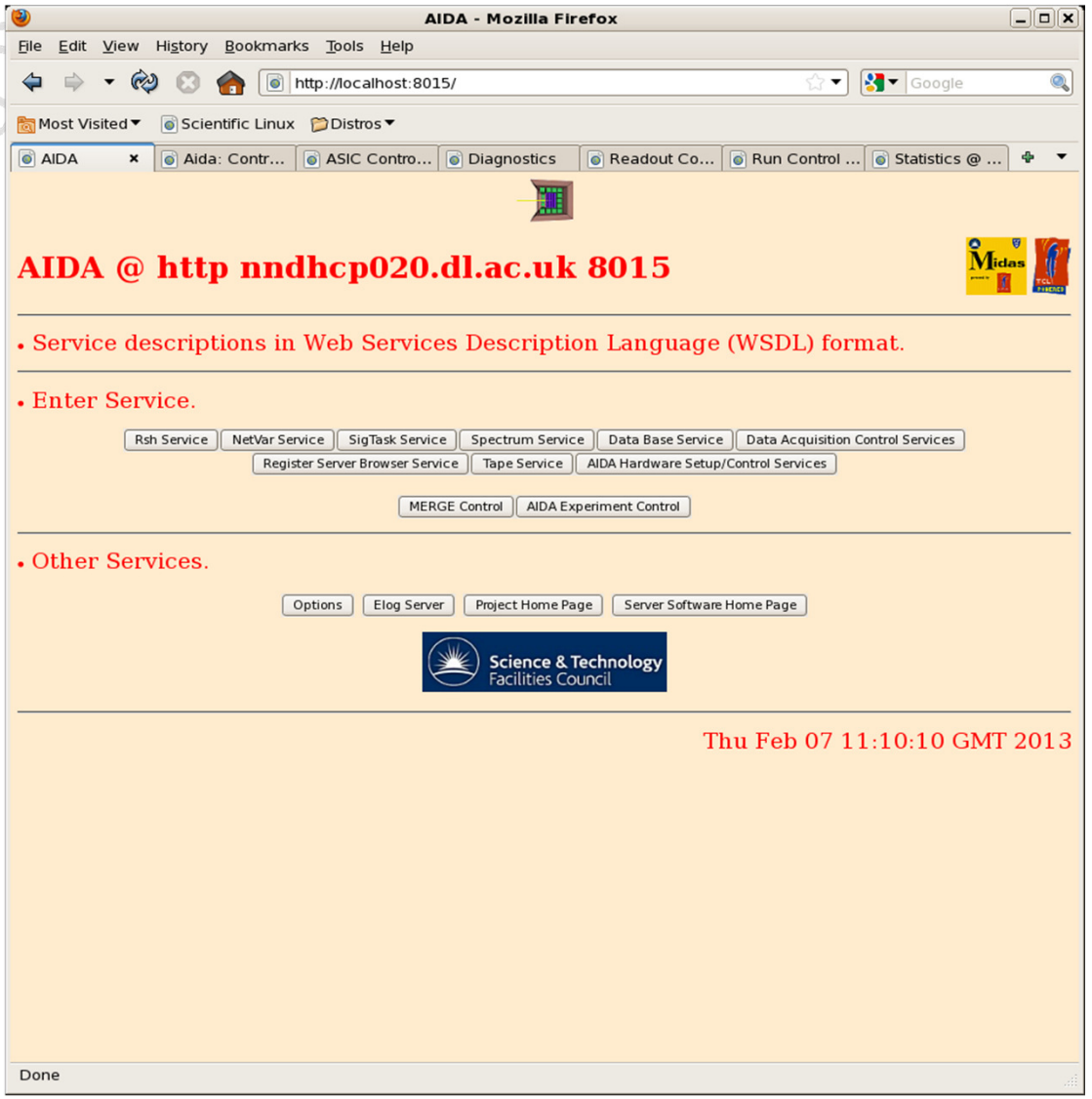
- Performance of 20GeV & 1GeV ranges meets specification
  - *need to optimise DSSSD-FEE coupling for 20MeV range*
  - *progress very encouraging*

- Basic data merge with MBS successfully demonstrated during AIDA+LYCCA test May 2011
  - *further work required*

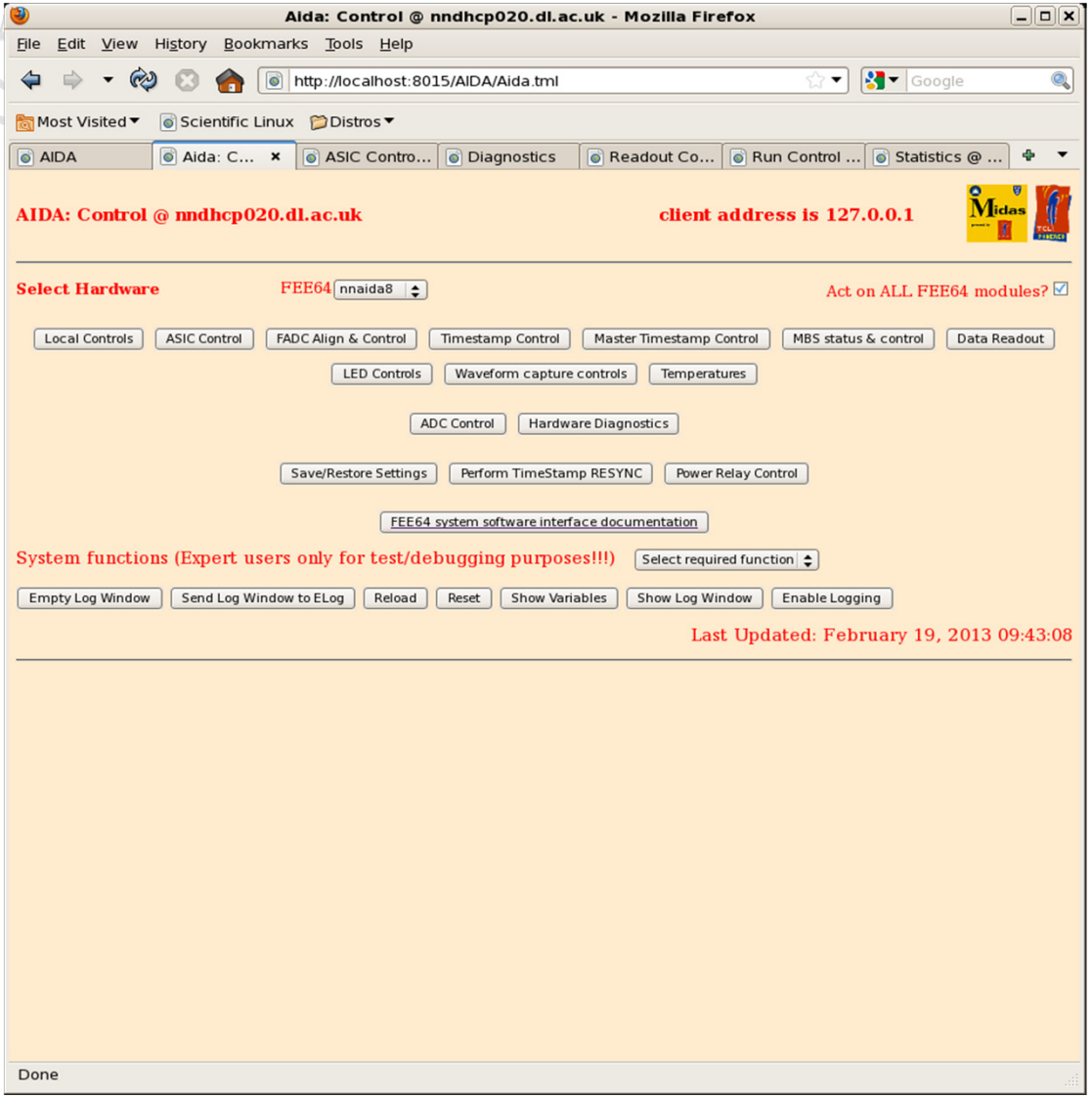
- Continuing FEE firmware development work in progress
  - *DSP (64 channel digital CFD being tested)*

- DAQ software development work in progress
  - interface migrated from Tcl/Tk to XML/SOAP (web-based)
  - control and management of multiple FEE modules
  - timestamp-ordered data merge (GREAT format)

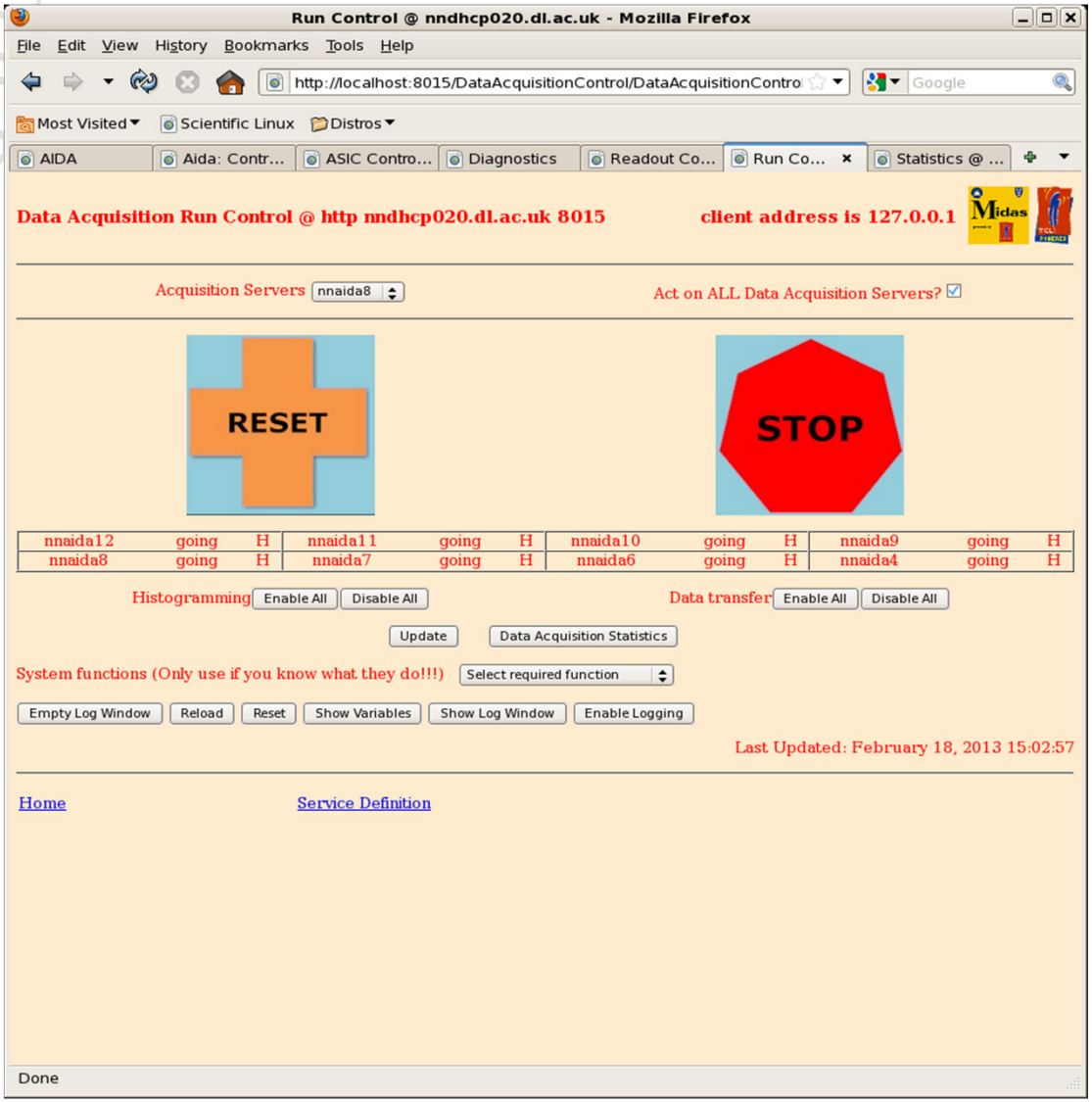
AIDA: homepage



AIDA: DAQ main menu

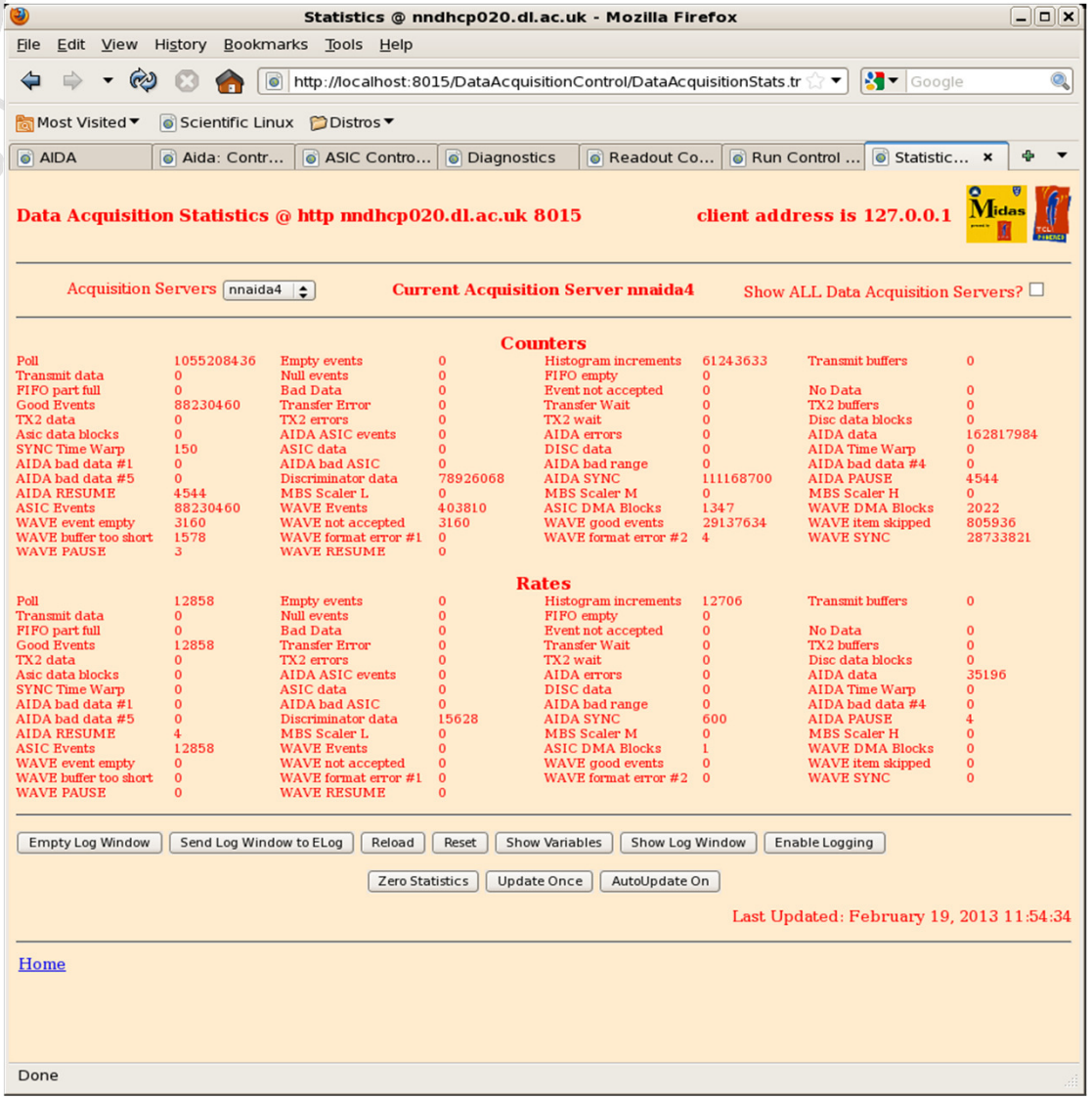


AIDA: experiment control

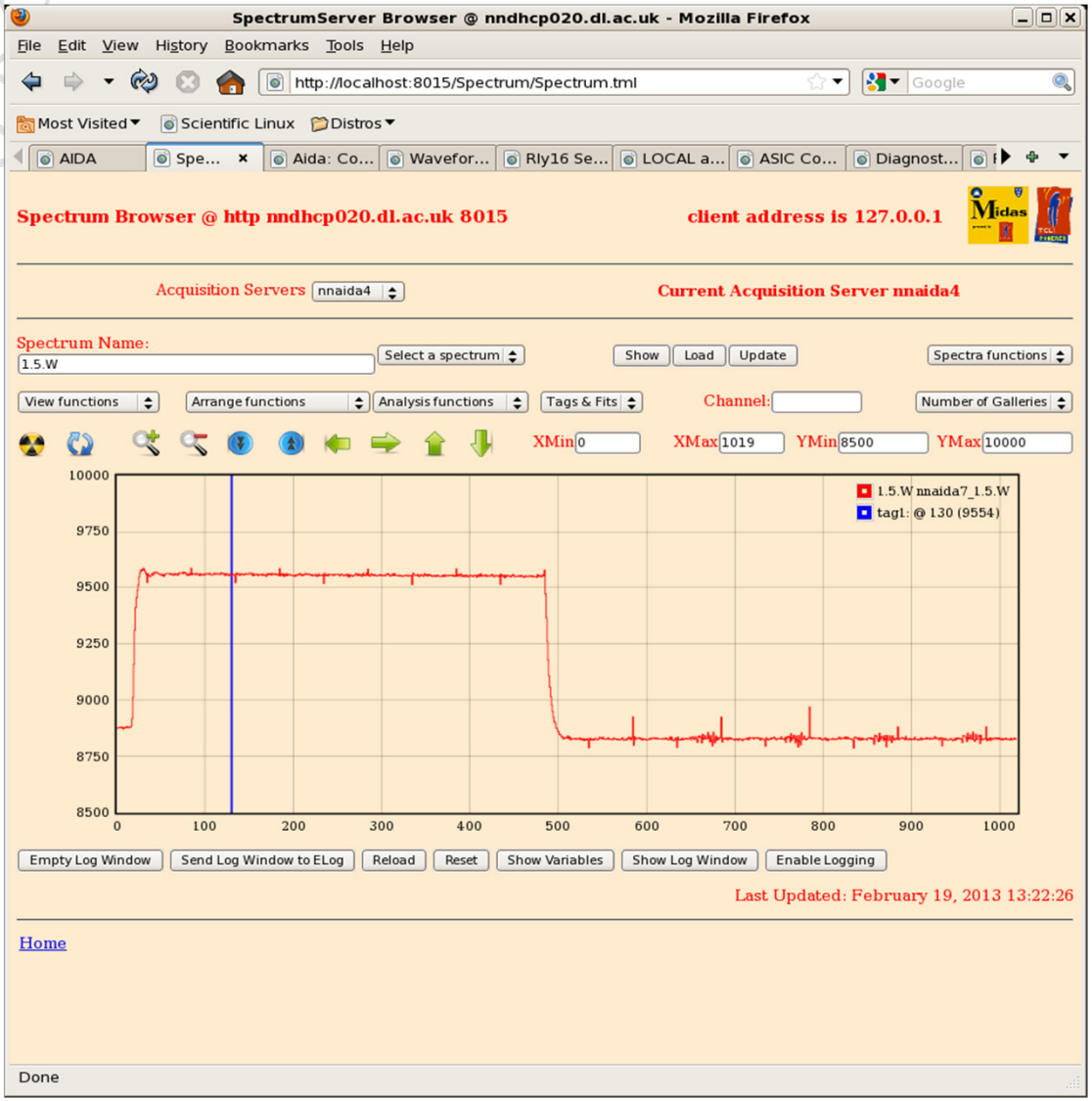


Note – illustrates configuration controlling 8x FEE64 cards

AIDA: DAQ statistics



AIDA: preamplifier waveform capture

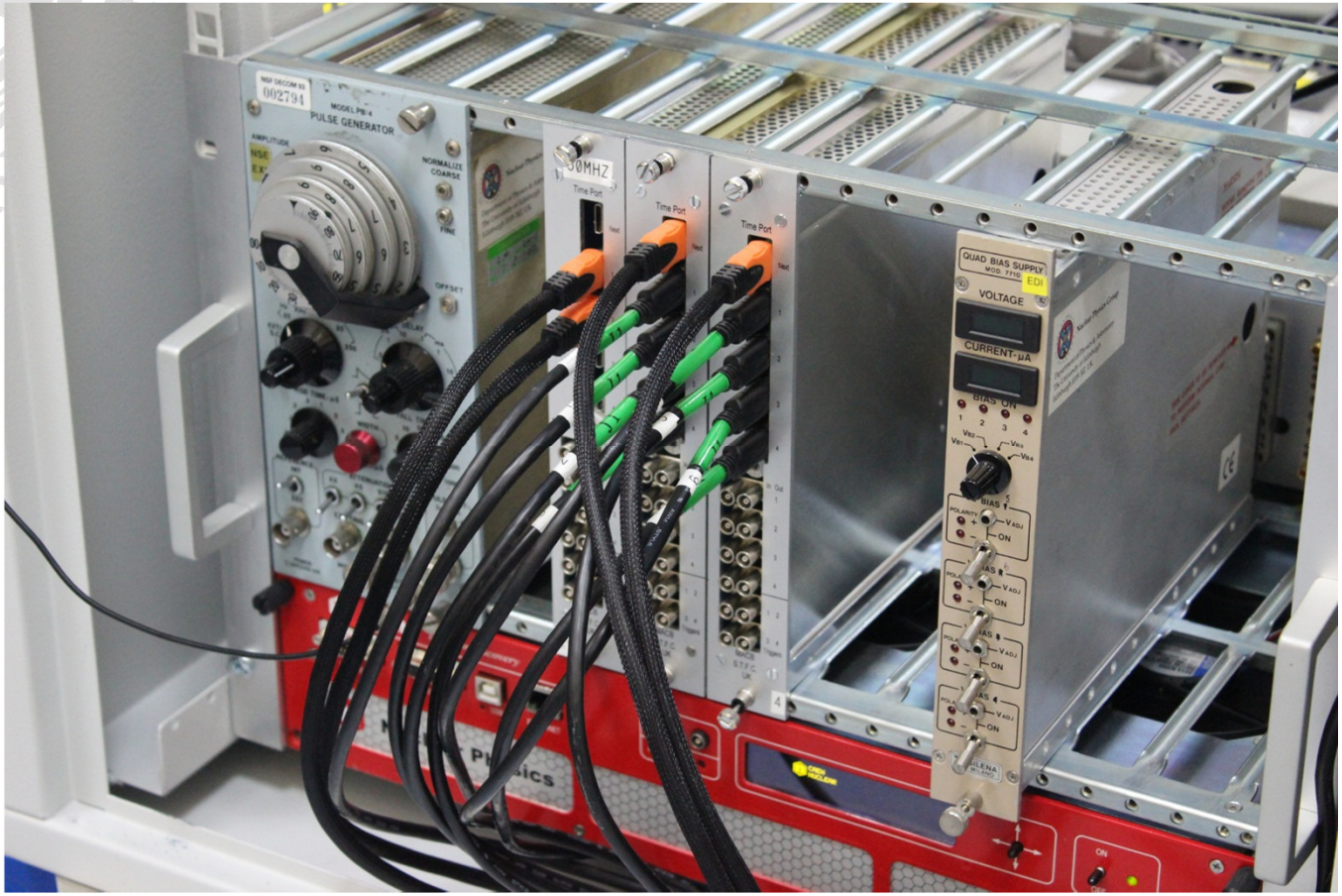


Data from AD9228 Octal, 50MSPS, 14-bit ADC

AIDA: Support Assembly

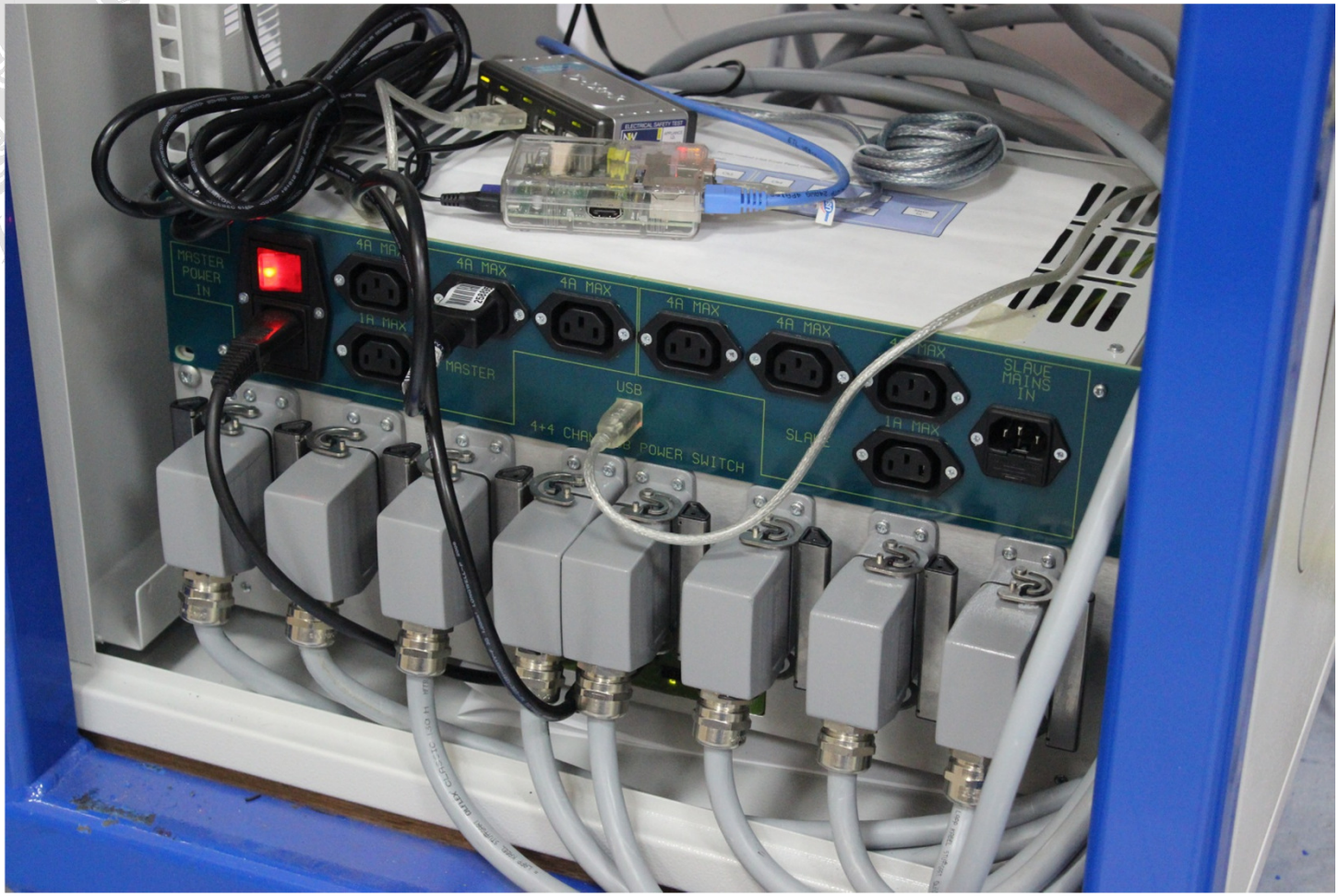
'All up' tests in T4 laboratory STFC Daresbury Laboratory
Note Julabo Recirculating Chiller to side of assembly

AIDA: MACB



Timestamping hardware with HDMI cabling to AIDA FEE modules

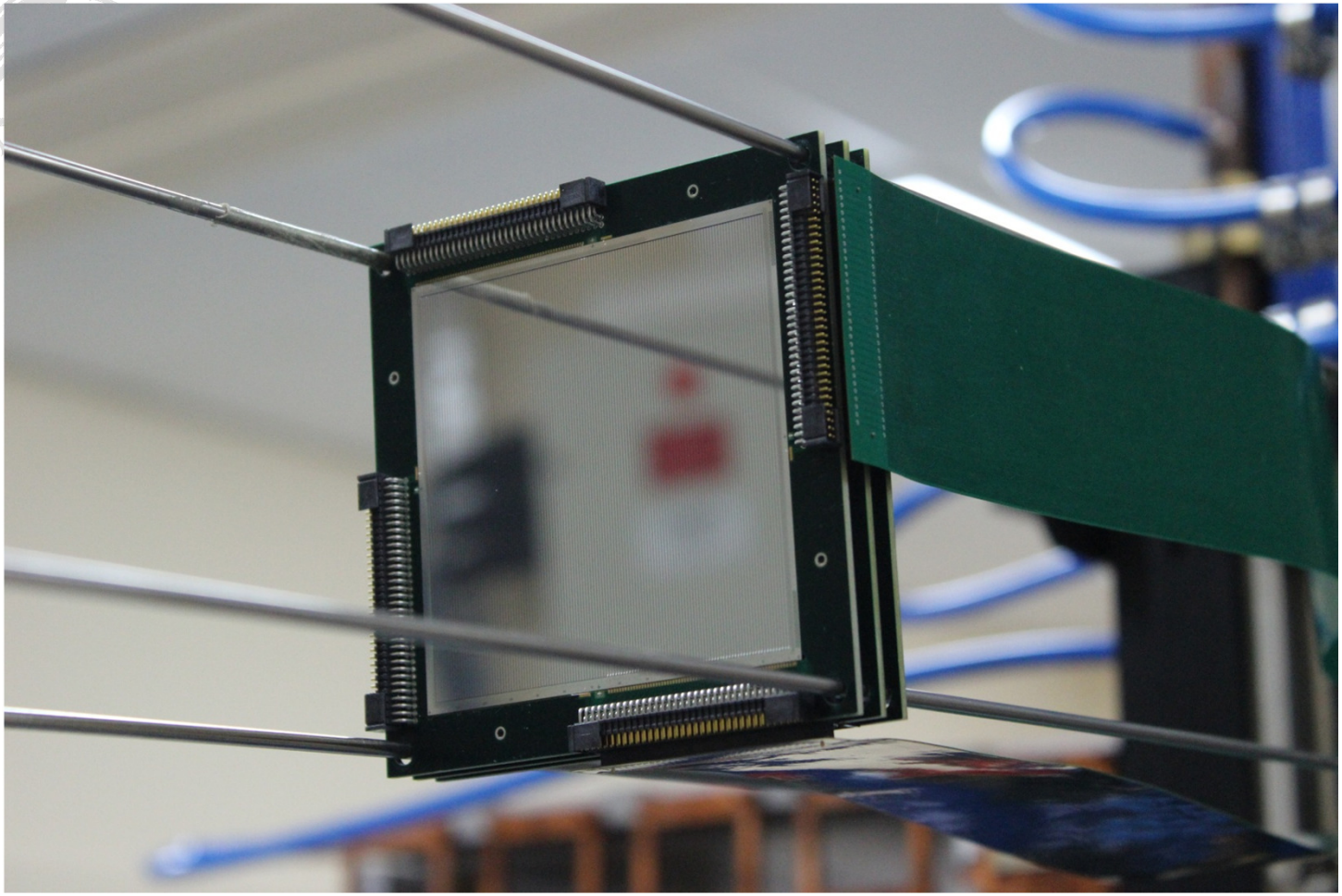
AIDA: FEE Power Supply



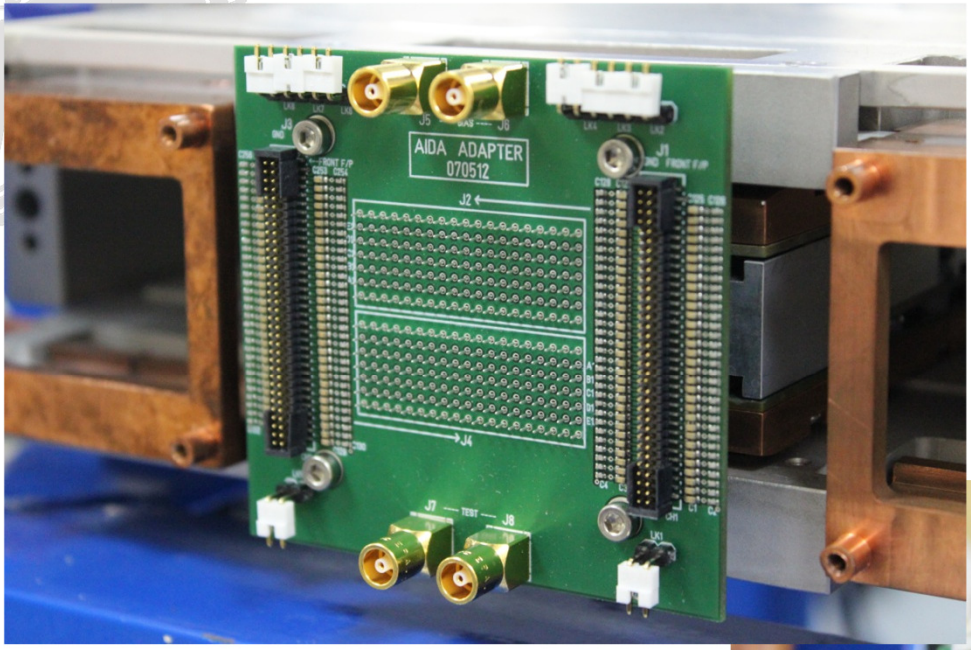
Power Supply Unit (bottom) controlled by Relay unit (top).
Note Raspberry Pi on top of Relay Unit which provides remote control via web

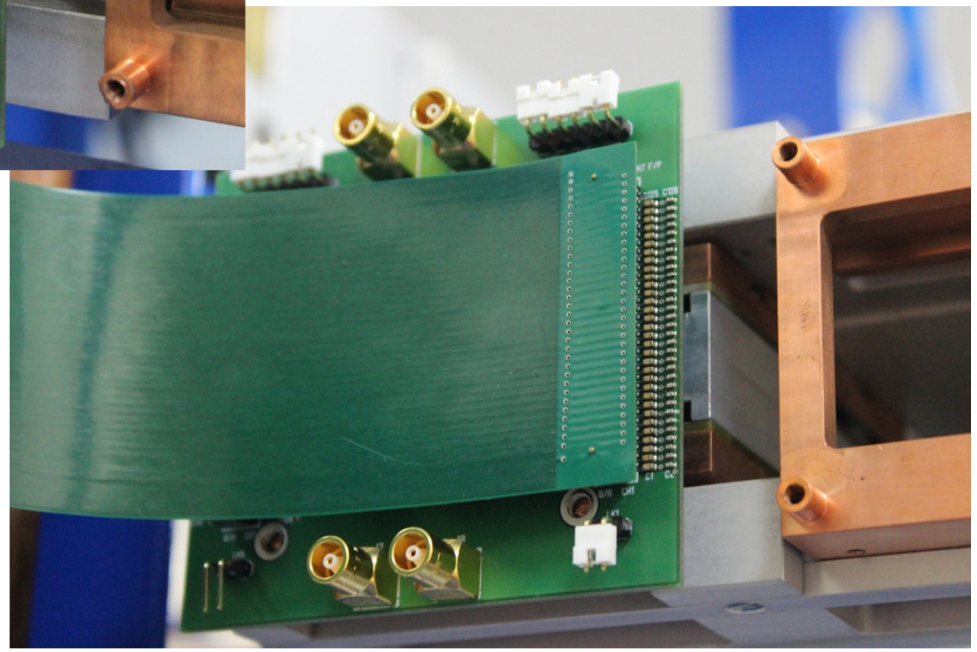
AIDA: Relay Control

AIDA: MSL type BB18-1000 + Kapton cabling



AIDA: Adaptor PCB with Kapton Cabling





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AIDA: Project Partners

- The University of Edinburgh (lead RO)
  Phil Woods *et al.*
- The University of Liverpool
  Rob Page *et al.*
- STFC DL & RAL
  John Simpson *et al.*

Project Manager: Tom Davinson

Further information: http://www.ph.ed.ac.uk/~td/AIDA

TDR - November 2008:
http://www.ph.ed.ac.uk/~td/AIDA/Design/aida_tdr.pdf