Front end electronics and system design for the NUSTAR experiments at the FAIR facility

Presented by Ian Lazarus on behalf of NUSTAR collaboration

FEE 2006 Workshop

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Overview

- What are FAIR and NUSTAR?
- FEE challenges in NUSTAR
- FEE design principles for NUSTAR
- Example- part of the DESPEC experiment

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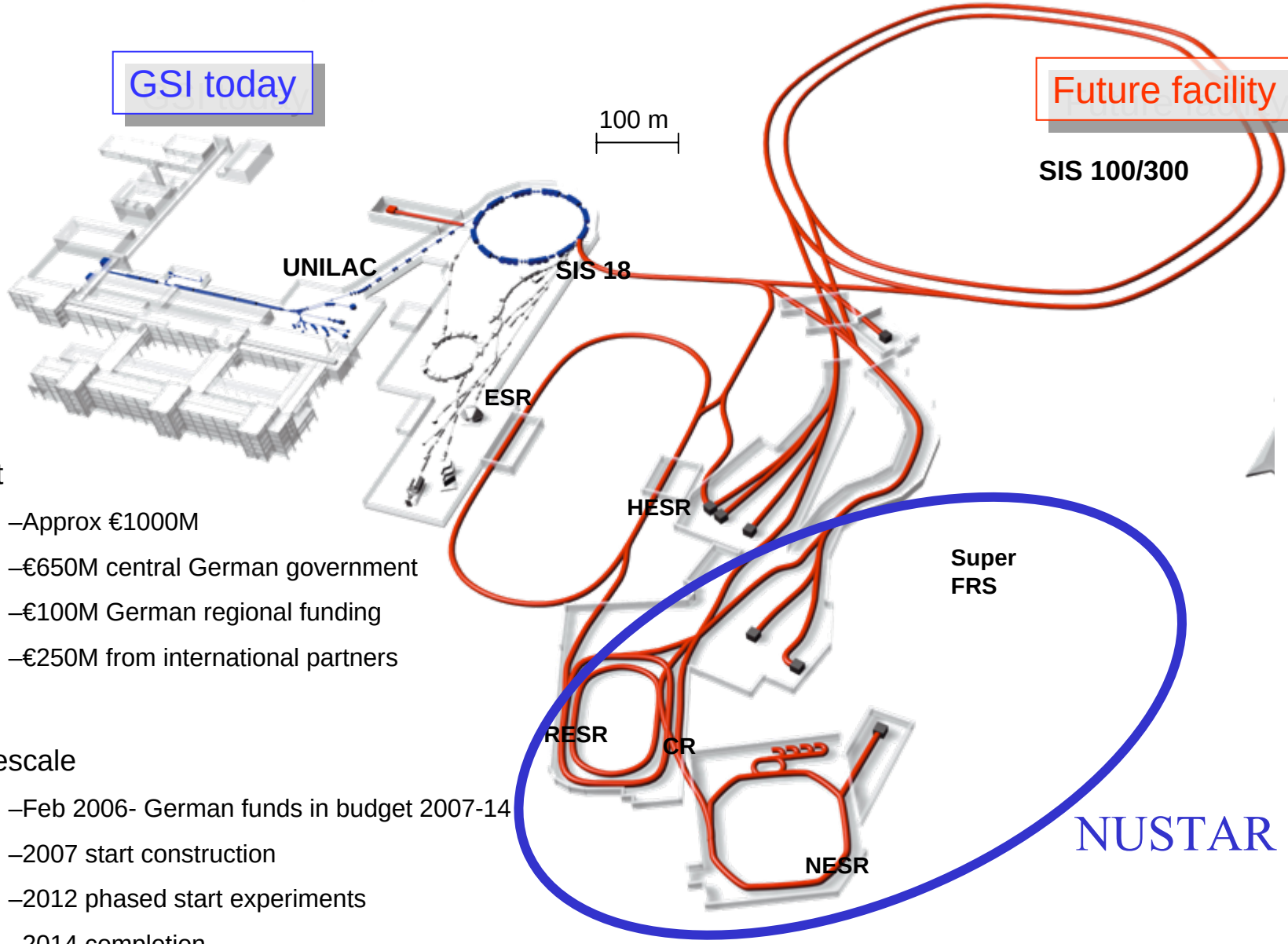
FAIR - Facility for Antiproton and Ion Research



- Cost
  - –Approx €1000M
  - –€650M central German government
  - –€100M German regional funding
  - –€250M from international partners
- Timescale
  - –Feb 2006- German funds in budget 2007-14
  - –2007 start construction
  - –2012 phased start experiments
  - –2014 completion

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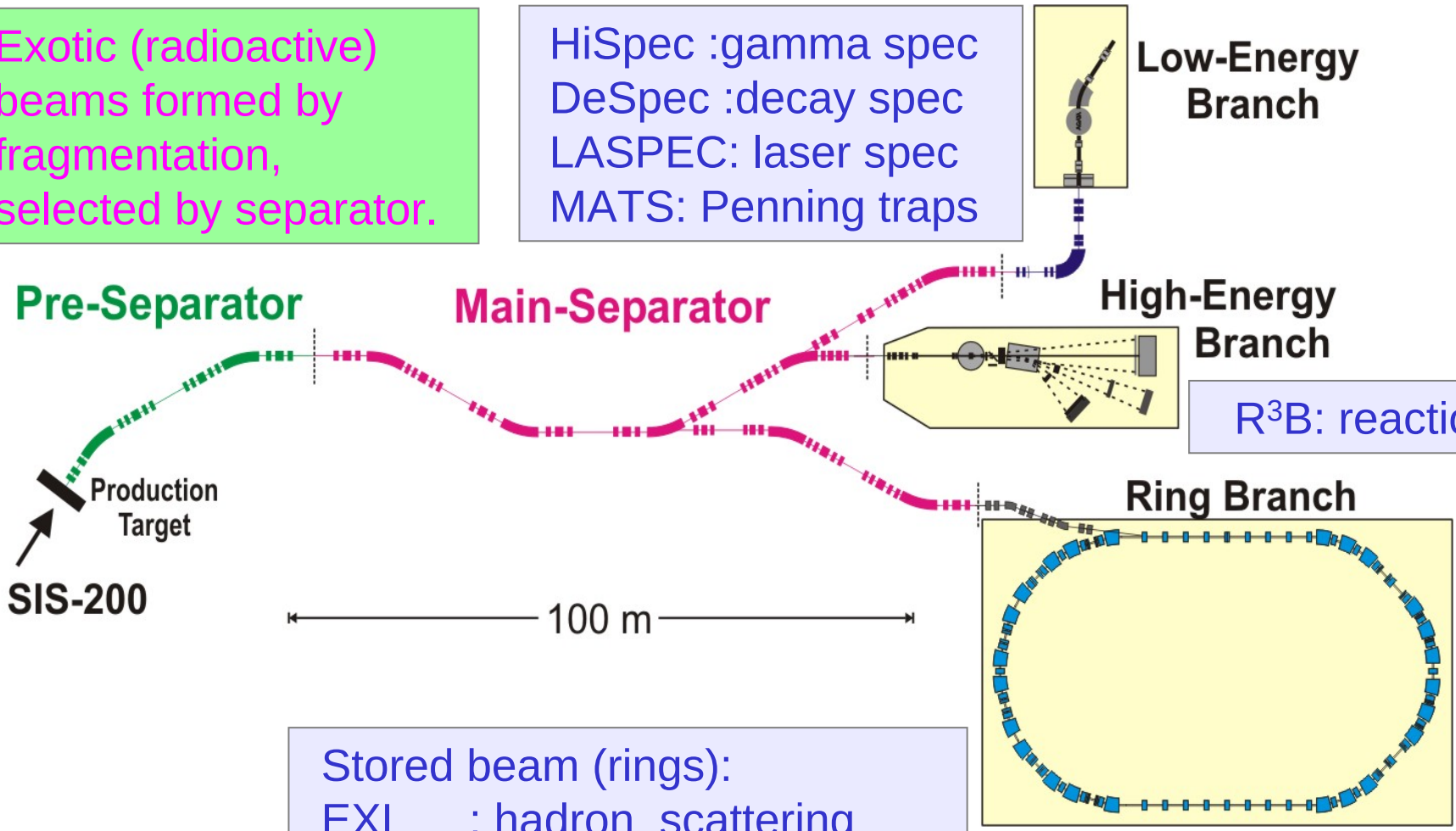
The NUSTAR facility (NUclear STructure Astrophysics and Reactions)

Exotic (radioactive) beams formed by fragmentation, selected by separator.

HiSpec :gamma spec
DeSpec :decay spec
LASPEC: laser spec
MATS: Penning traps



R^3B: reactions

Stored beam (rings):
EXL : hadron scattering
ELISe : electron scattering
AIC : antiproton scattering

NUSTAR Low energy branch

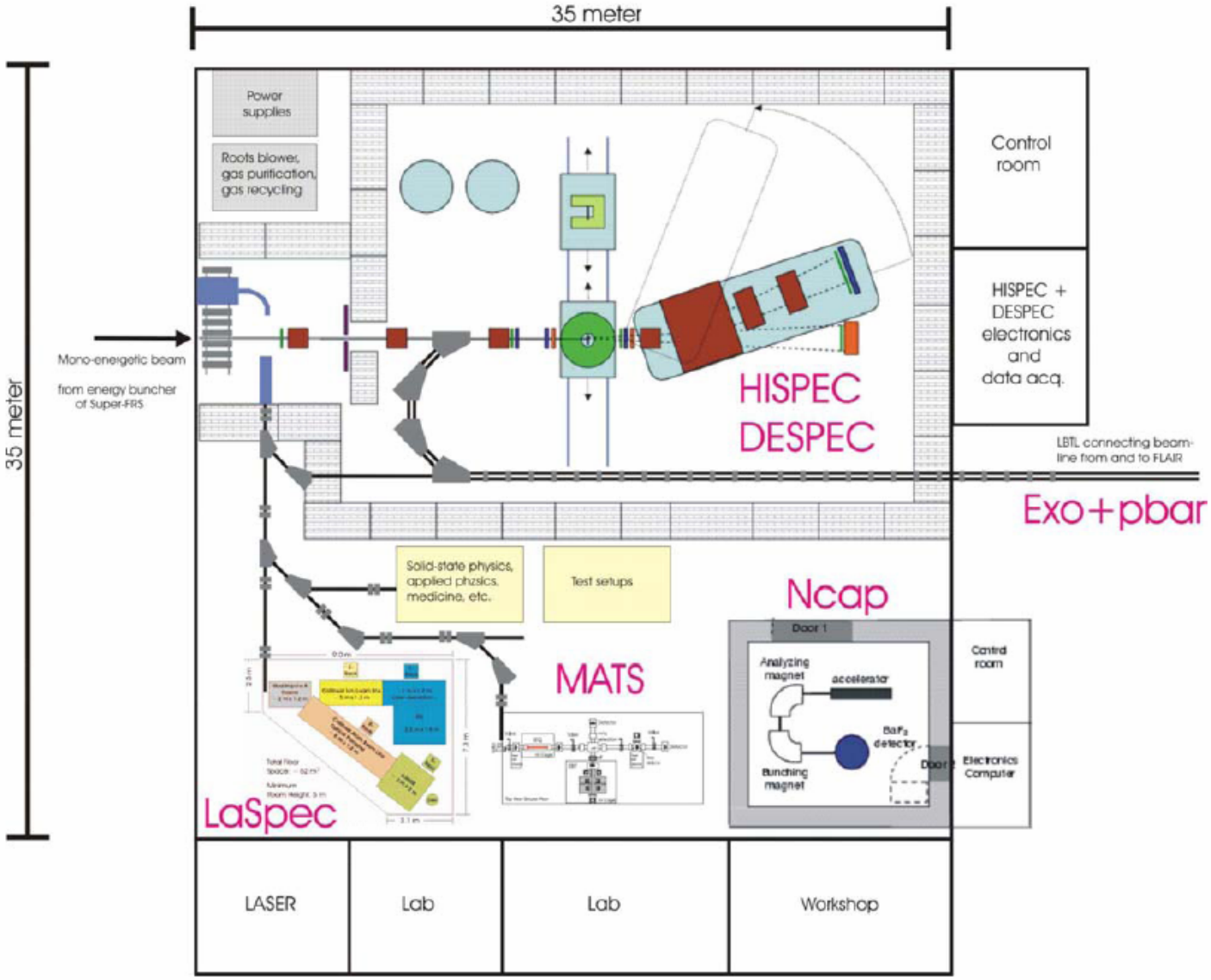
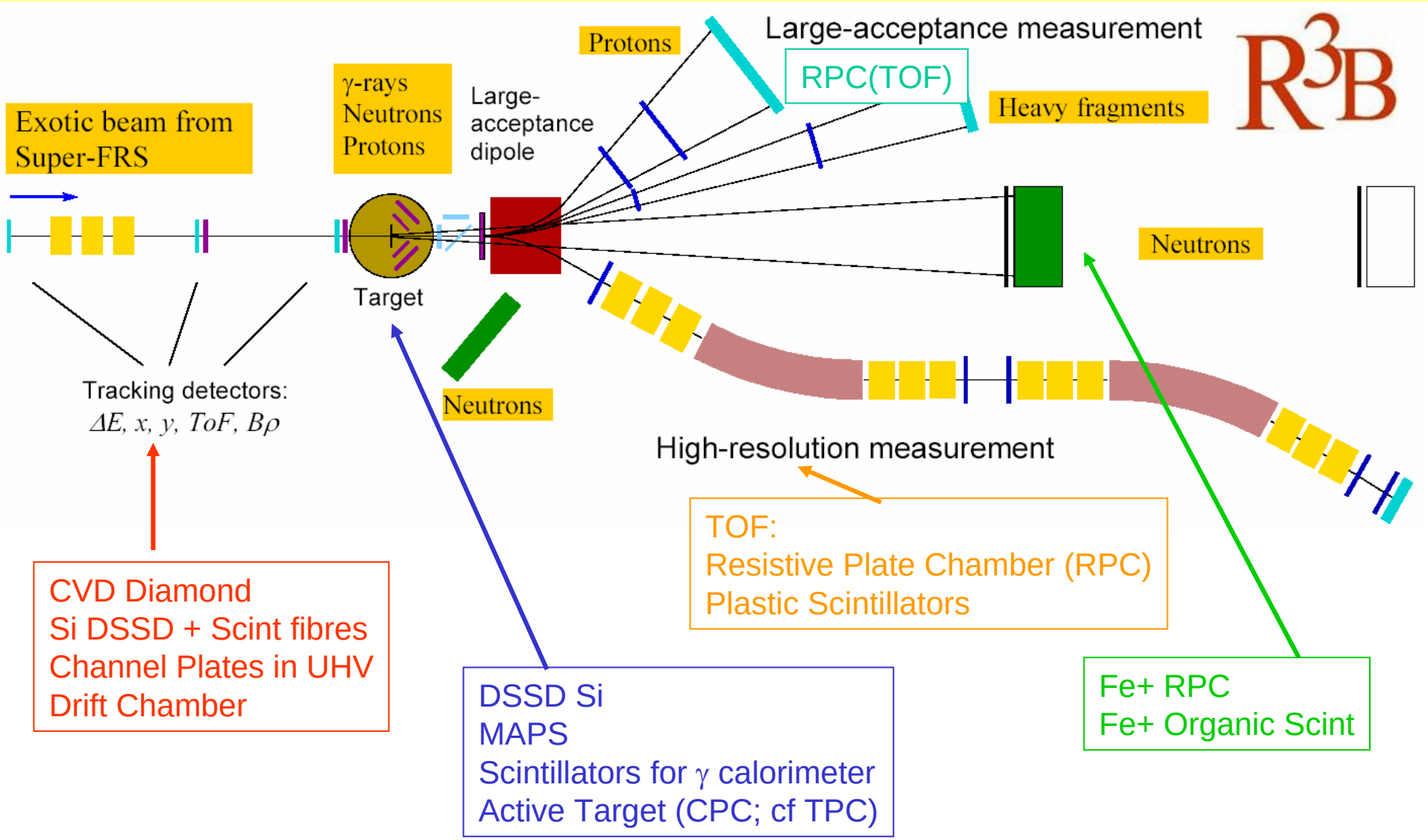


Fig. 1 Overview of the experimental area of the Low-Energy Branch

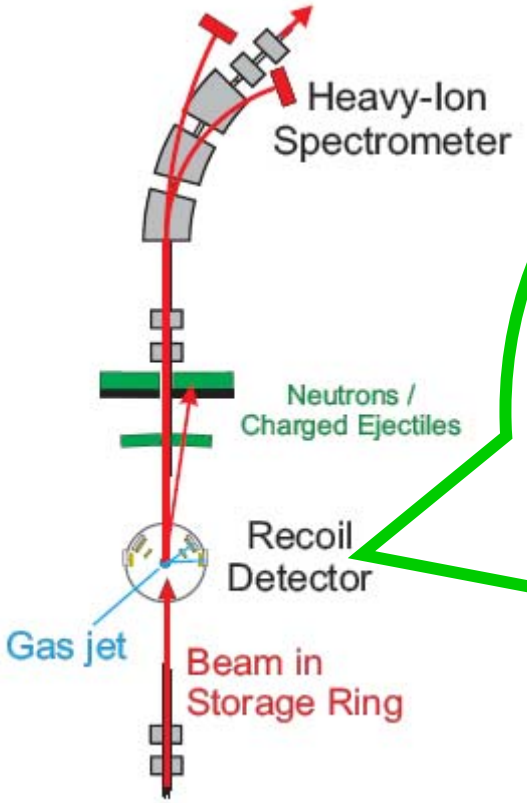
The high-energy branch of the Super-FRS:

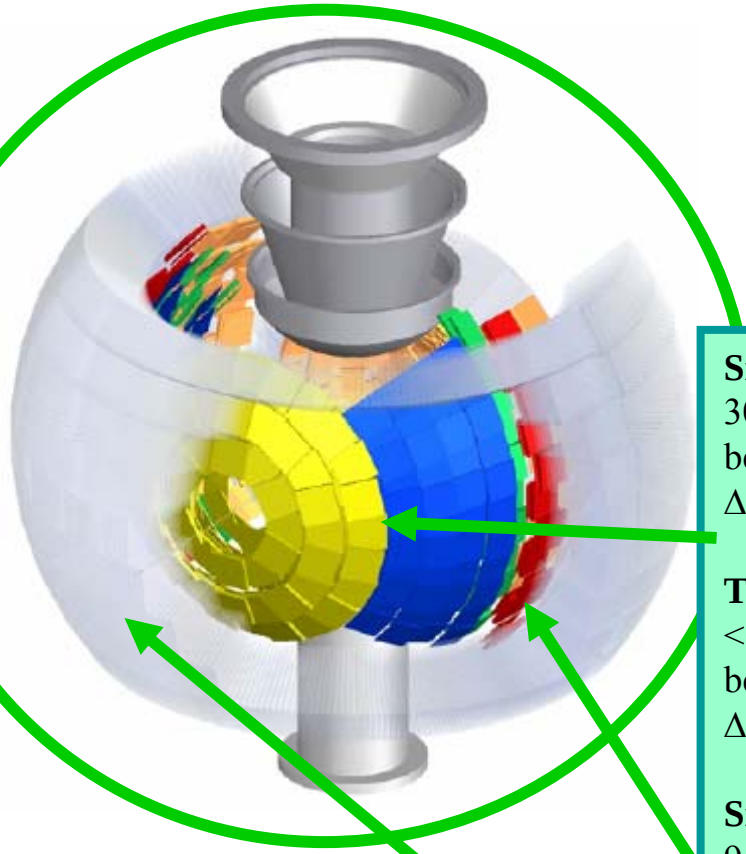
A universal setup for kinematical complete measurements of

Reactions with Relativistic Radioactive Beams



EXL Exotic Nuclei Studied in Light-Ion Induced Reactions at NESR





Si DSSD ⇨ **ΔE, x, y**
300 µm thick, spatial resolution better than 500 µm in x and y, ΔE = 30 keV (FWHM)

Thin Si DSSD ⇨ **tracking**
<100 µm thick, spatial resolution better than 100 µm in x and y, ΔE = 30 keV (FWHM)

Si(Li) ⇨ **E**
9 mm thick, large area
100 x 100 mm^2,
ΔE = 50 keV (FWHM)

CsI/LaBr3 crystals ⇨ **E, γ**
High efficiency, high resolution, 20 cm thick

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FEE Challenges in NUSTAR

- Some experiments present no real FEE challenge
  - e.g. LaSpec (just needs some NIM + PC)

- Others want the impossible
  - e.g. >500k Si channels with preamp, shaper, timing, digital PSD all in UHV (10^{-11} mbar)
    - Power! Vacuum feed-throughs!!
    - (Currently negotiating with physicists.)

FEE Challenges in NUSTAR

Some places where ASIC solutions are under consideration in NUSTAR:

- EXL- high Si channel count in UHV. Challenges are
  - very low power per channel (target <1mW/channel, aim at 200uW)
  - limited space as well as channel count forces use of ASICs
  - limiting number of feedthroughs (implies significant multiplexing)
  - Variety of detector types, pitches (C_{in}) (different DSSD strips, also SiLi, & PD)
  - Vacuum (10^{-11} to 10^{-7}mbar) compatibility (130C baking, no contaminants released)
  - if E, ToF measurements not good enough for p-α discrimination then need PSD too
- Despec- decay spectroscopy
  - fast recovery from massive overload.
  - space and position constraints
- R3B Active Target (ACTAR). Charge Projection Chamber (c.f. TPC).
  - Low noise preamps plus fast digitisers (probably external) to study pulse shape and position.
- Gamma-ray calorimeter (CsI or LaBr3) with about 13k channels.
  - Potential use here for ASICs due to channel count (preamp+shaper+time)

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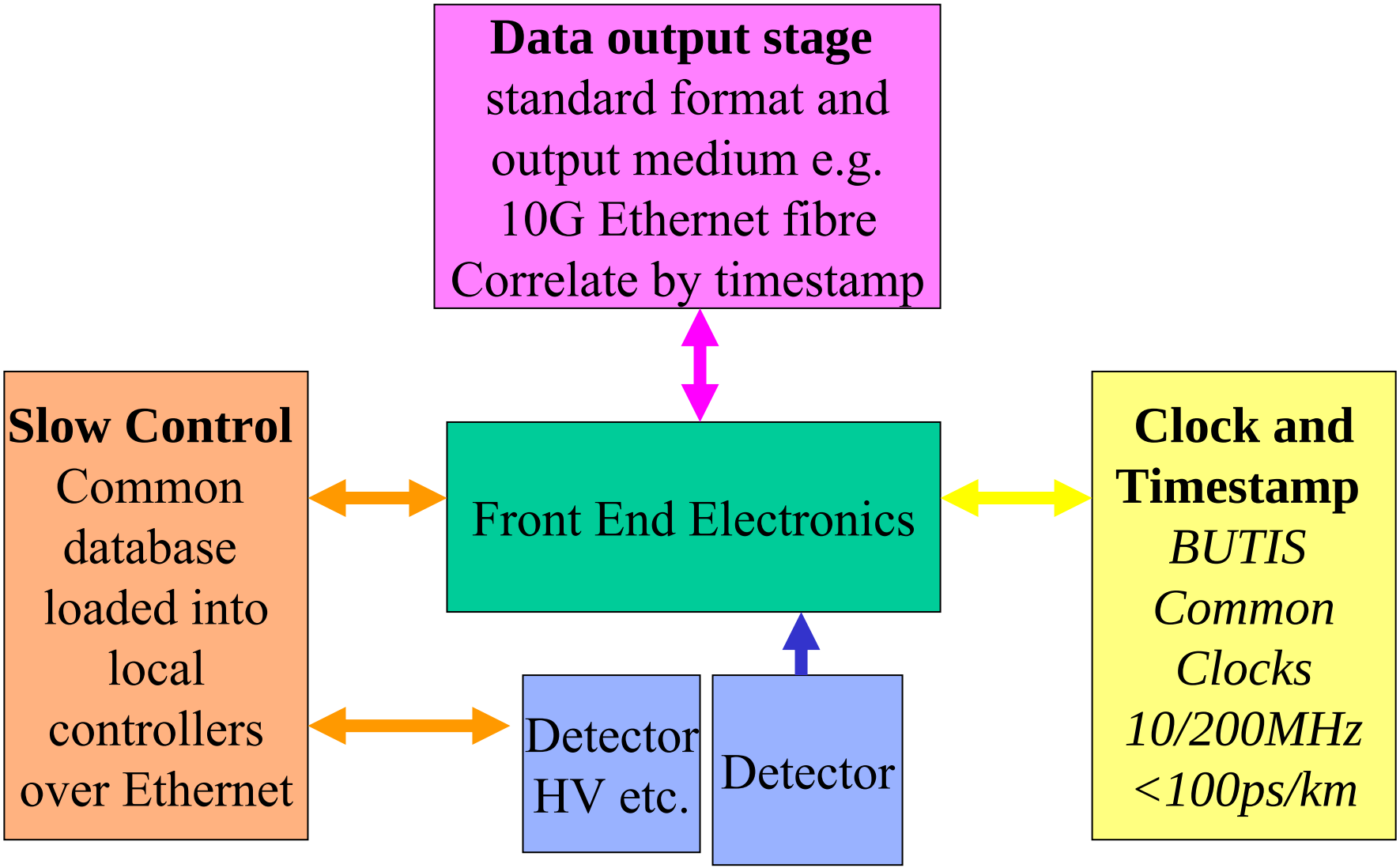
NUSTAR- Defining 3 common interfaces or docking stations



DAQ- key concepts

- DAQ- :
  - Software Triggering (timestamp based)
  - High channel counts
  - High Bandwidth Data Readout- (esp. front end and tracking detectors)
  - Use of commercial high bandwidth networks
  - Increasingly large PC farms

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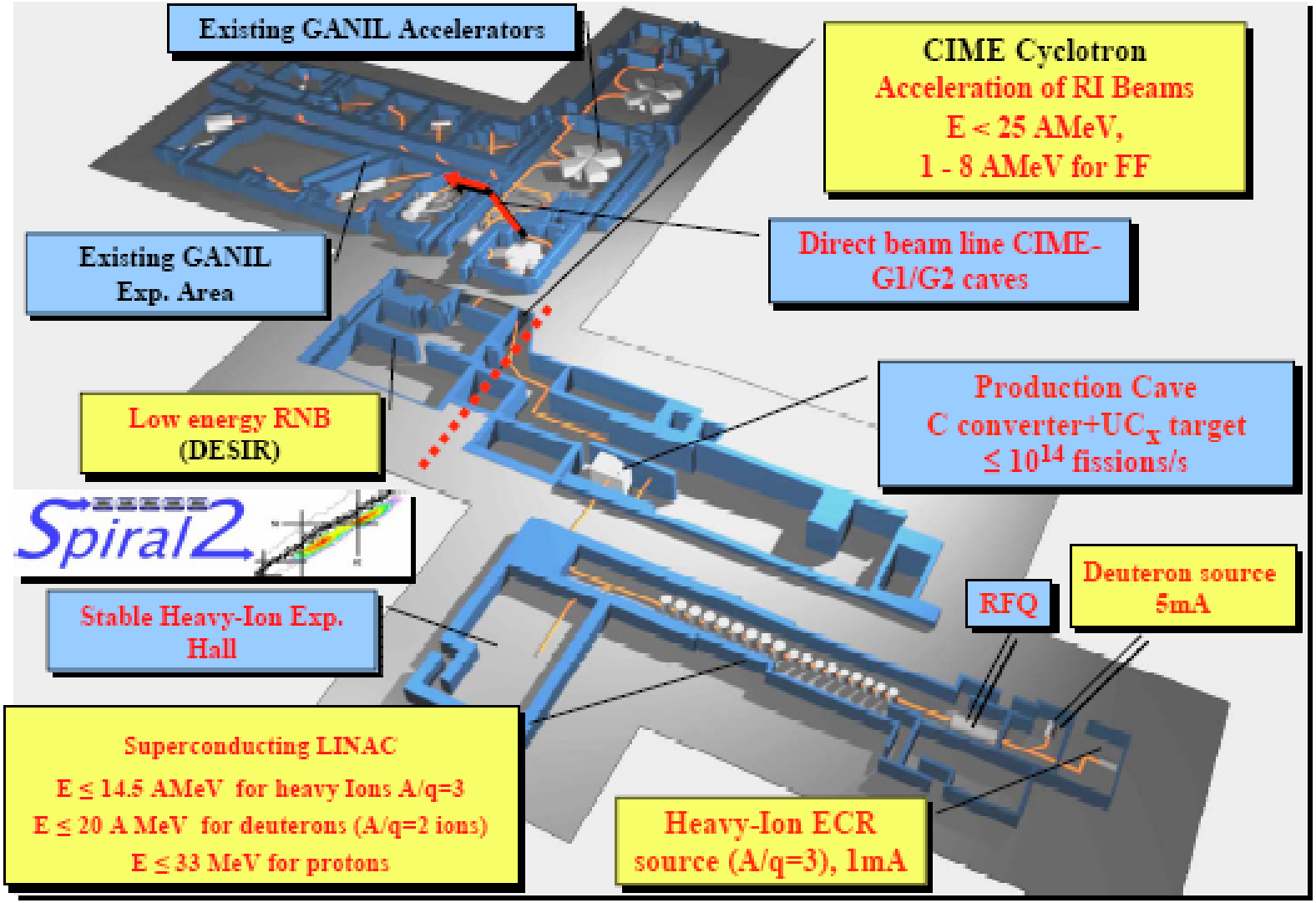
SPIRAL2 at GANIL



ISOL beams: high optical purity (few mm of diameter), $\Delta E/E$ few 10^{-4}, high intensity

Collaboration between FAIR & SPIRAL2

- NUSTAR and SPIRAL2 meetings 3x p.a. to discuss FEE, ASICs and DAQ (first meeting Jan 2006, next June 2006).
- Looking for synergy in FEE and DAQ
- Lolly Pollacco and Ian Lazarus appointed to co-ordinate ASICs (try to avoid duplication)

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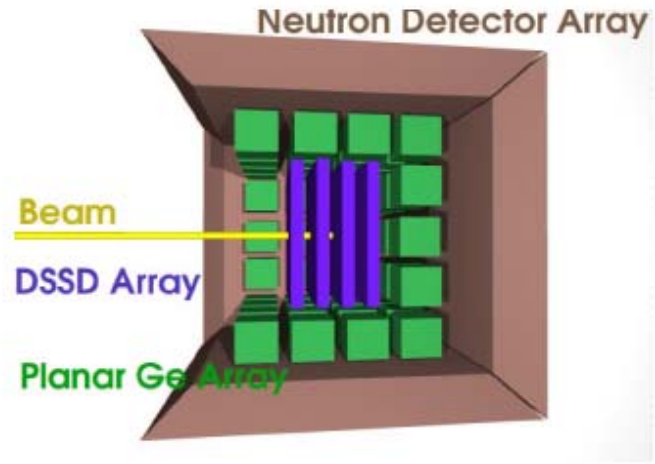
AIDA for DESPEC- the concept

Advanced Implantation Detector Array (AIDA)



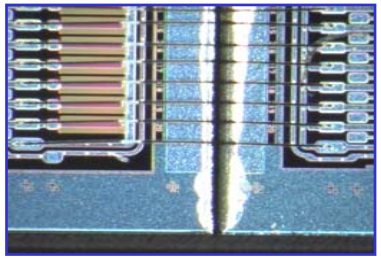
- Super FRS Low Energy Branch (LEB)
- Exotic nuclei – energies ~50-150MeV/u
- Implanted into multi-plane DSSD array
- Implant - decay correlations
- Multi-GeV DSSD implantation events
- Observe subsequent p, 2p, α, β, γ, βp, βn … decays
- Measure half lives, branching ratios, decay energies …
- DSSD segmentation ensures average time between implants for given x,y quasi-pixel >> decay half life to be observed.
- Implies quasi-pixel dimensions ~ 0.5mm x 0.5mm

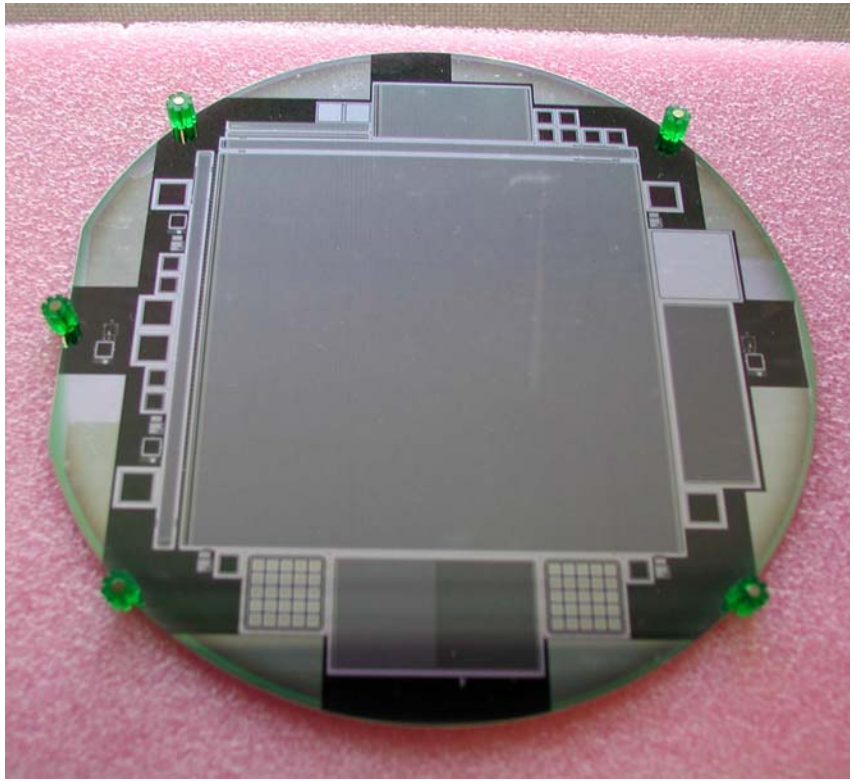
AIDA for DESPEC- the detector

DSSD

Technology well established
(e.g. GLAST LAT tracker)

- 6” wafer technology
  10cm x 10cm area
- 1mm wafer thickness
- Integrated components
  a.c. coupling
  polysilicon bias resistors
  … important for ASICs
- Series strip bonding

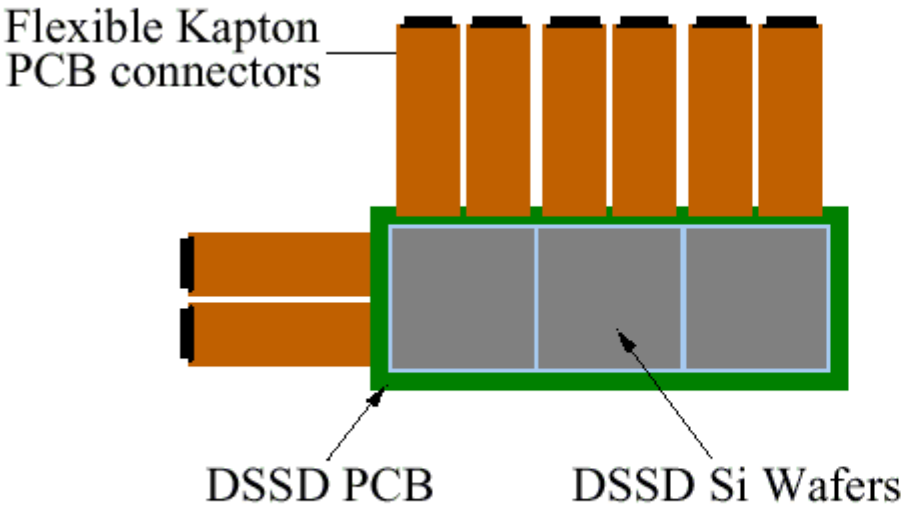


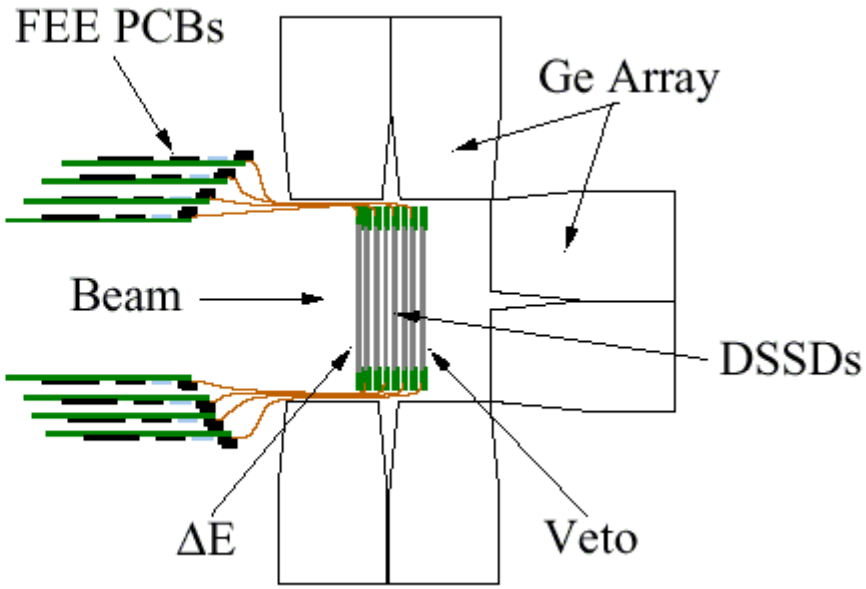


8.95 cm square Hamamatsu-Photonics SSD before cutting from the 6-inch wafer. The thickness is 400 microns, and the strip pitch is 228 microns.

AIDA for DESPEC

General Arrangement





AIDA for DESPEC- Instrumentation

Instrumentation

Why use of Application Specific Integrated Circuit (ASIC) technology?

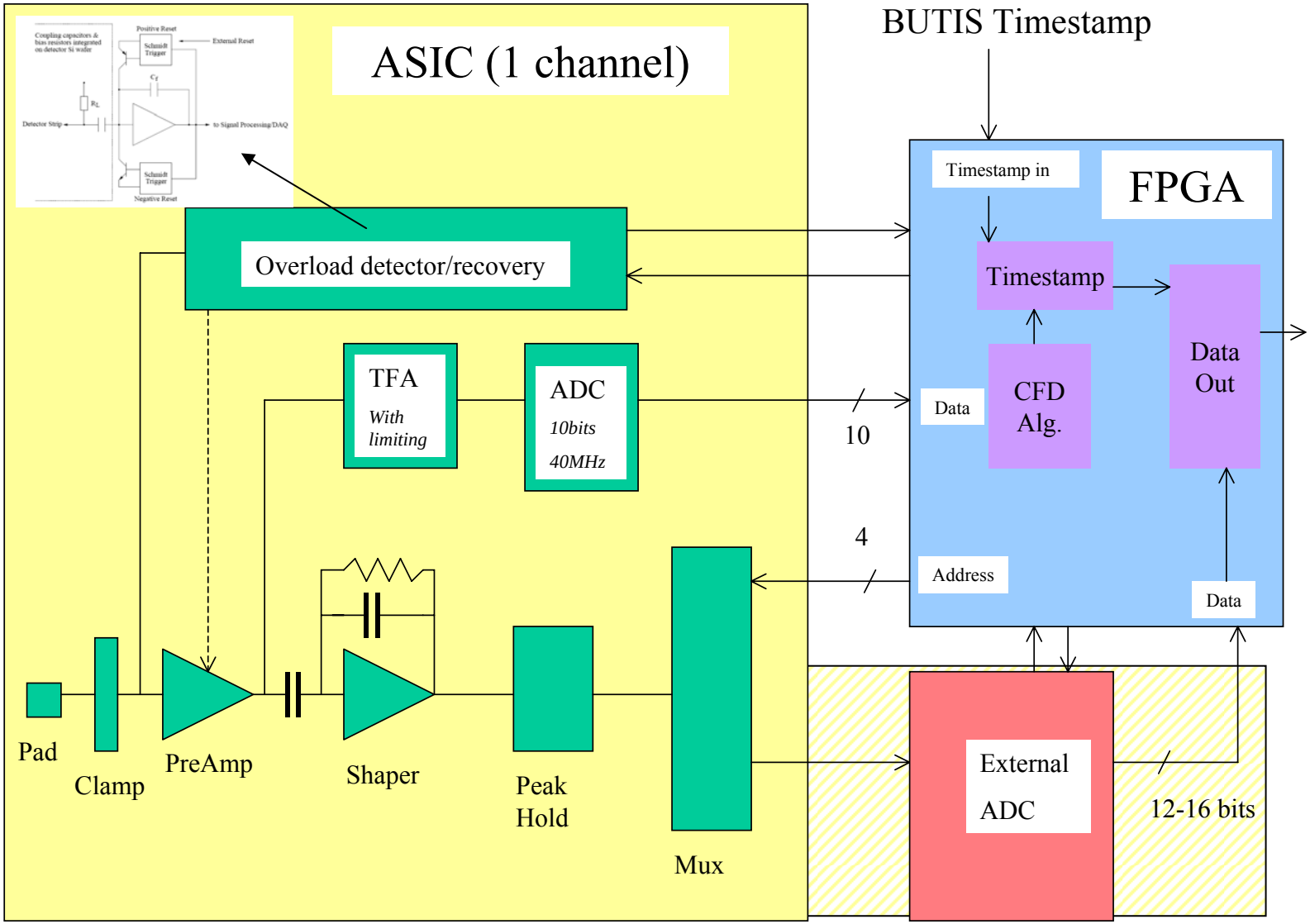
- Large number of channels required (8 x (128+(3x128))= 4096)
- Limited available space
- Cost

Outline ASIC Specification

- Selectable gain: low 20GeV FSR
  high 20MeV FSR
- Noise σ ~ 5keV rms.
- Selectable threshold: minimum ~ 25keV @ high gain (assume 5σ)
- Integral and differential non-linearity
- Autonomous overload recovery ~μs
- Signal processing time <10μs (decay-decay correlations)
- Receive timestamp data
- Timing trigger for coincidences with other detector systems

DSSD segmentation reduces input loading of preamplifier and enables excellent noise performance.

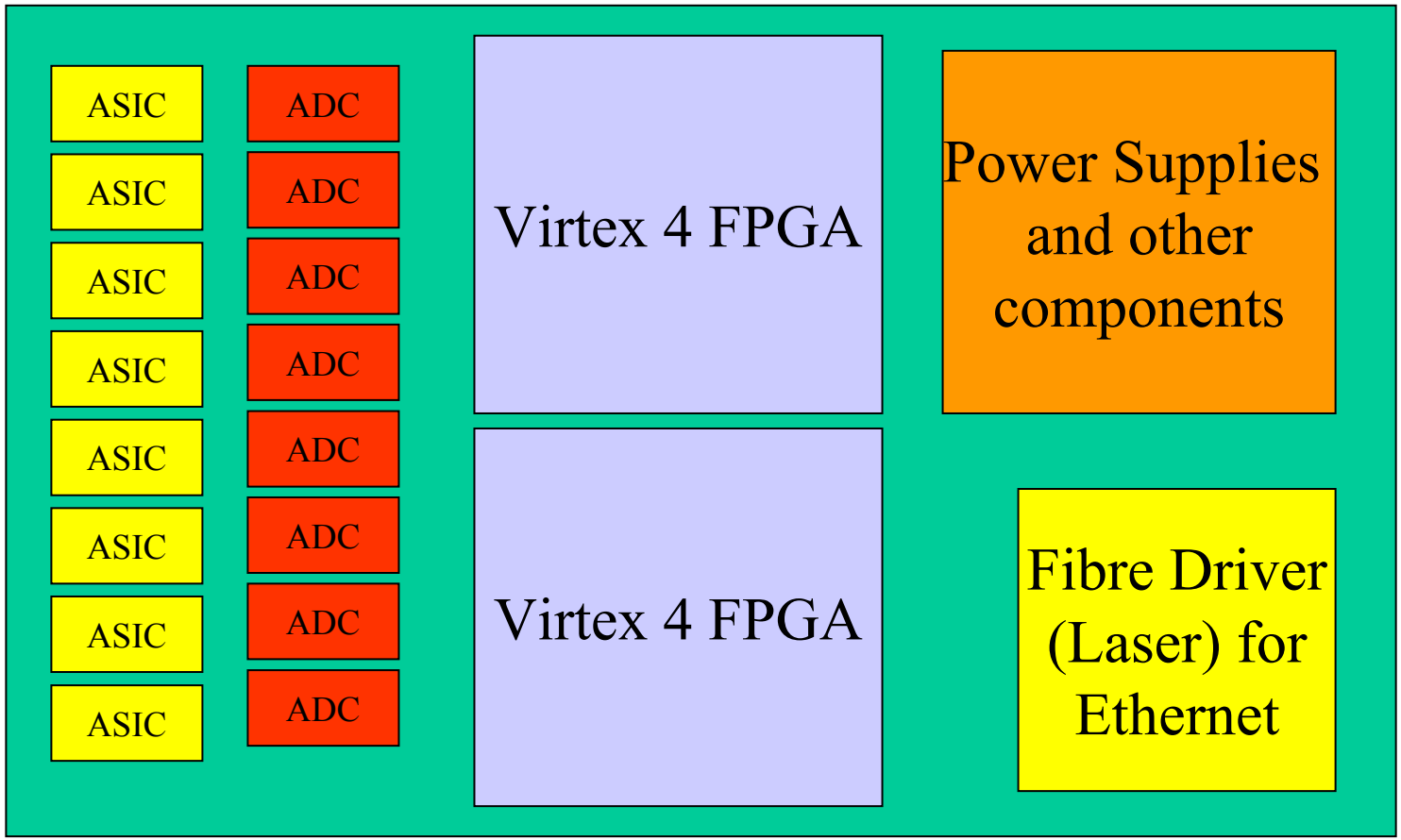
1 of the 16 channels in the DESPEC Implantation Detector ASIC (shown with external FPGA and ADC)



128 Channel FEE Card for DESPEC

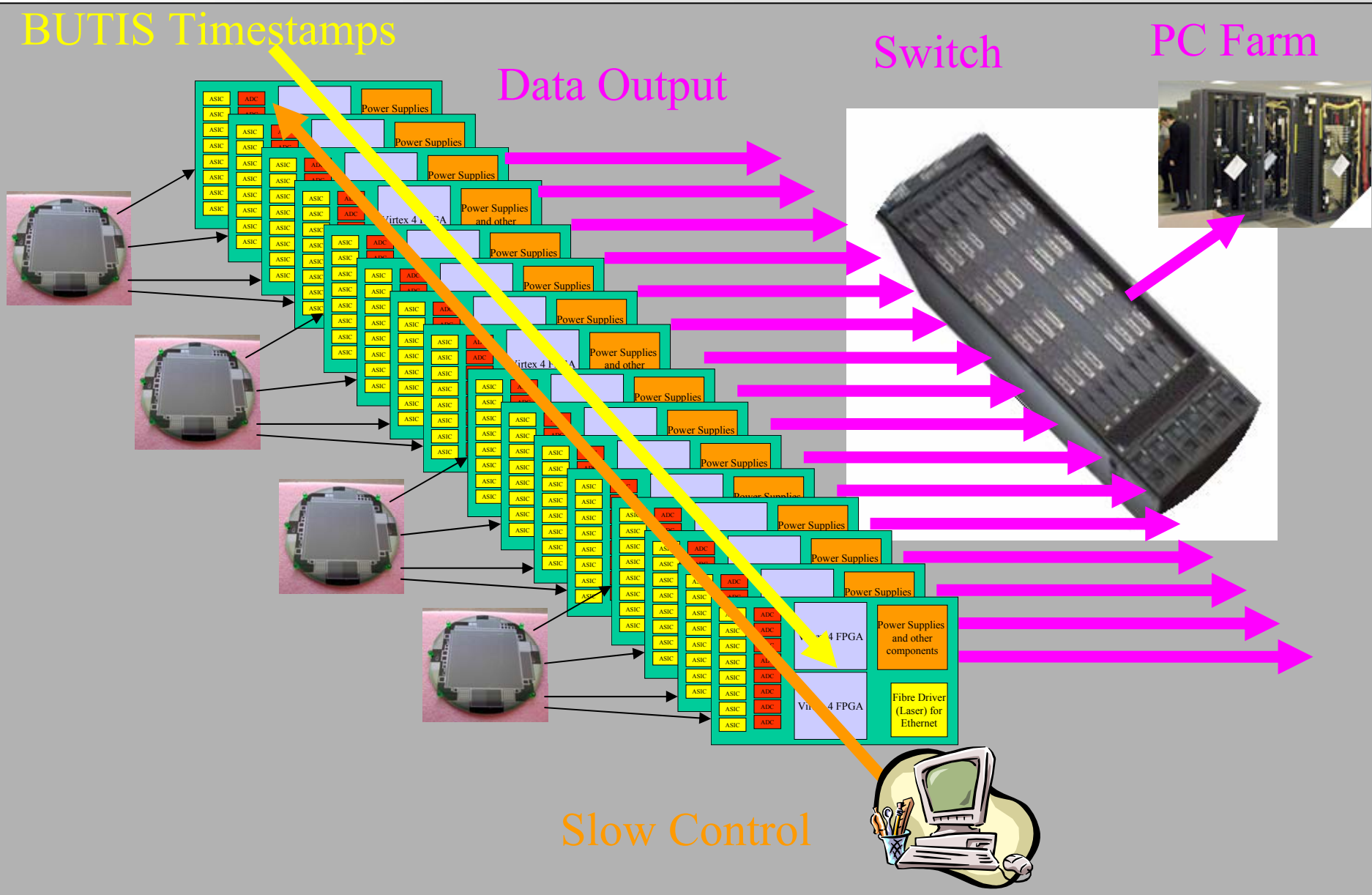
16 ch ASIC *16 bit ADC*

128 detector signals in; 1 data fibre out



Estimated size: 80x220mm,
Estimated power 25W per 128ch (800W total)

Diagram of half of AIDA system



Summary

- FAIR and NUSTAR present exciting physics opportunities and interesting technical challenges.
- There is a wide variety of FEE requirements in NUSTAR ranging from minimal to very difficult.
- In order to make best use of limited resources (especially ASIC designers) we will coordinate to avoid duplication both internally and with SPIRAL2. Forums have been set up to discuss the following:
  - FEE
  - ASICs
  - DAQ
- Funding has started so ideas are now beginning to be implemented- the real work starts now!

Acknowledgements

Presentation includes pictures from other people.

Thanks to:
•Tom Davinson (University of Edinburgh)
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•Haik Simon (GSI)

NUSTAR slow control and DAQ discussions included
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• Heinrich Wörtche (KVI)
• Lolly Pollacco (CEA Saclay)