CCLRC Technology

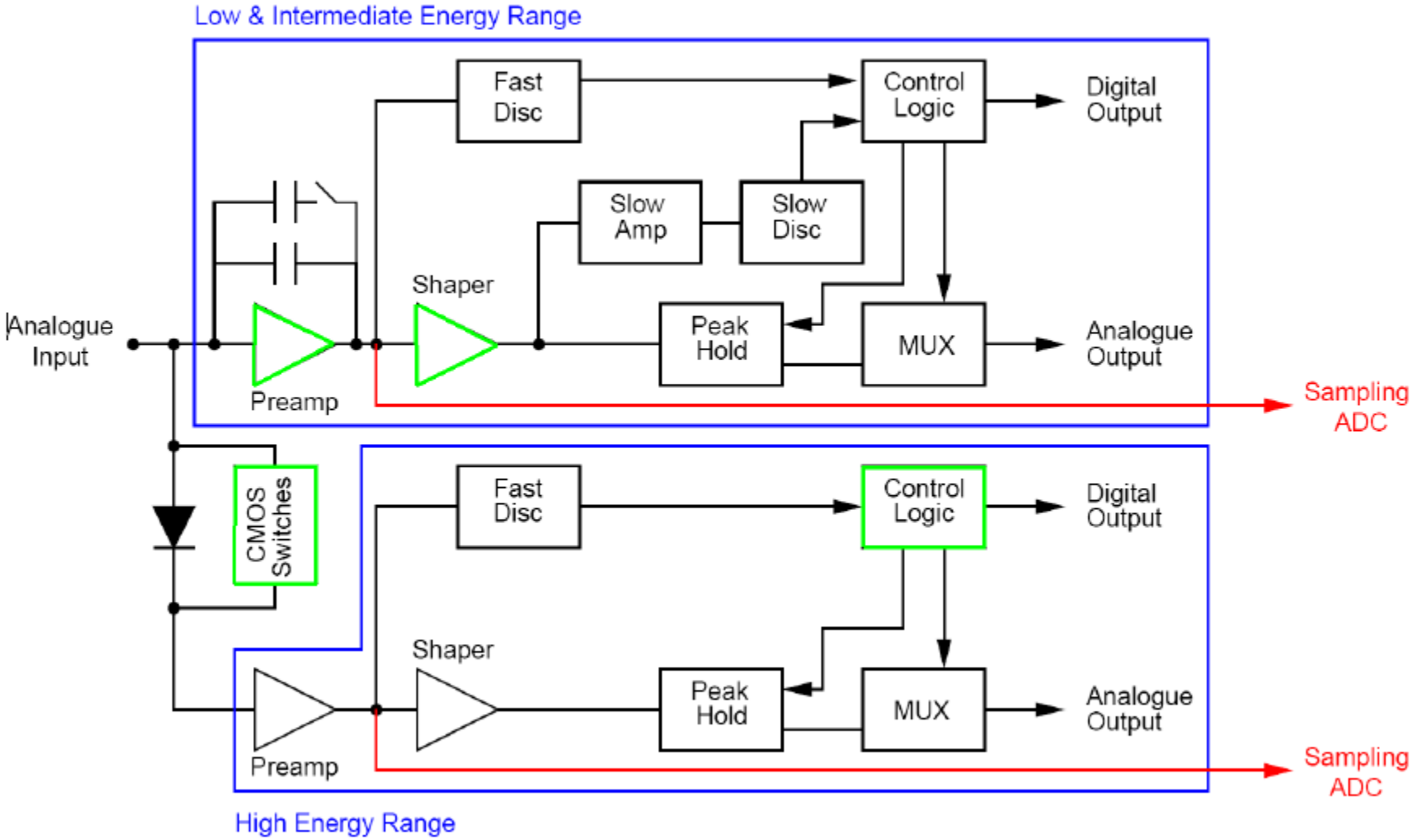
AIDA detailed design

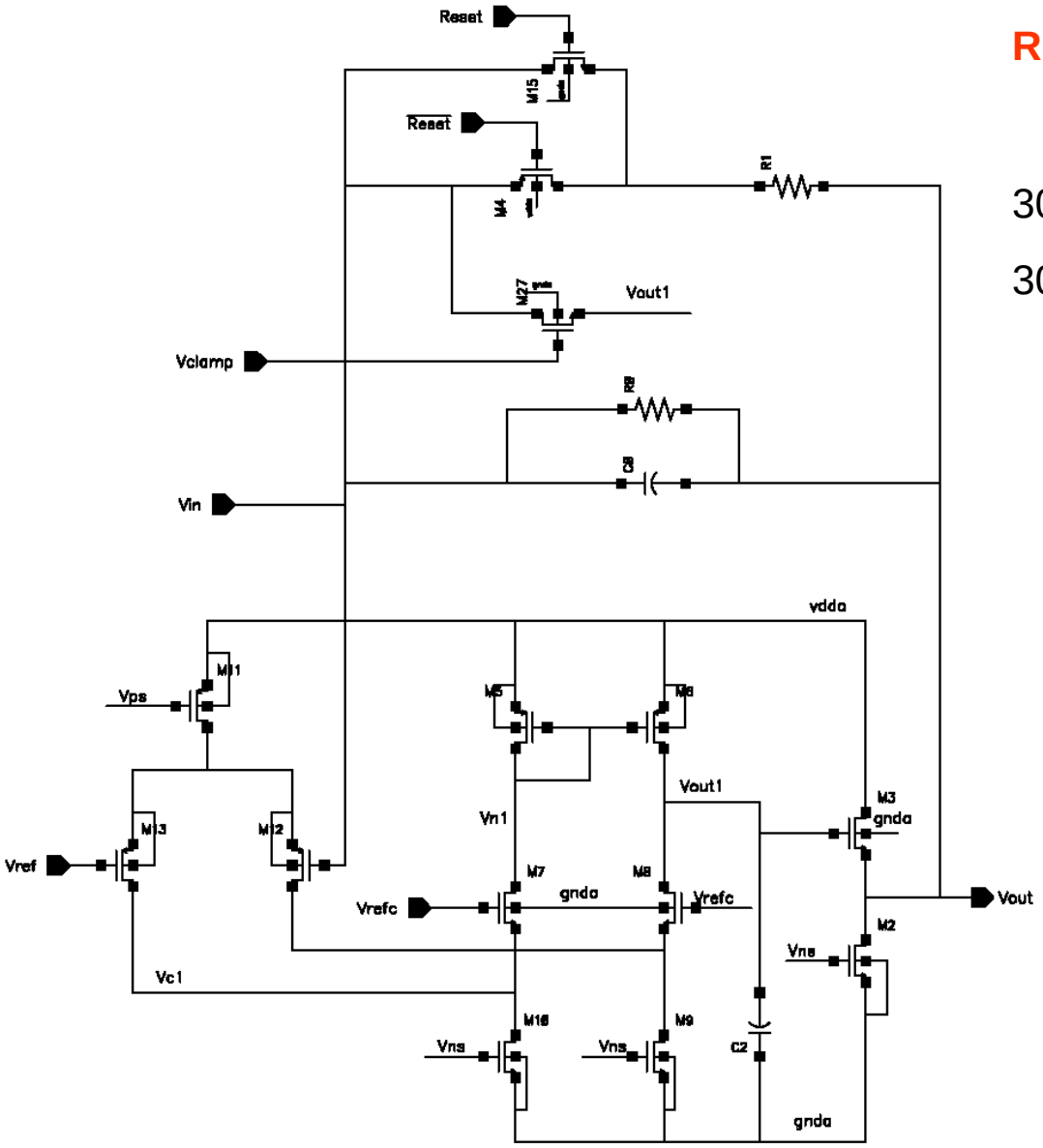
Amplifier feedback options

Steve Thomas

ASIC Design Group

20th February 2007


Low & Intermediate Energy Range
Fast Disc
Control Logic
Digital Output
Slow Amp
Slow Disc
Shaper
Analogue Input
Peak Hold
MUX
Analogue Output
Preamp
Sampling ADC
CMOS Switches
Fast Disc
Control Logic
Digital Output
Shaper
Peak Hold
MUX
Analogue Output
Preamp
Sampling ADC
High Energy Range

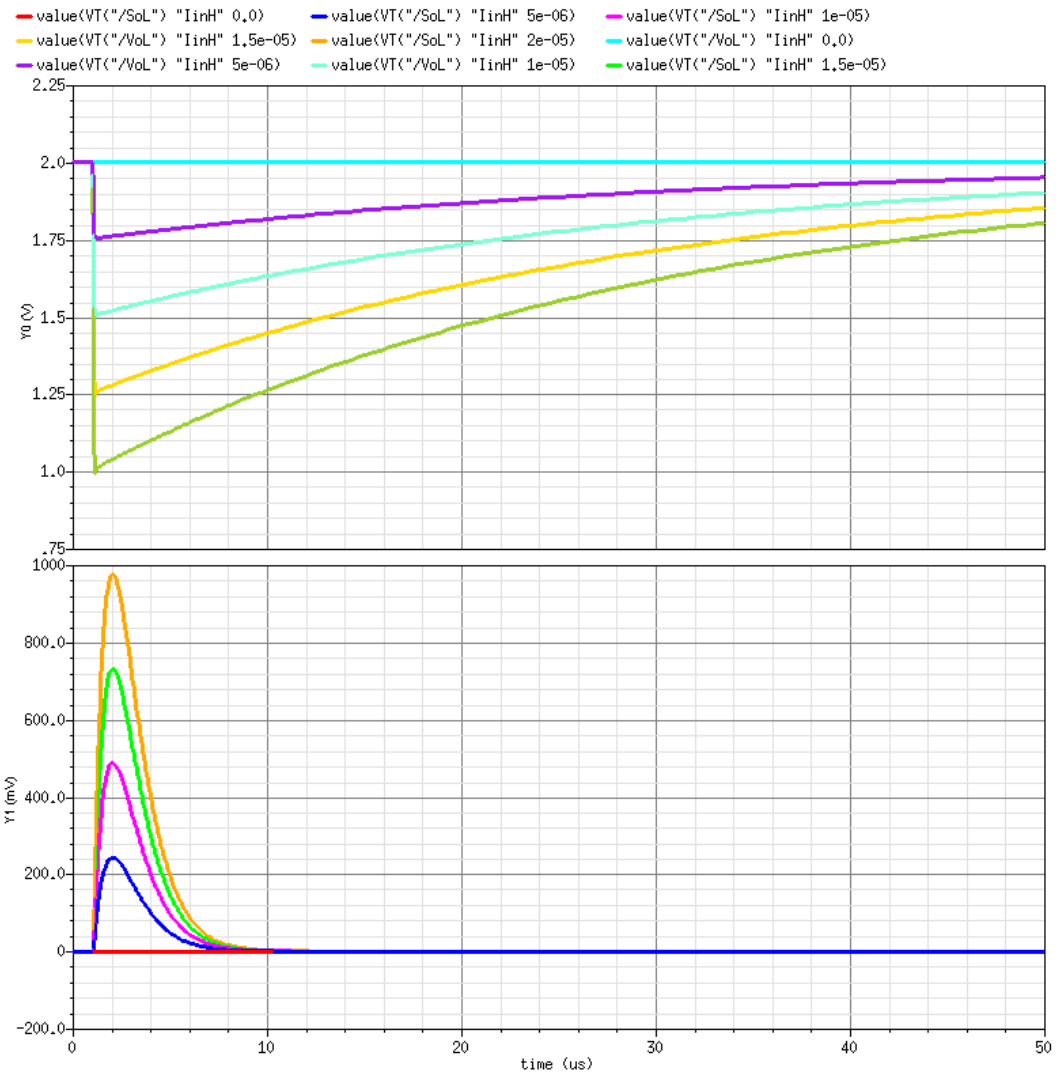


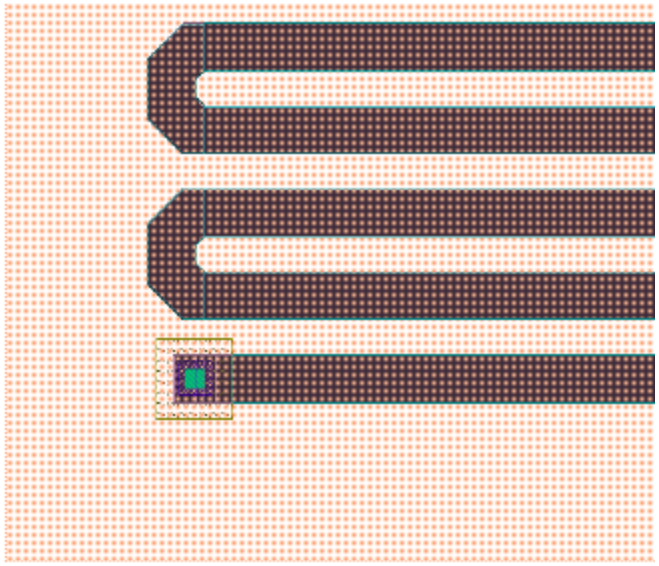
Resistive feedback - idealised model

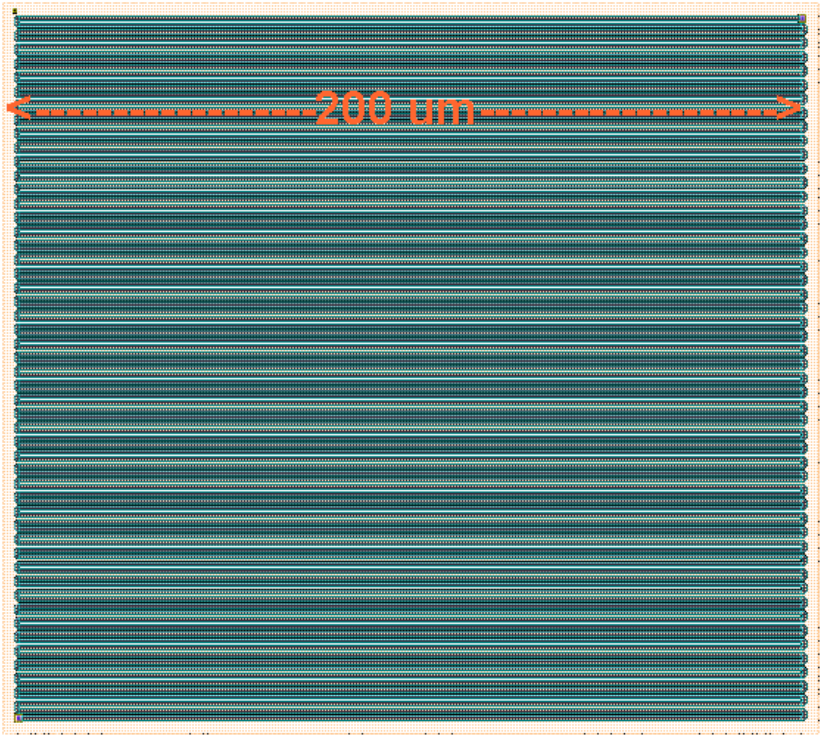
30MΩ, no parasitic capacitance

30μs time constant

30M resistor - no capacitance



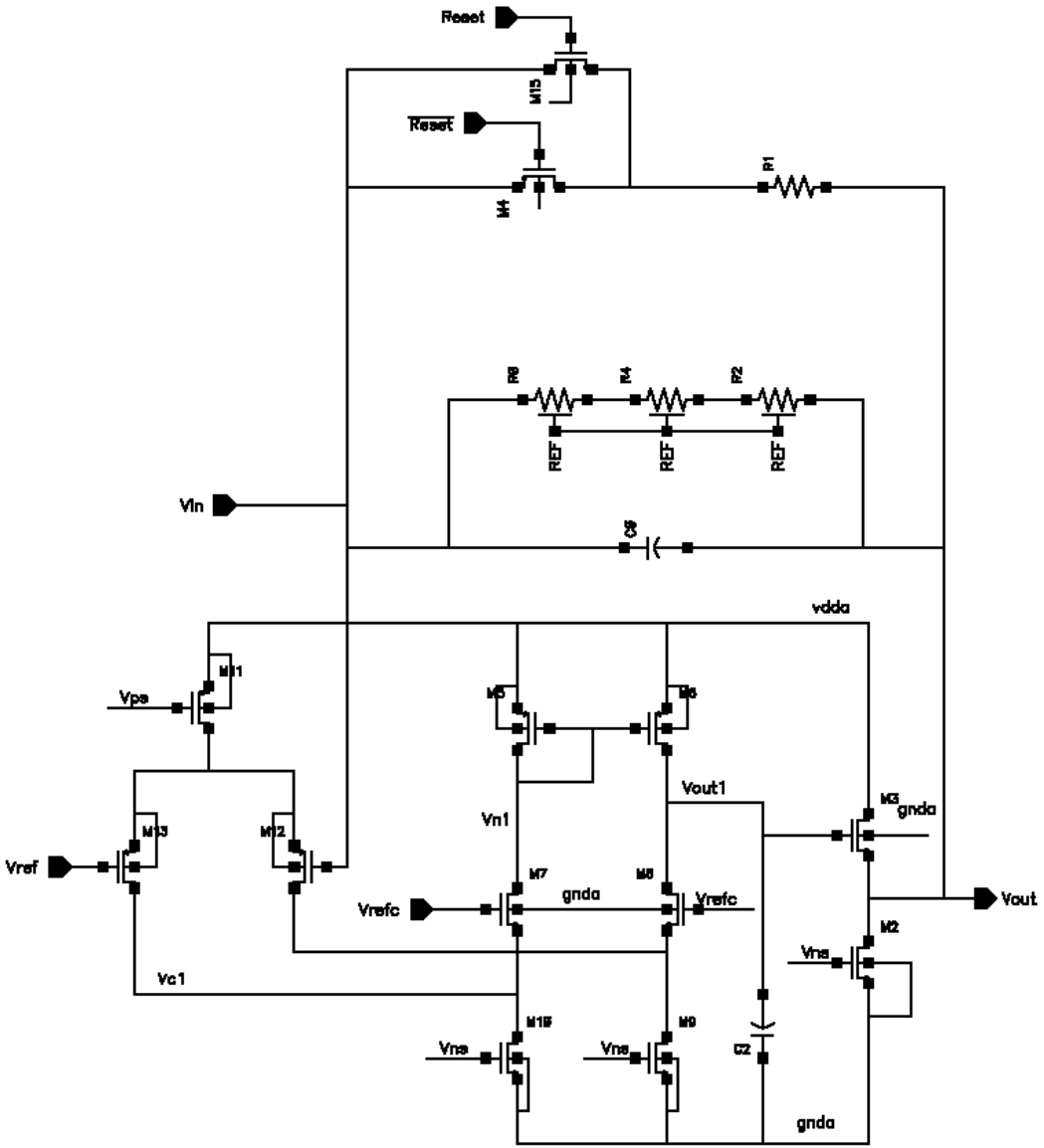




Feedback resistor

Poly2 : 1.2kΩ per square

~3pF parasitic to substrate

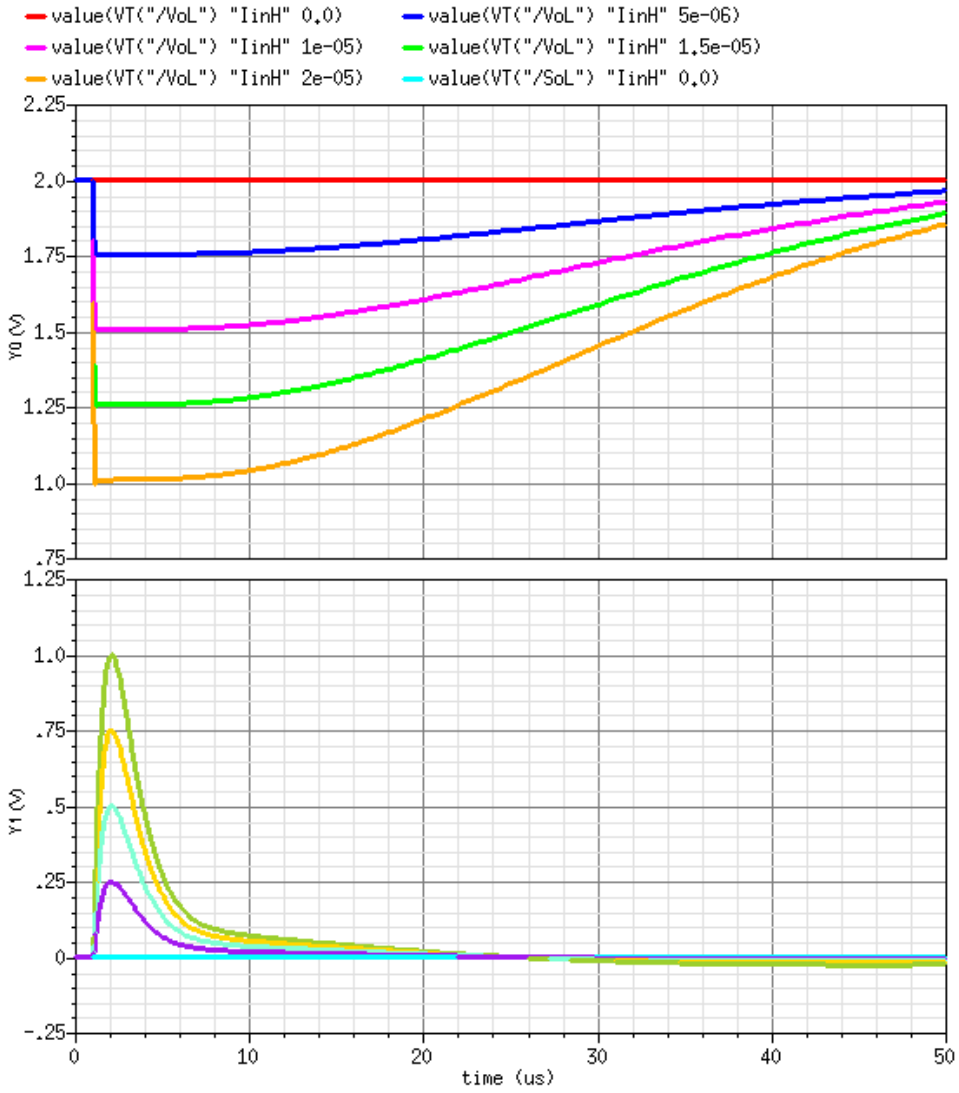


Resistive feedback

30MΩ, with capacitance

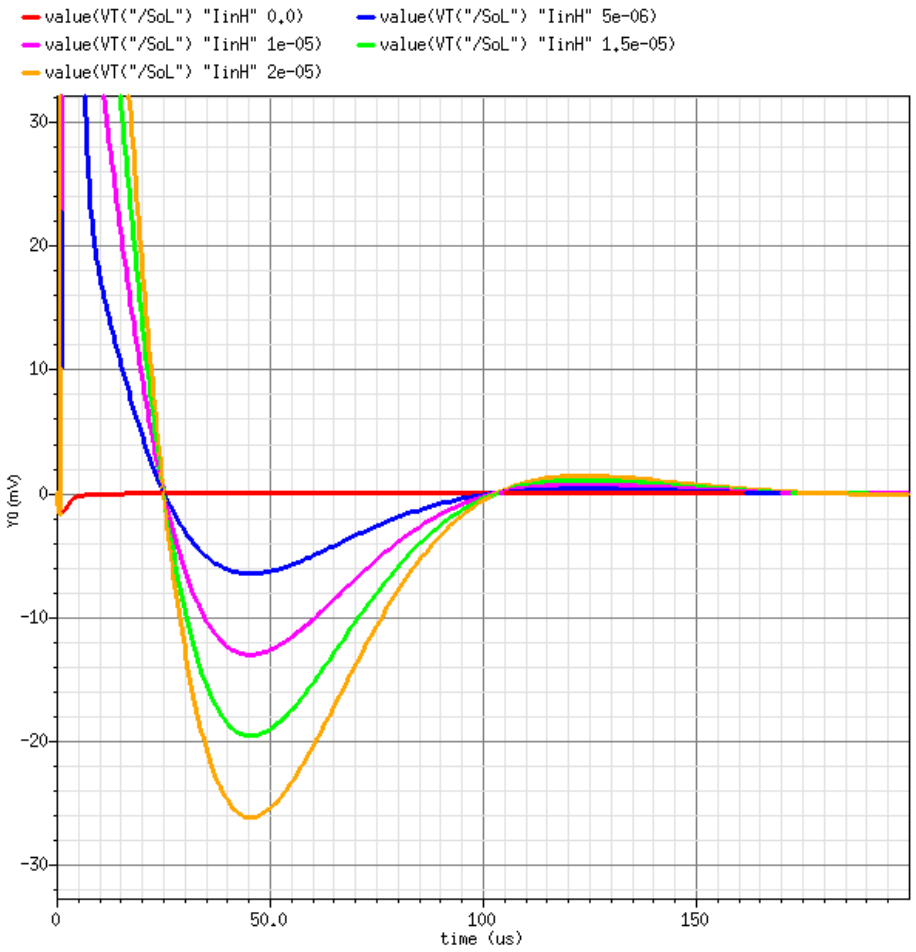
~1pF per 10MΩ segment

~10μs time constant

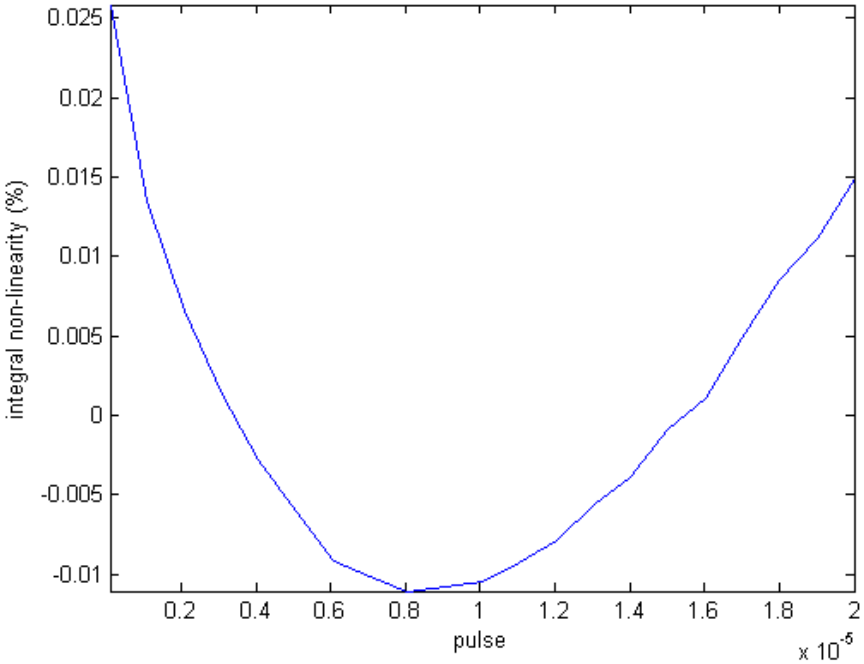


30M resistor - with capacitance

30M resistor - with capacitance

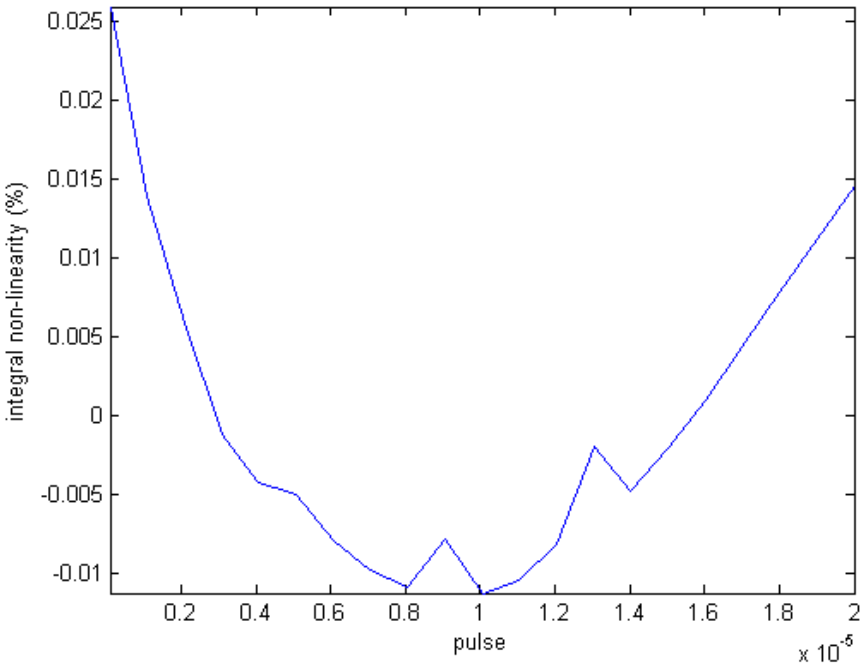


Pole-zero failure

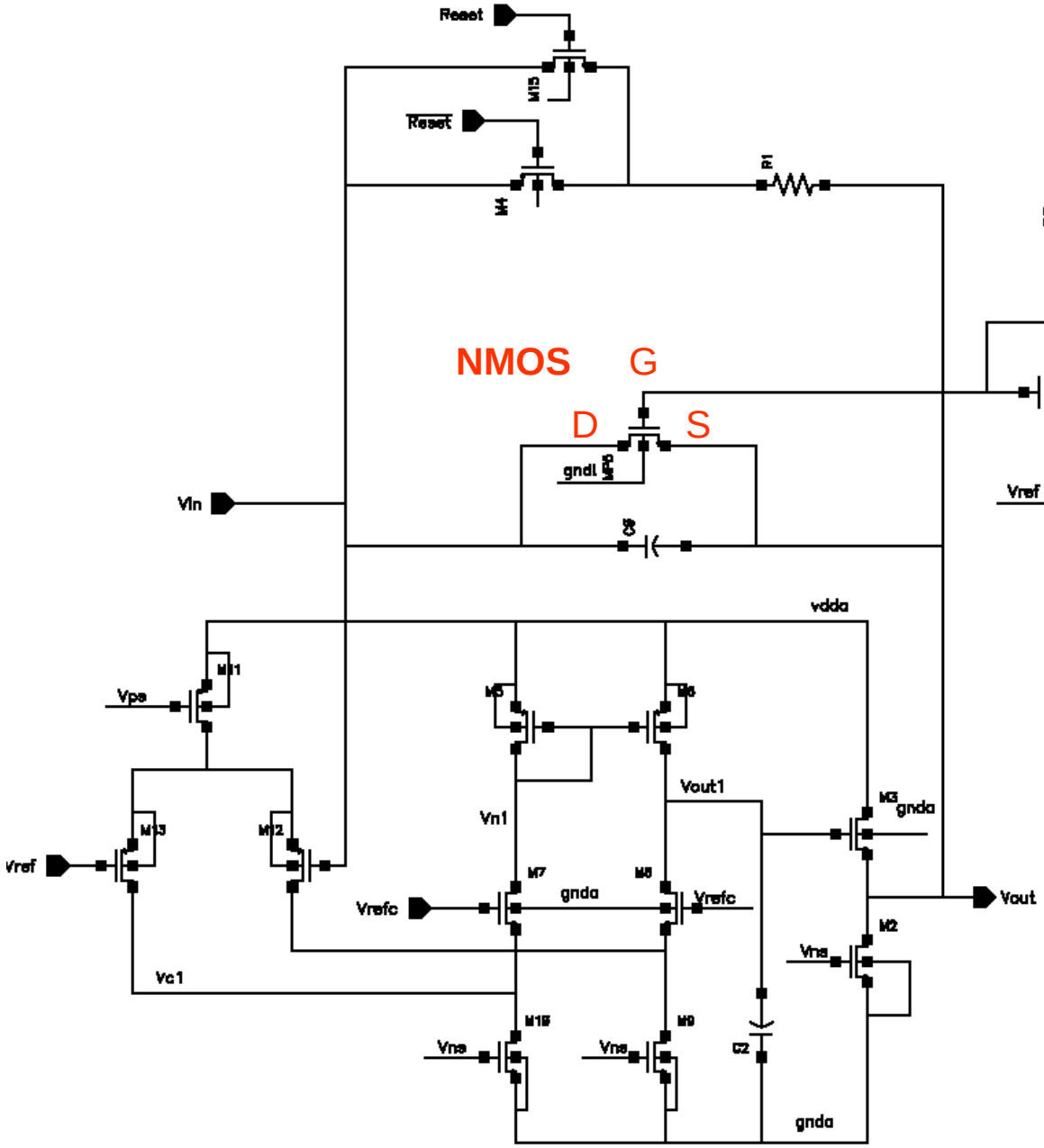


Linearity

30M resistor - no capacitance



30M with capacitance



NMOS feedback

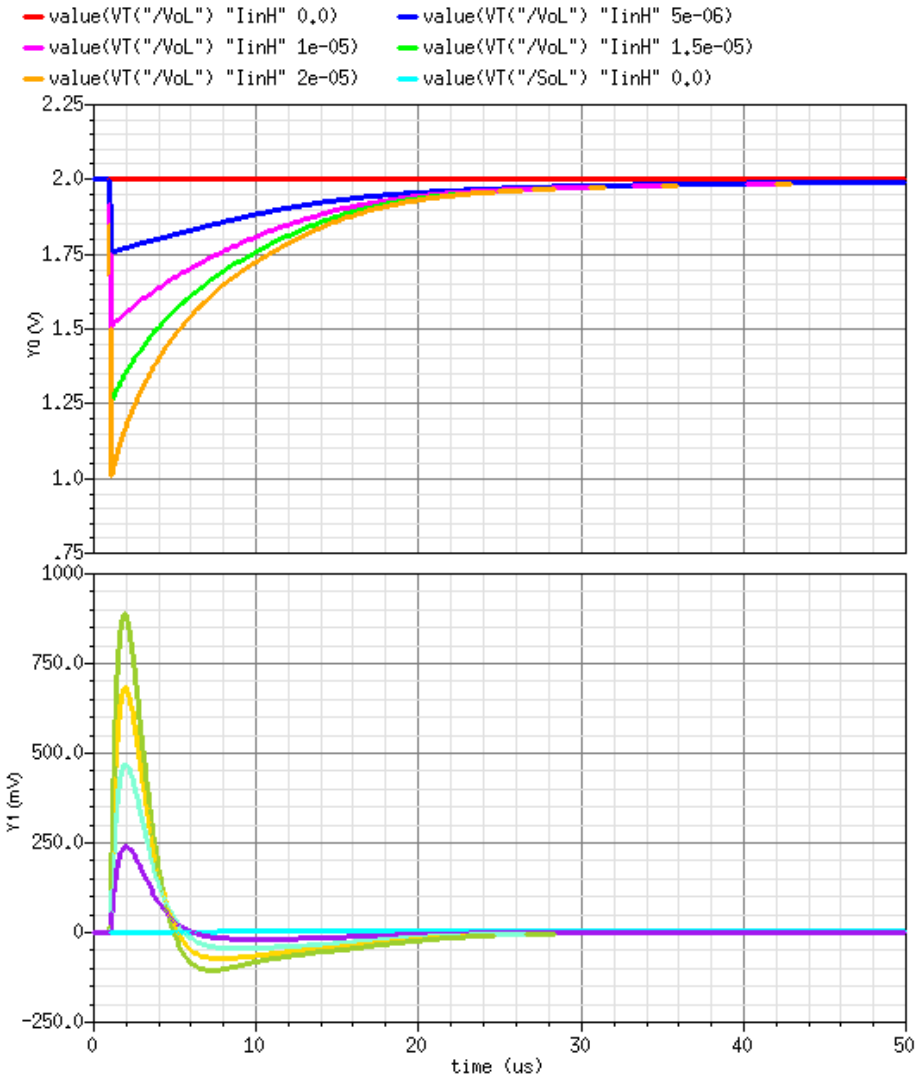
Source follows output

Gate fixed.

Vgs varies with output

Feedback is resistive, but highly variable

NMOS feedback



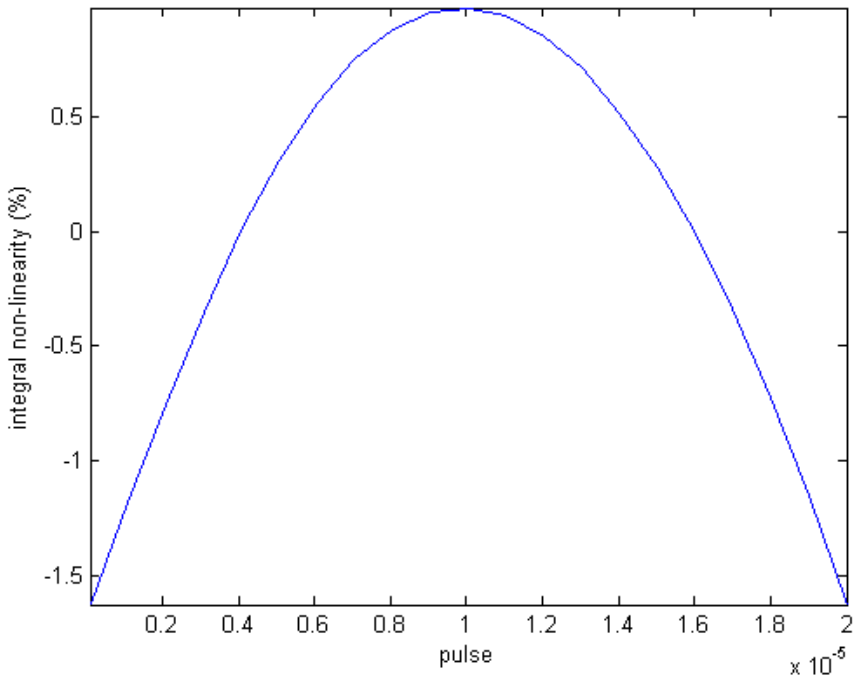
1nA feedback current

W=1um, L=50um feedback device

Pole-zero adjusted for 30MΩ

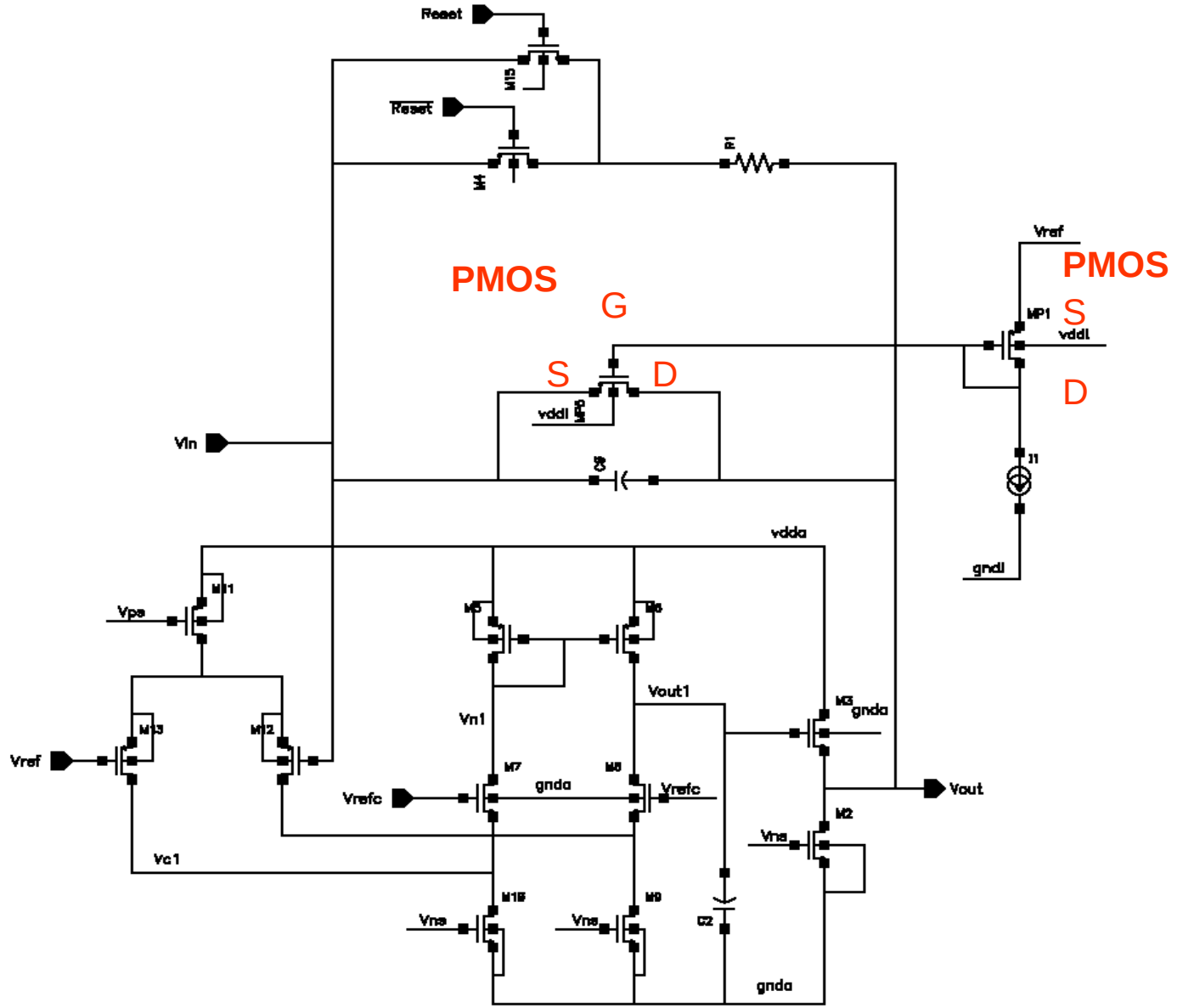
Undershoot gets worse for large signals

NMOS feedback linearity



1nA feedback current

W=1um, L=50um feedback device



PMOS feedback

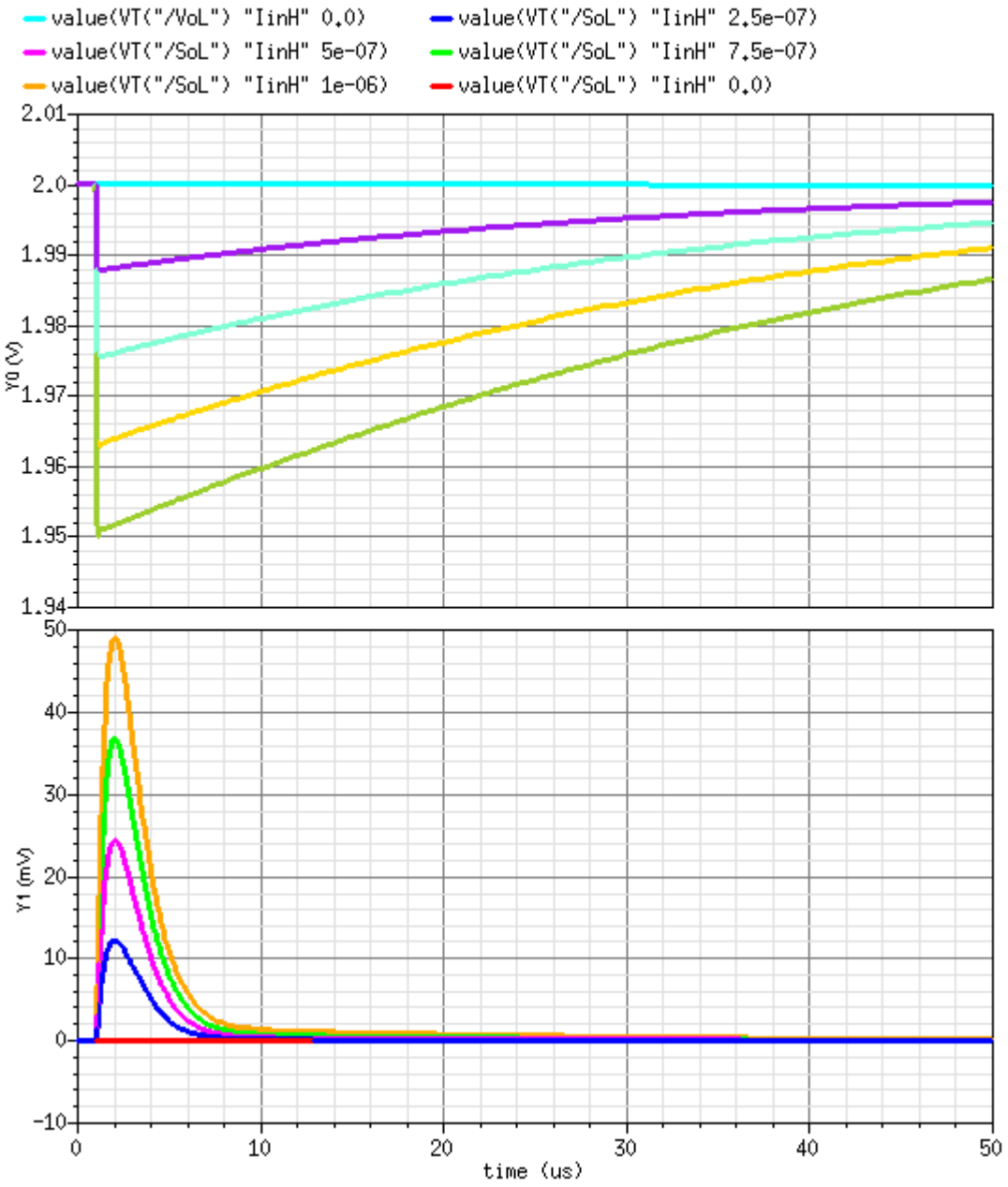
Source at Vref

Gate fixed

Drain follows output

Vgs constant

PMOS feedback



Small signals 0-1uA

Ifb= 1.3nA

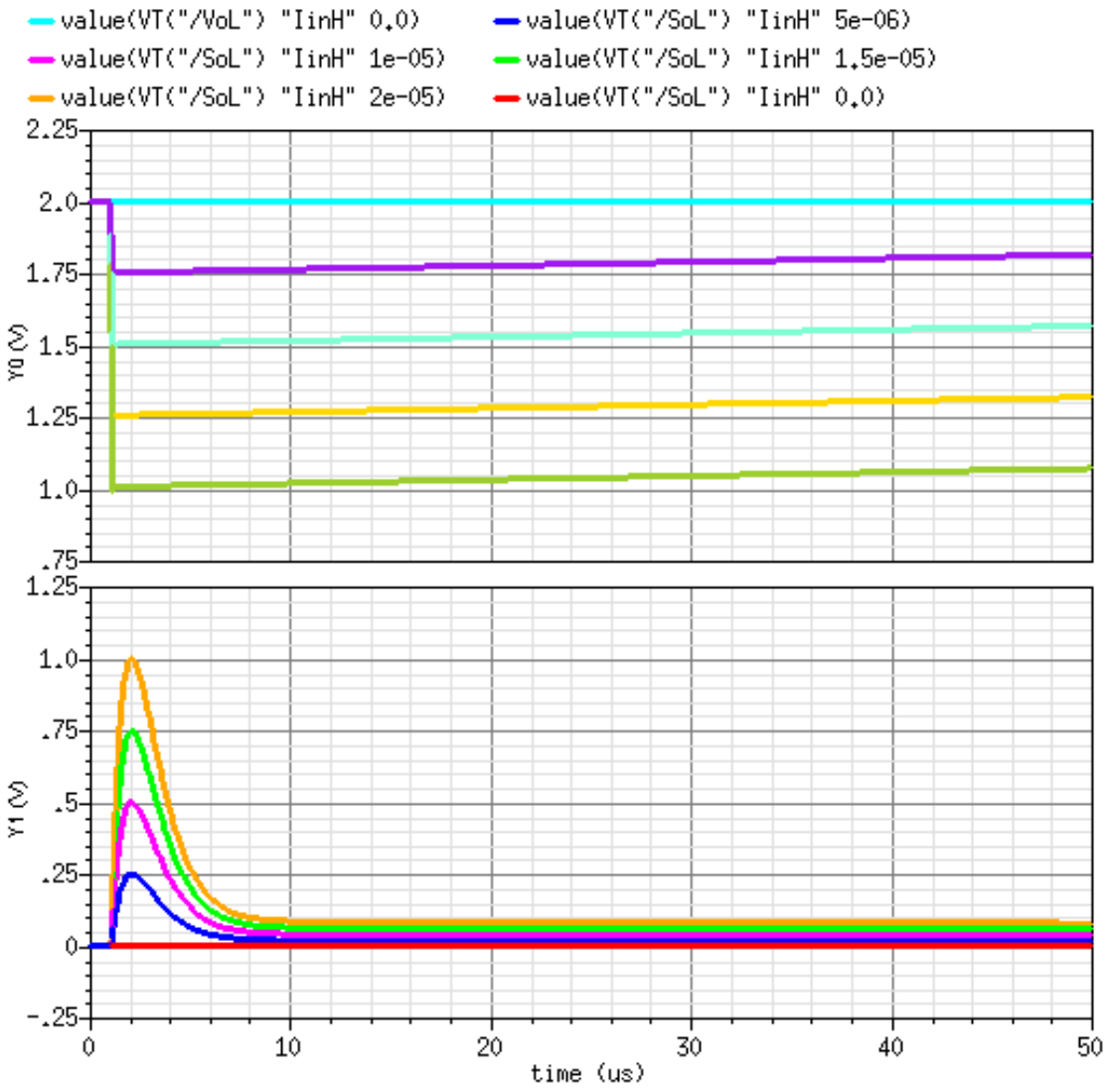
W=1um, L=20um

Linear response

Vgs-Vt > Vds

Resistive feedback

PMOS feedback



Large signals 0-20uA

Ifb= 1.3nA

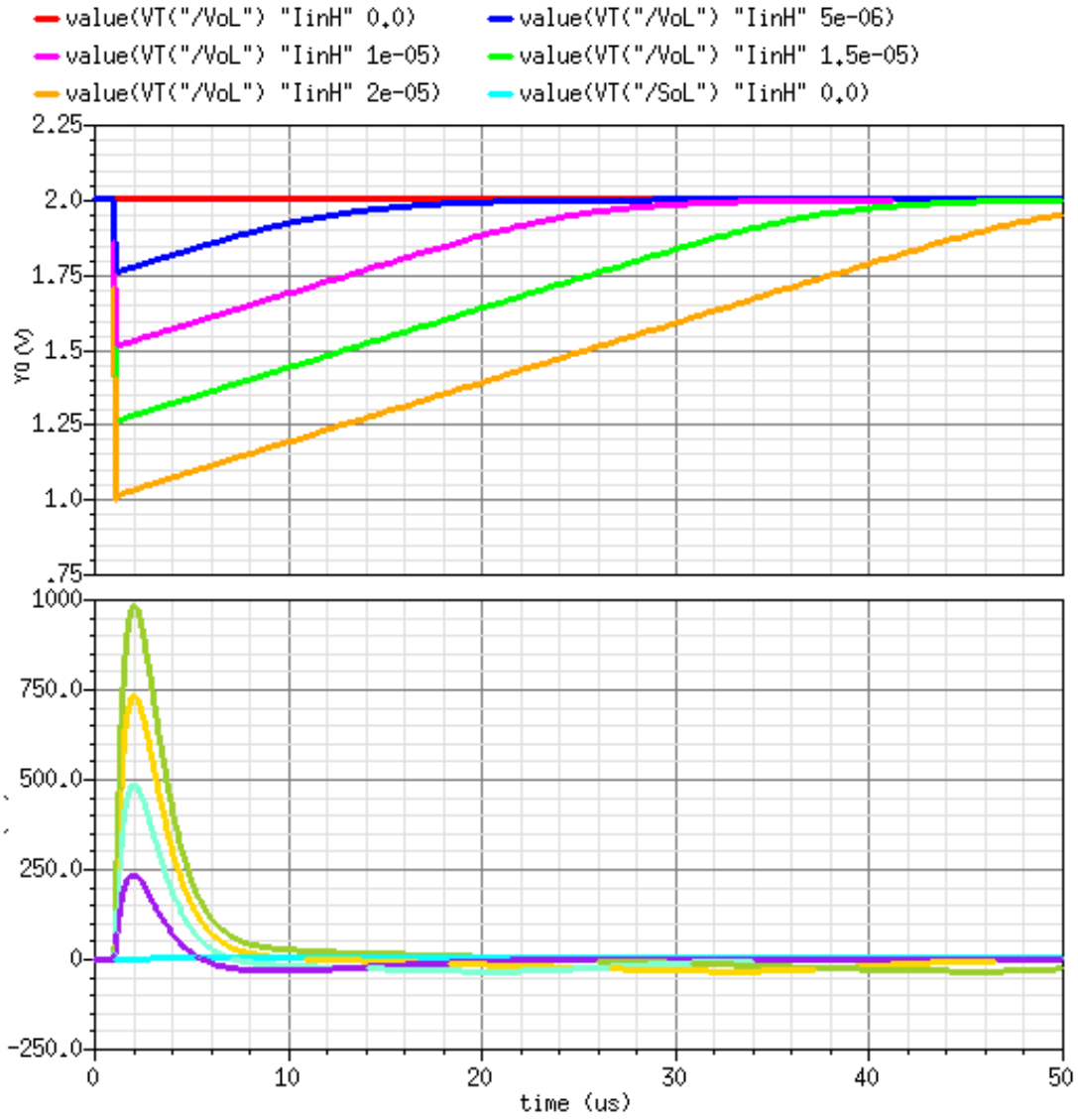
W=1um, L=20um

Saturated response

Vgs-Vt < Vds

Feedback transistor acts as constant current source

PMOS feedback

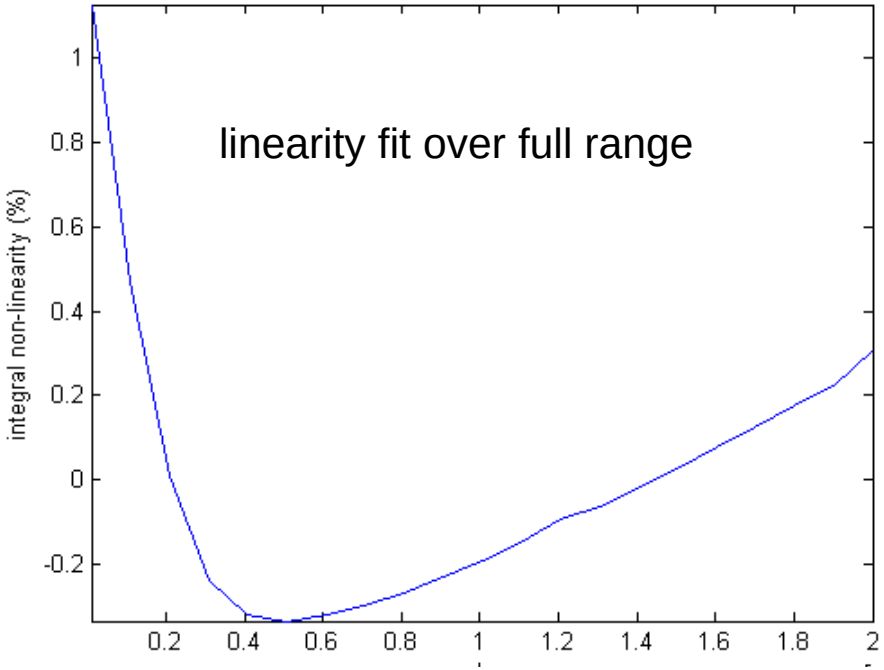


Large signals 0-20uA

Ifb= 20nA

W=1um, L=20um

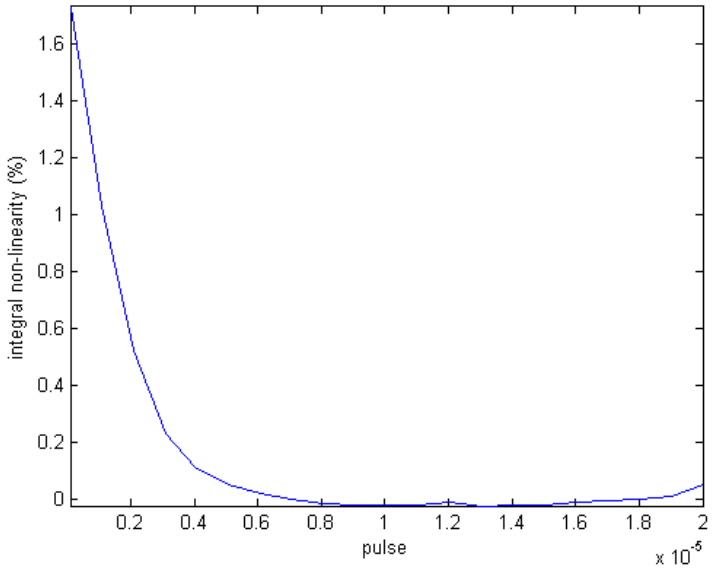
PMOS feedback linearity



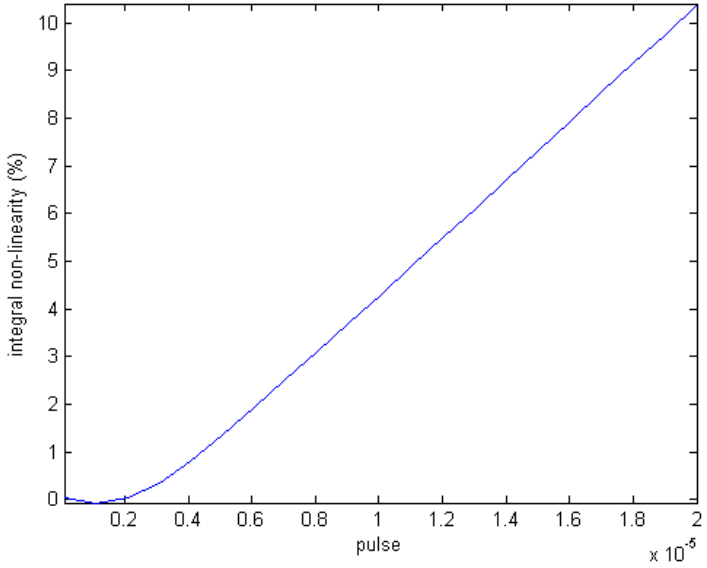
Large signals 0-20uA

Ifb= 20nA

W=1um, L=20um

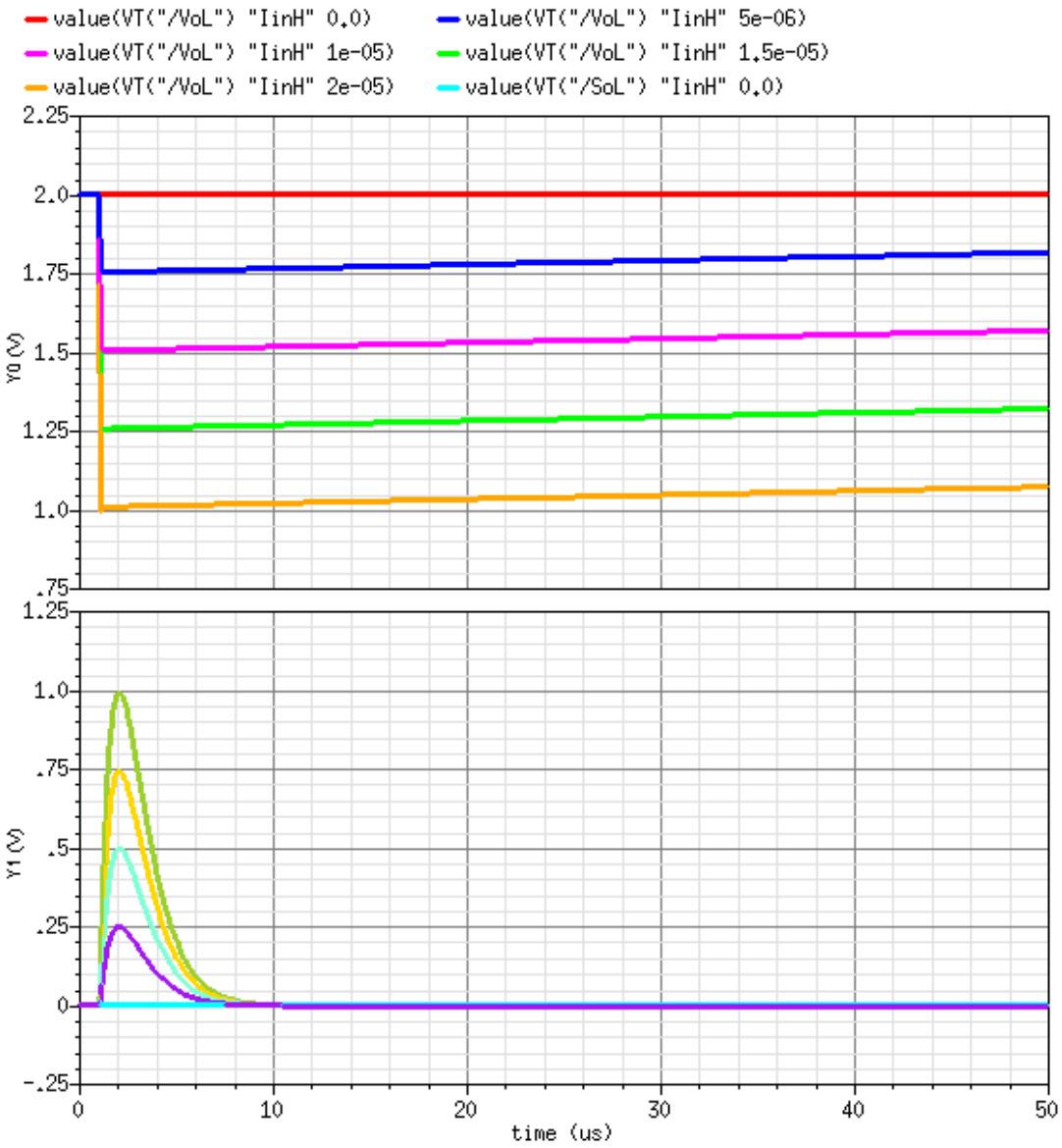


linearity fit for large signals



fit for small signals

PMOS feedback



No pole-zero cancellation,

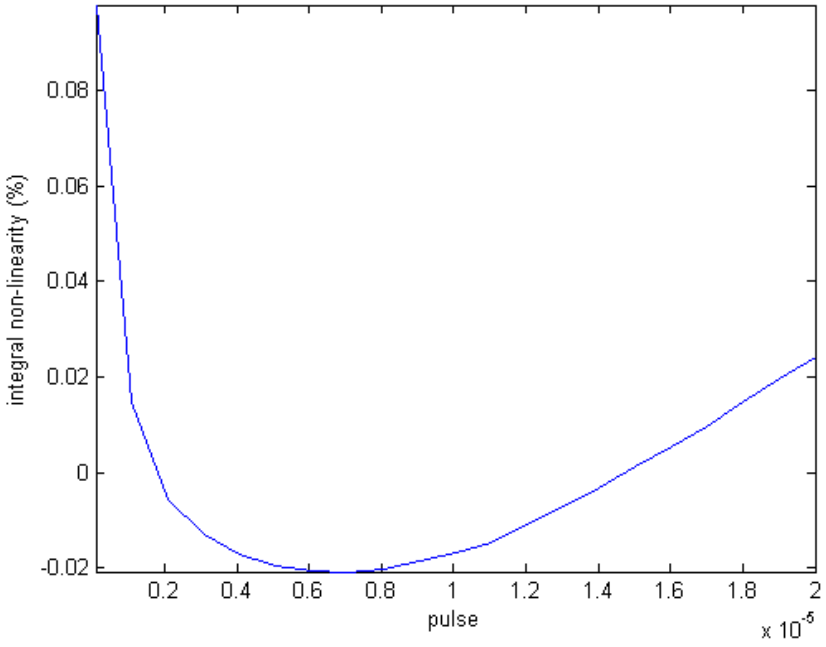
slow recovery

Large signals 0-20uA

Ifb= 1.3nA

W=1um, L=20um

PMOS feedback linearity



No pole-zero cancellation

Large signals 0-20uA

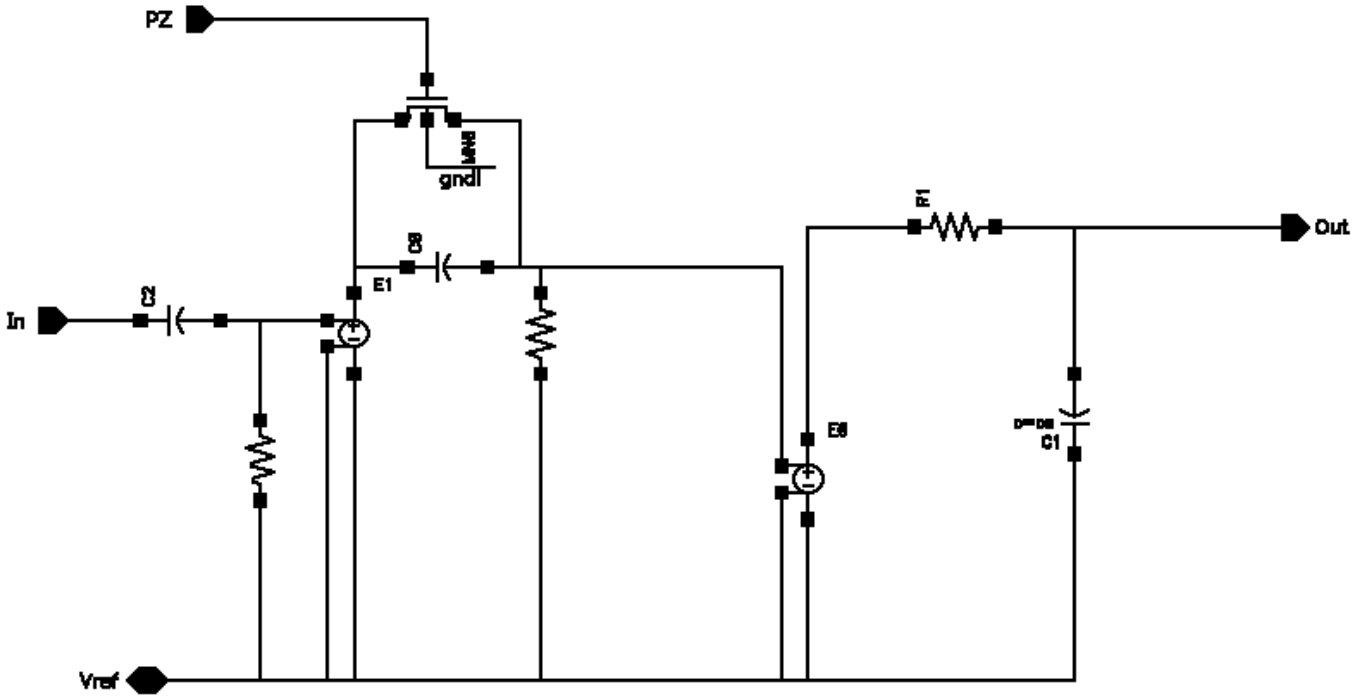
Ifb= 1.3nA

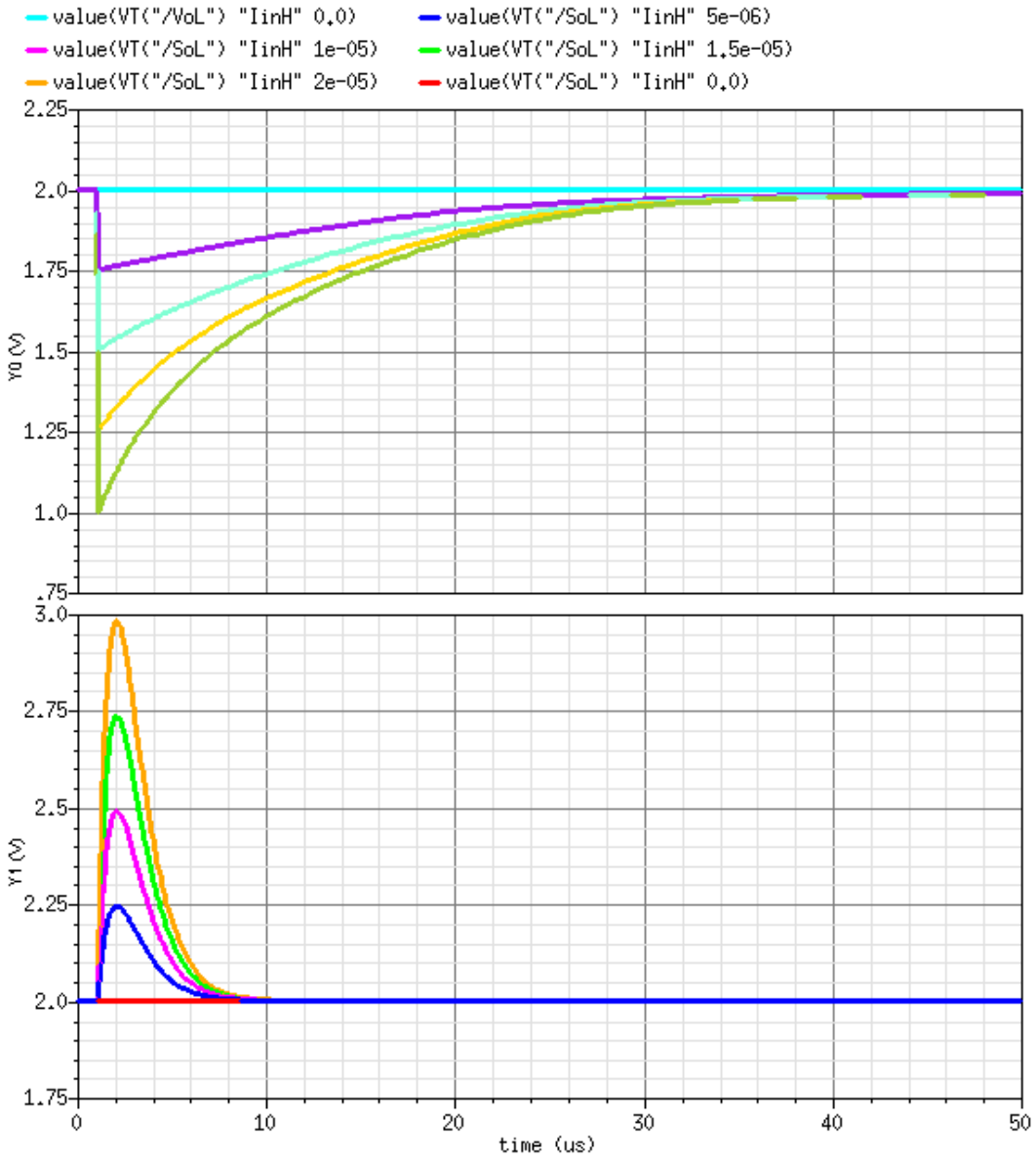
W=1um, L=20um

NMOS linearity compensation

PZ resistor replaced by transistor

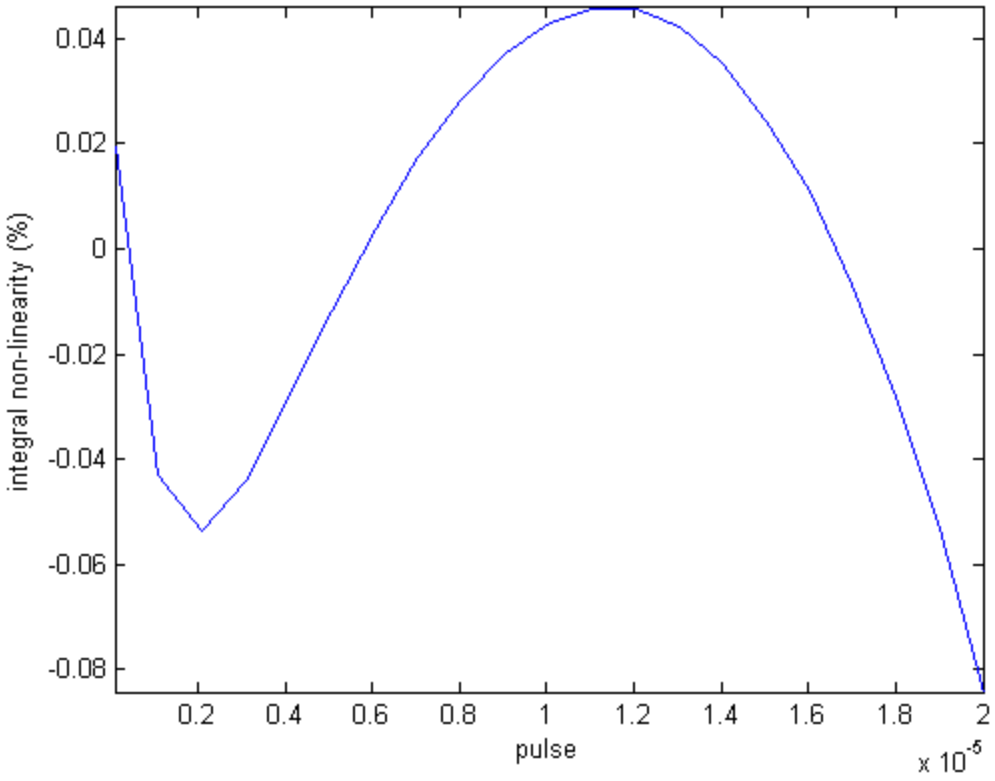
Bias conditions match feedback device





NMOS feedback with compensation

NMOS feedback with compensation



Linearity

Conclusions

- At least 3 options for amplifier feedback

  1 resistor - linear, but problem with parasitic capacitance

  2 NMOS - variable resistor feedback, difficult to achieve slow preamp recovery

  3 PMOS - current source feedback, linear if recovery is slow.

- Non-linearity can be compensated to some degree

  Pole-zero resistor replaced by a transistor at the same bias point as the feedback device