AIDA design review

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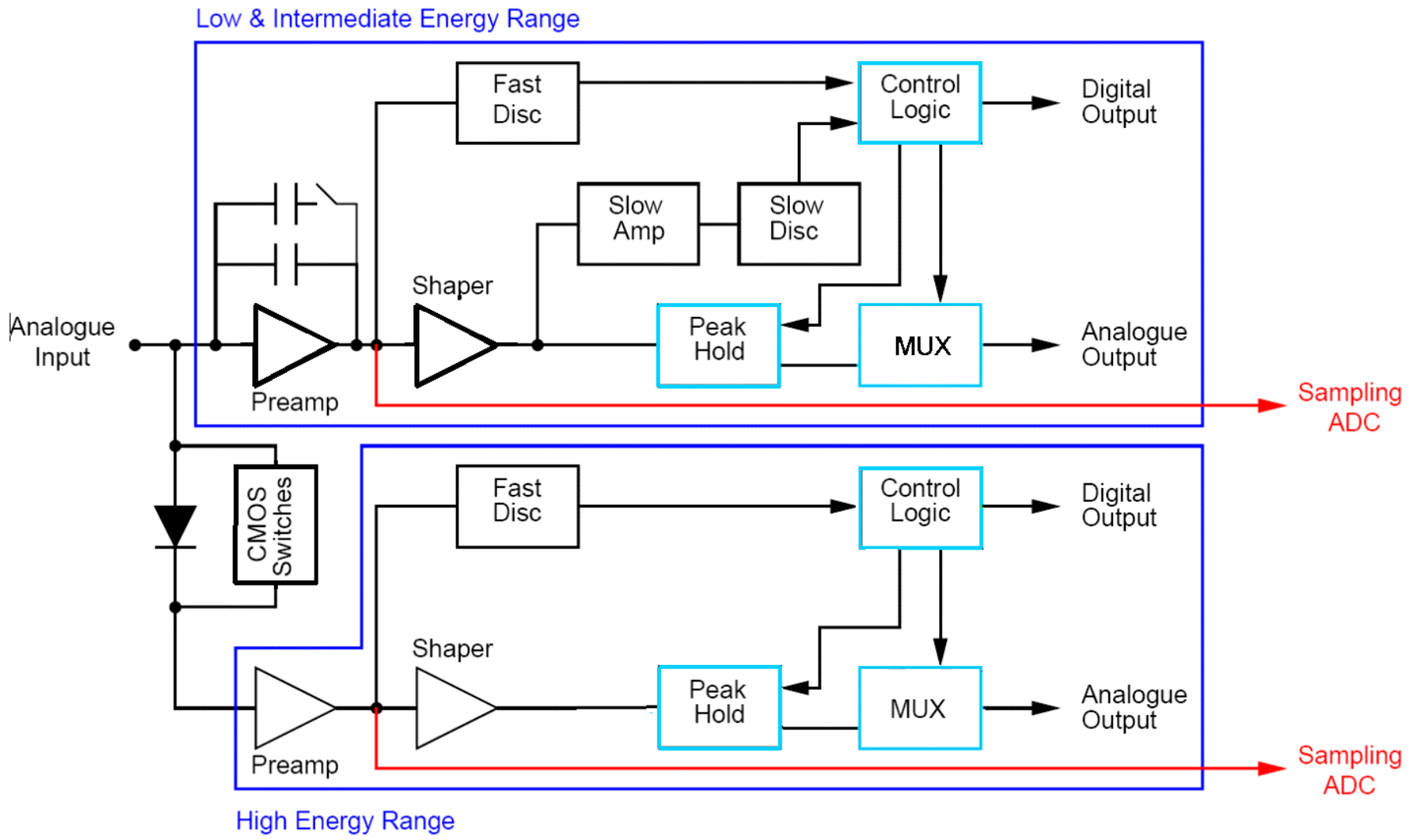
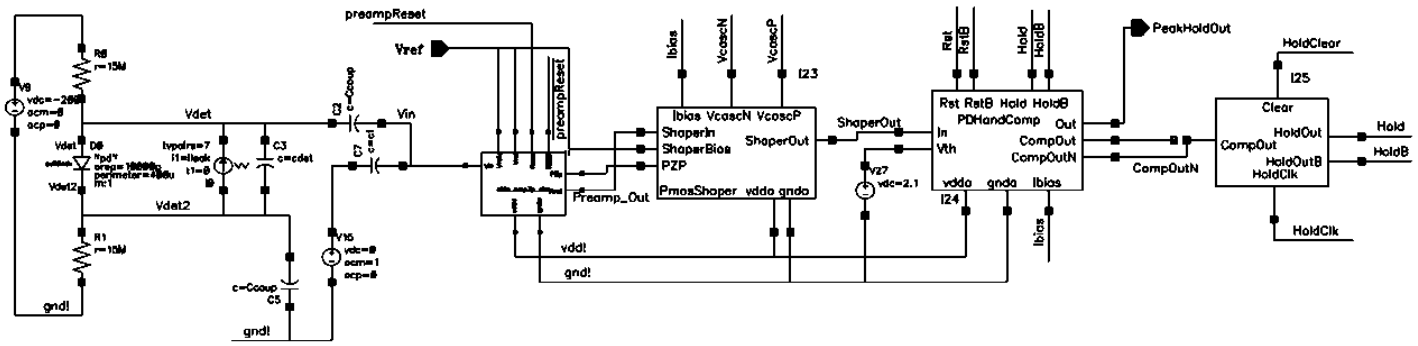
Overview

- Design status from July 2007
- Digital design progress:
  - Data-driven read-out
  - Multiple hits
  - Peak-hold reset
- Additional features:
  - Link between high/low channels
  - Flexibility in read-out architecture
- Next steps:
  - Analogue optimisation (new detector model)
  - Top-level design and layout

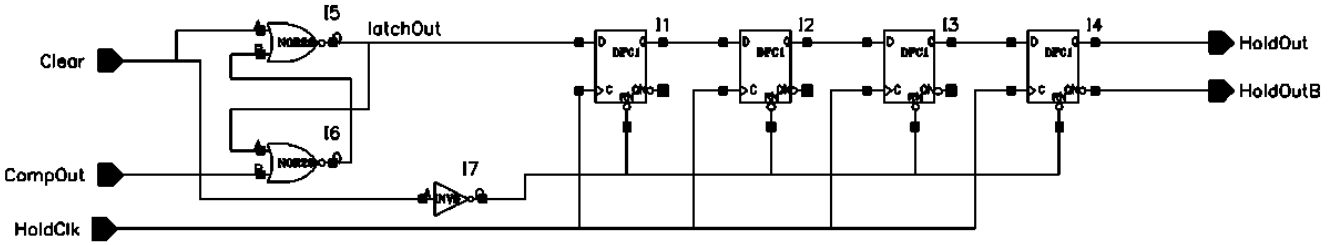
Design focus: control logic, mux, peak hold



Status of design in July:
Analogue channel, with peak-hold gating



Pre-amp Shaper Peak-hold/Comparator Latch



Hold latch - 4 clock cycle delay from Compout to Holdout

Progress on digital design

- Top-level digital design implemented (based on ERD)
- Provides control of
  - power-on reset
  - peak-hold gating
  - sparse read-out, with pointer logic
  - address generation
  - reset of peak-hold/comparator after read-out
- Design needs to be extended for pre-amp, shaper and clamp reset

Digital function 1

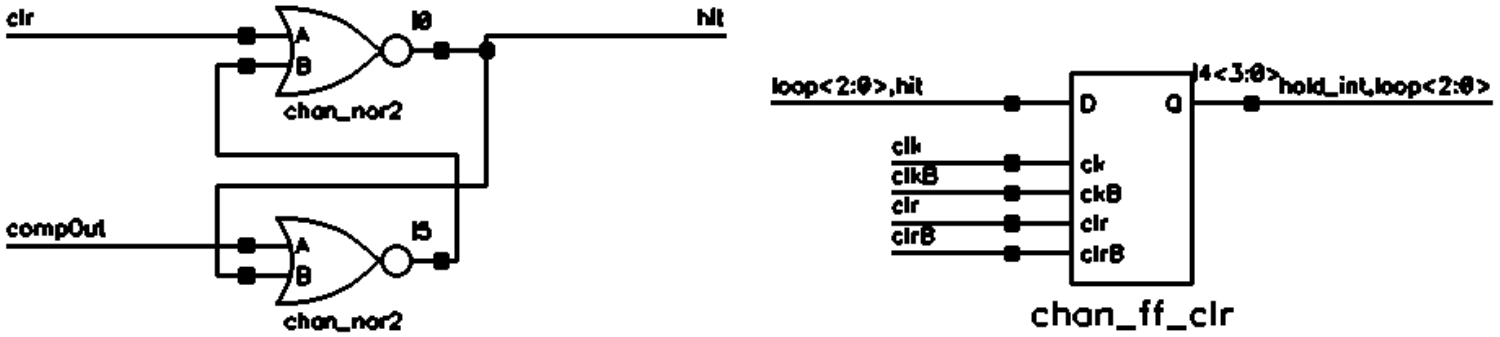
Power on sequence:

- Initialisation of digital circuits (asynchronous reset)
- Pre-amp / shaper reset for all channels (timing dependent on clock)
- Extended reset of peak-holds / comparators.
- Generation of read-out pointer

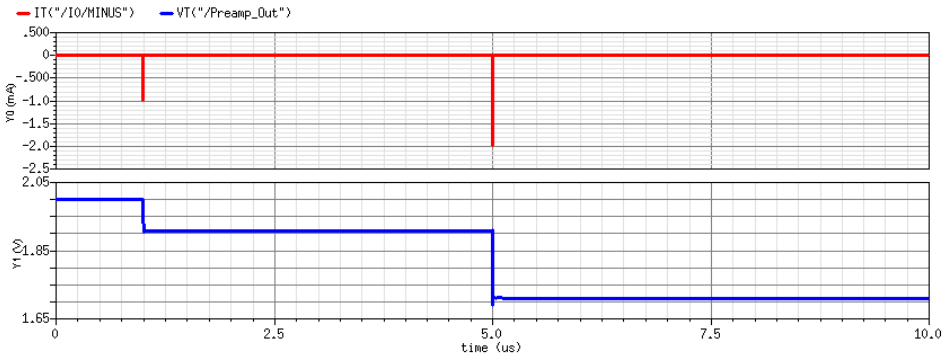
Digital function 2

Peak-hold control:

- The peak-hold continuously monitors the shaper output
- When the shaper goes above threshold, the comparator output sets the read-out hit flag
- The hold signal is generated after a set number of clock cycles. This prevents the peak-hold from responding to new voltage peaks.
- The hold is released at the end of the read-out phase

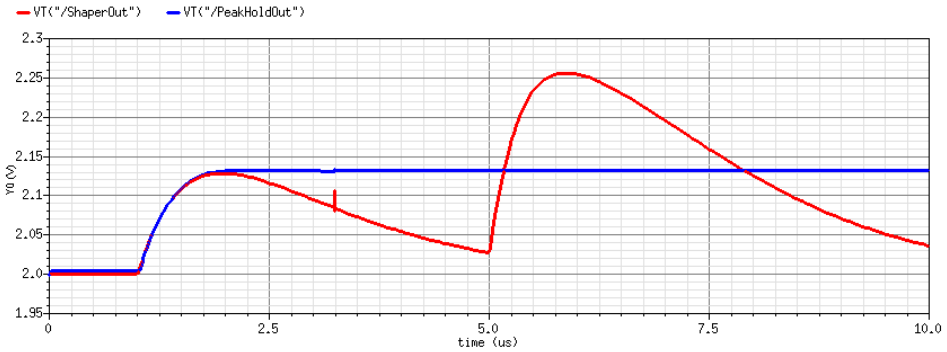


Peak-hold gating



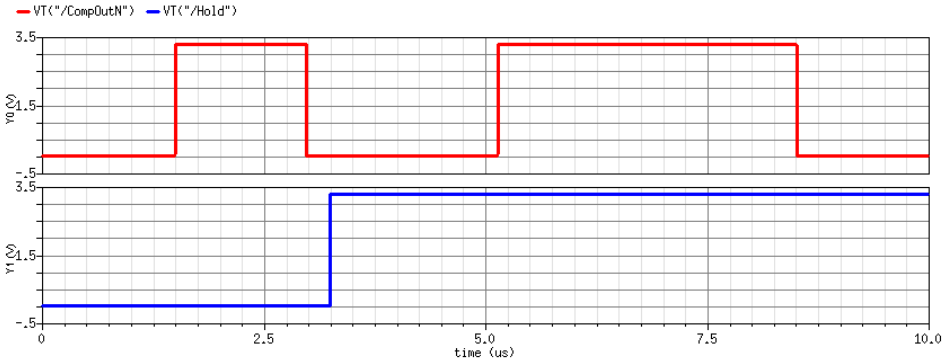
Detector current (1pC, 2pC)

Pre-amp output (Cf=10pF)



Shaper output (1μs peak)

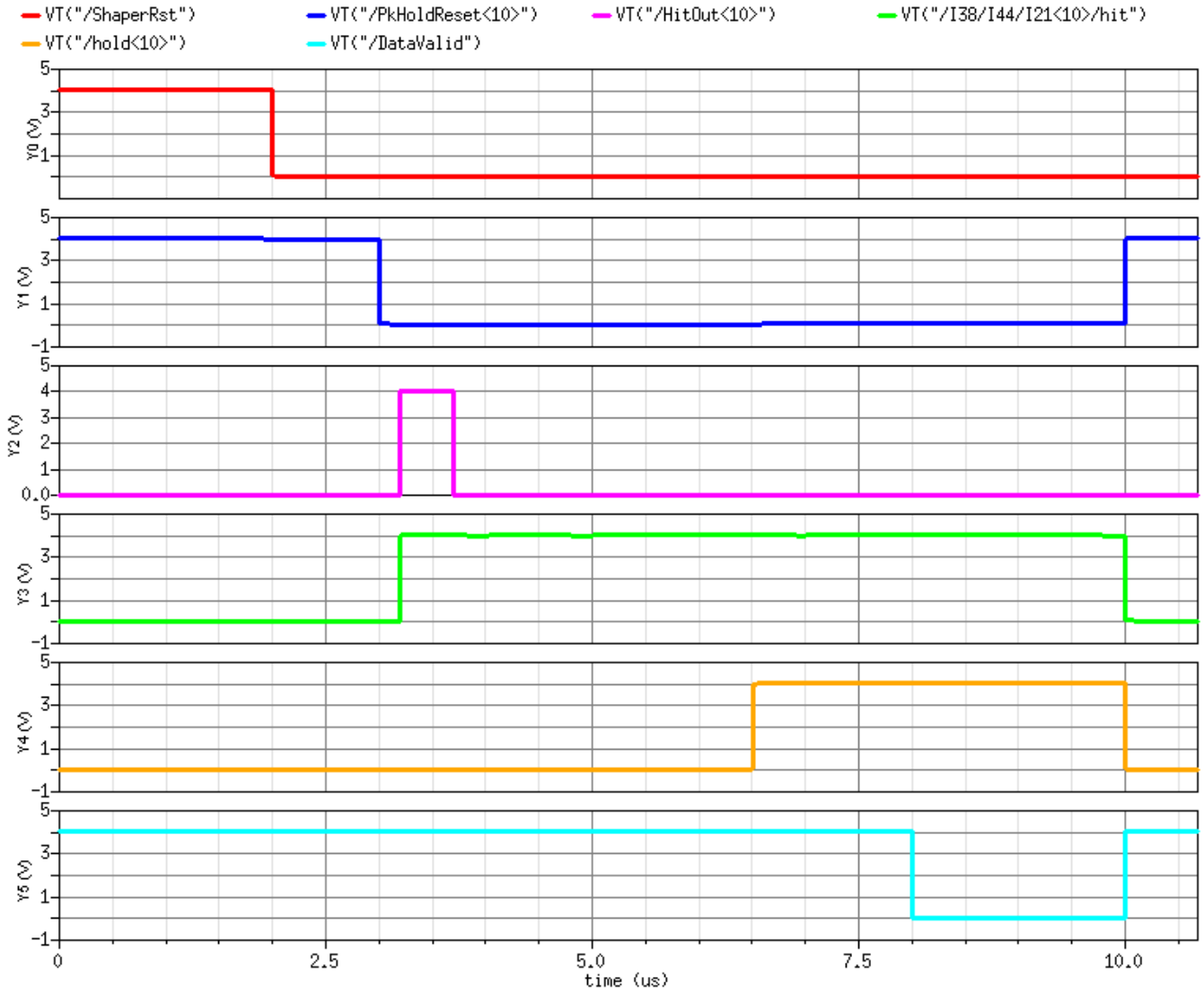
Peak-hold output



Comparator output

Peak-hold gate

Simulation of comparator initiating read-out



Shaper reset

Peak hold reset

Hit Out <10>

Hit flag

Hold

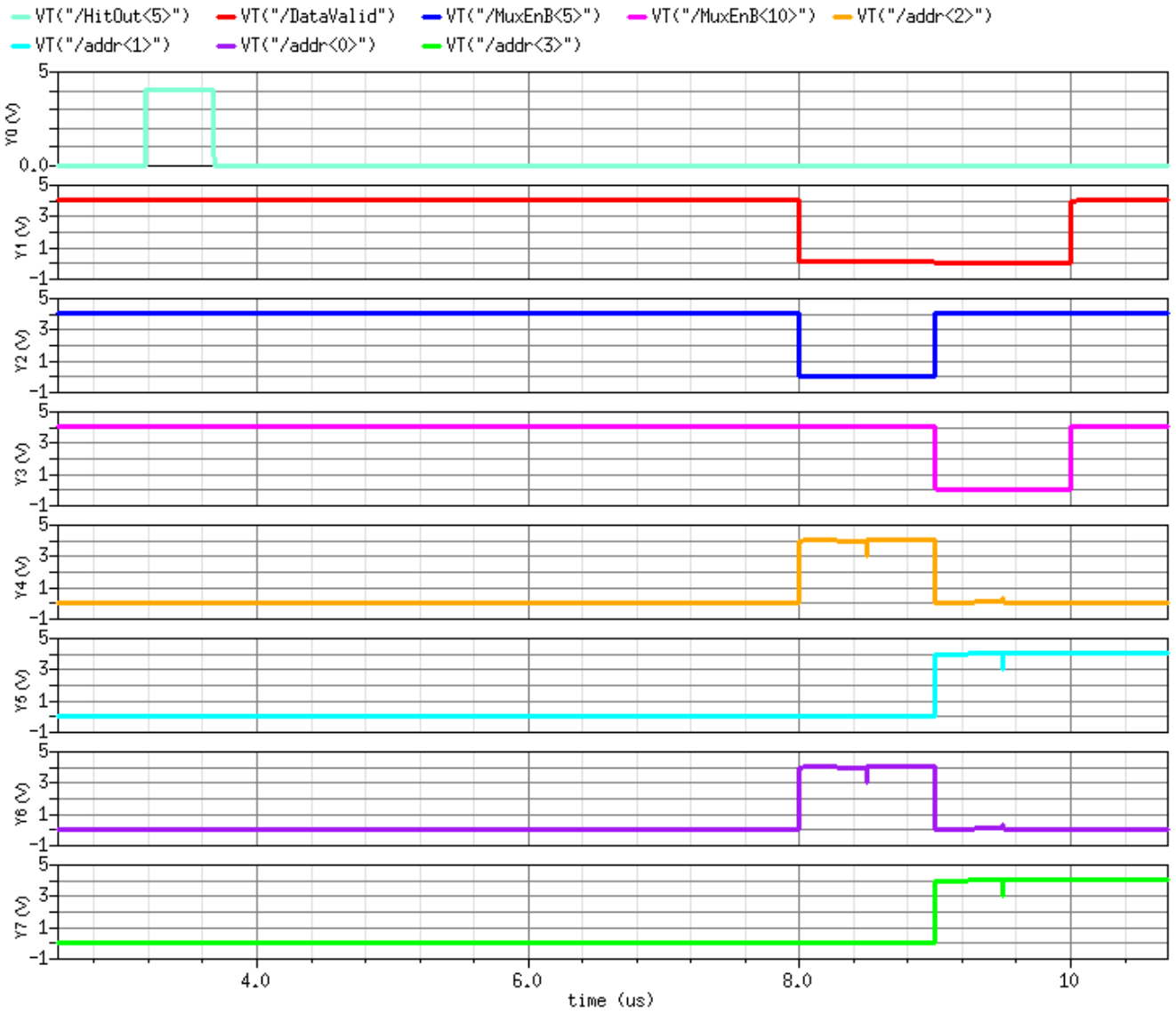
Data valid

Digital function 3

Pointer logic:

- The comparator hit sets the read-out flag for a channel
- The pointer passes from channel to channel, stopping where a flag is set
- The multiplexer is enabled and the 4-bit address is generated
- The analogue voltage is available from the mux for one clock cycle, then the pointer moves on.

Simulation of 2 hit channels



Hit Out<5> and <10>

Data valid

Mux enable <5>

Mux enable <10>

address <0>

address <1>

address <2>

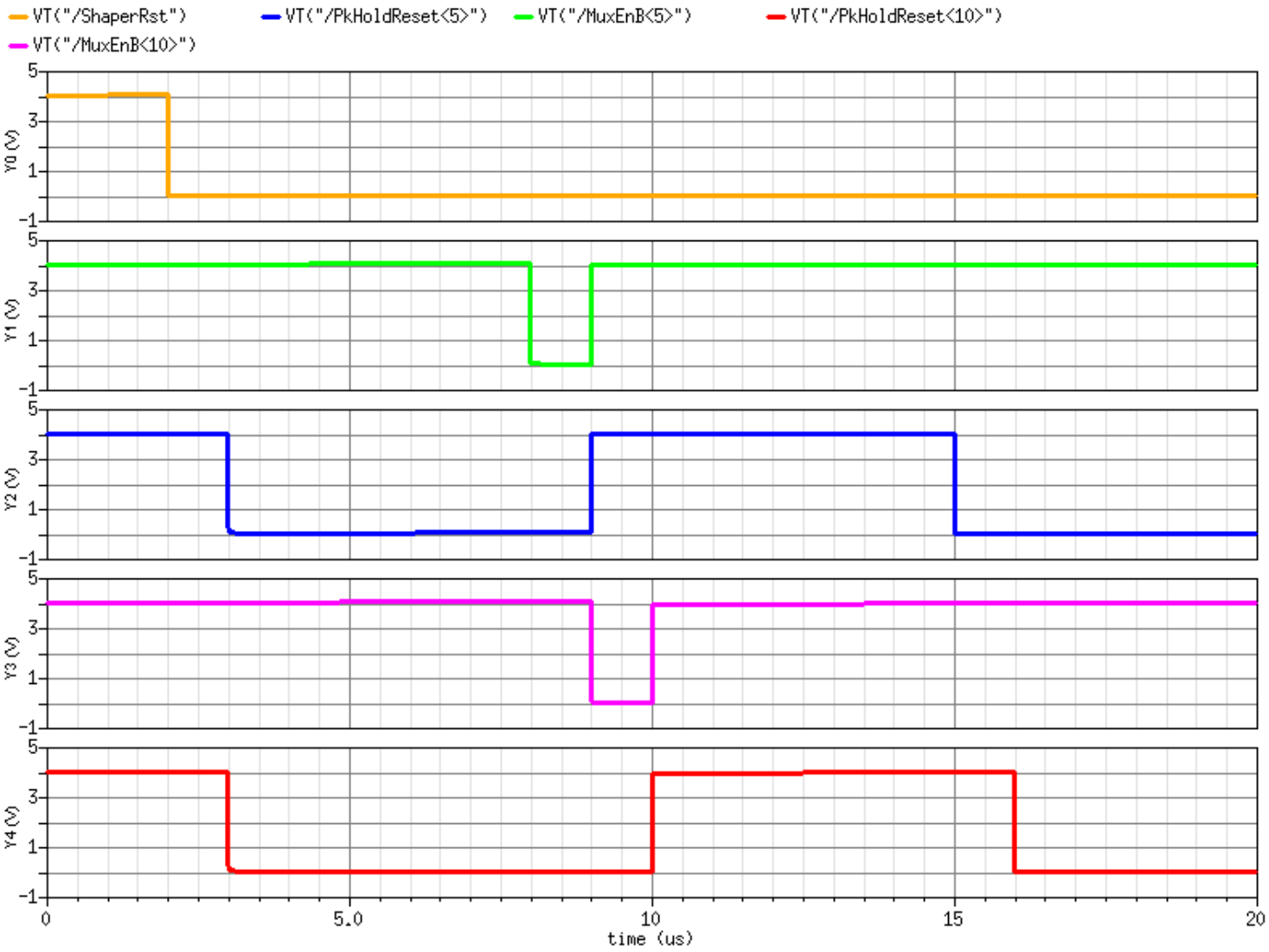
address <3>

Digital function 4

Channel reset:

- The peak-hold and comparator need to be reset after each channel is read out
- The reset is held on for a adjustable time (N clock cycles) . This allows time for the pre-amp/shaper to recover from reset and stabilise
- The time delay is generated by a single shift register block (not repeated for each channel)

Peak-hold extended reset



Shaper reset

Mux enable <5>

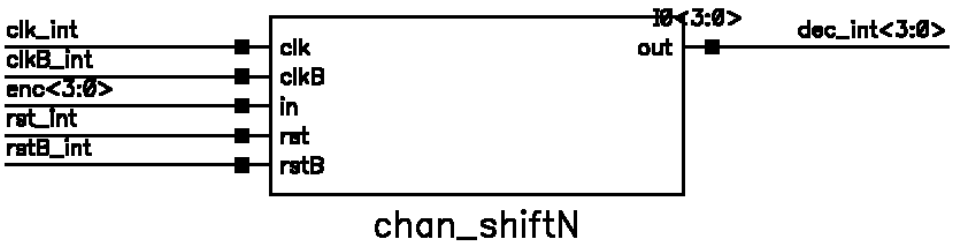
Peak hold reset <5>

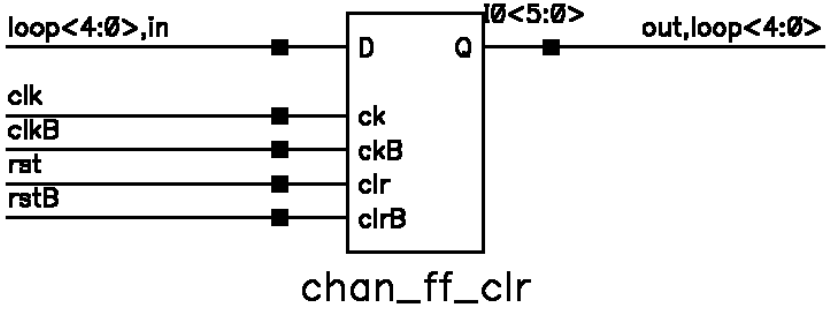
Mux enable <10>

Peak hold reset <10>

Channel reset control

- The channel number (0-15) is encoded into 4 bits
- The bits feed into an N-bit shift register (N~20)
- The output is the delayed channel position
- The 4 bit code is decoded back to channel number
- The selected channel is reset
- N can be software controlled, over a wide range.



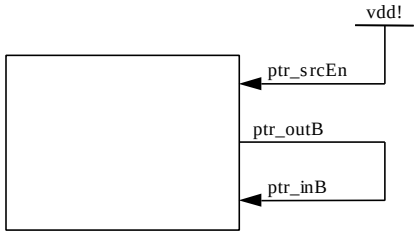


Link between low / high energy channels

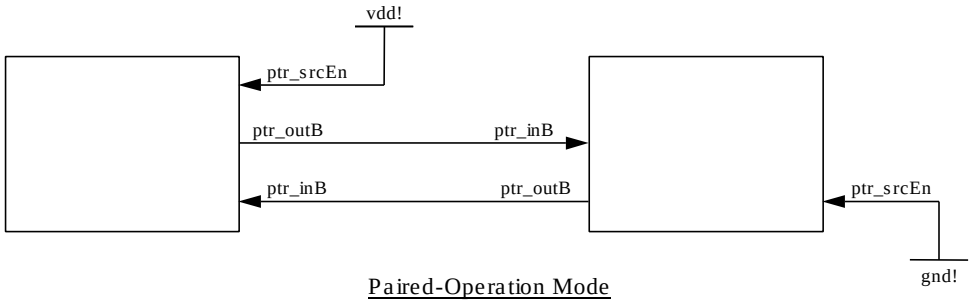
- The control logic by default treats each channel as independent (not true for high/low ranges of a single channel)
- The logic could be optimised for quick recovery of the low energy range, after a high-energy implant event (with fast amplifier reset, rather than attempting a full read out)
- The two control blocks (p3) should therefore be regarded as a single (combined) design

Flexible read-out option

- The pointer logic was originally designed for a paired configuration
- The pointers are externally accessible, so two chips can be sparsified together (with a single analogue output and combined addressing)



Stand-alone Mode



Paired-Operation Mode

This flexibility could be retained on AIDA, with no penalties in single-chip format (stand-alone mode)

Next steps:

- Additional manpower allocation (Davide Braga)
- Amplifier optimisation for smaller peak current (plasma model for detector)
- Investigation of polarity switching
- Top-level control circuit design
- Physical layout
- Target of January for design submission?
  (project plan assumed ~90% for 2007 ASIC design manpower - average so far is ~60%)