AIDA design review

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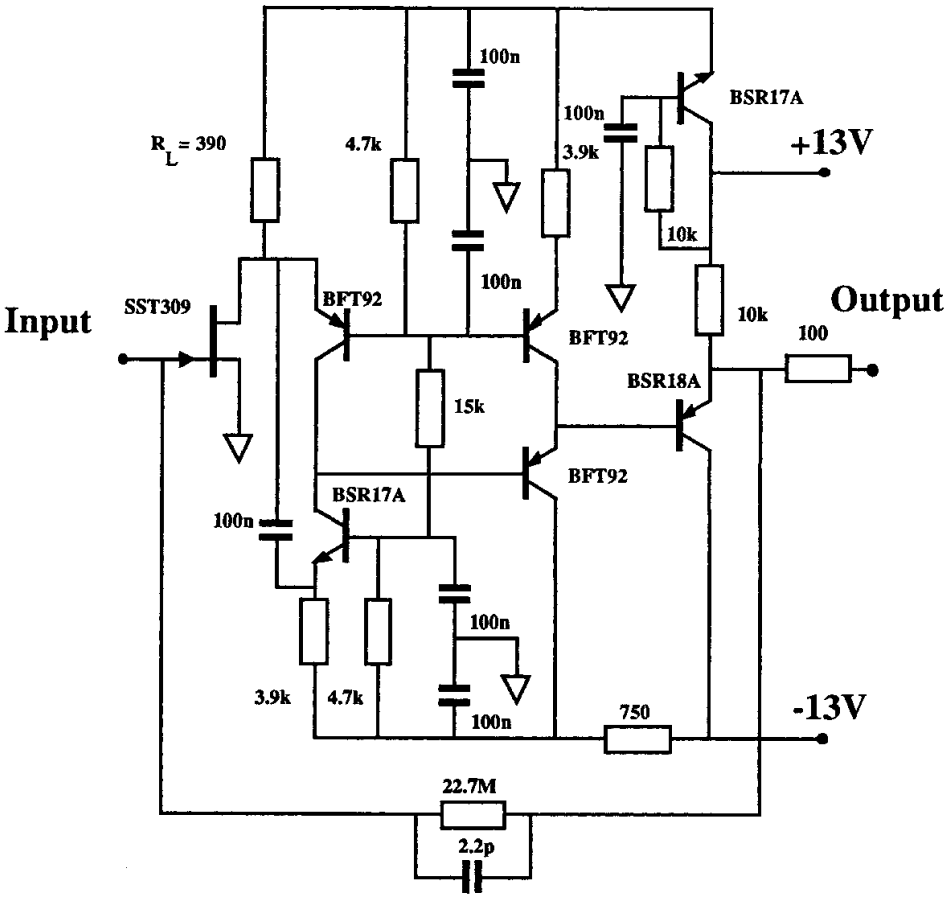
5 July 2007

Overview

- RAL108 review
  - Original configuration
  - High dynamic range
  - Detector tests
- AIDA simulations
  - Analogue channel
  - Mixed mode
  - Transient noise
- Future work

RAL108 pre-amplifier schematic



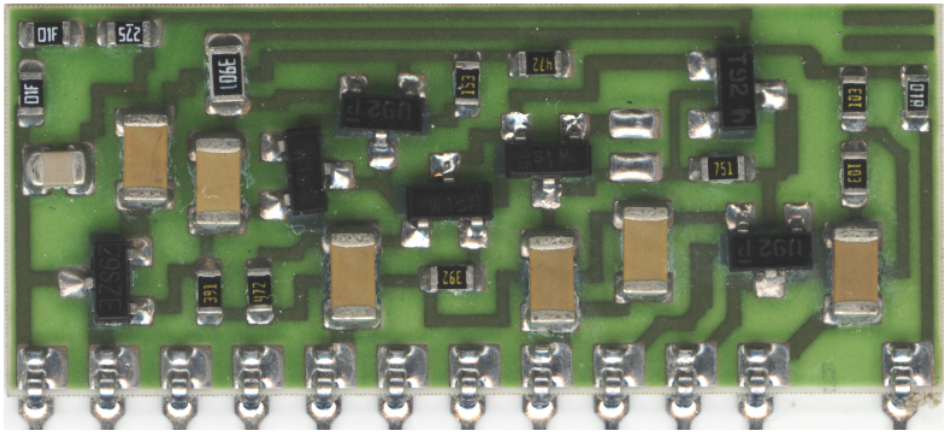
Standard configuration:

- 2.2pF // 22.7MΩ
- 50µs fall-time
- ~5-10ns rise-time

Features:

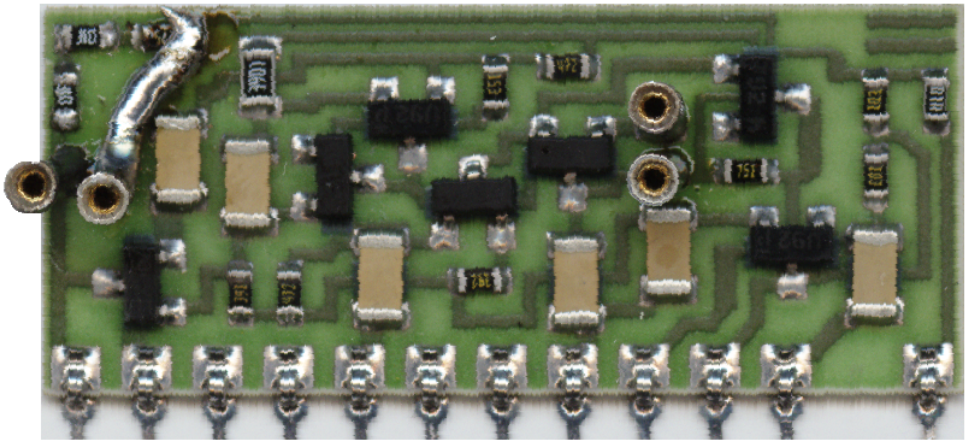
- Easily reworkable, for larger Cf
- Optional compensation (capacitor on internal node or resistor in series with Cf)

RAL108 pre-amplifier layout



2.2pF // 22.7MΩ feedback

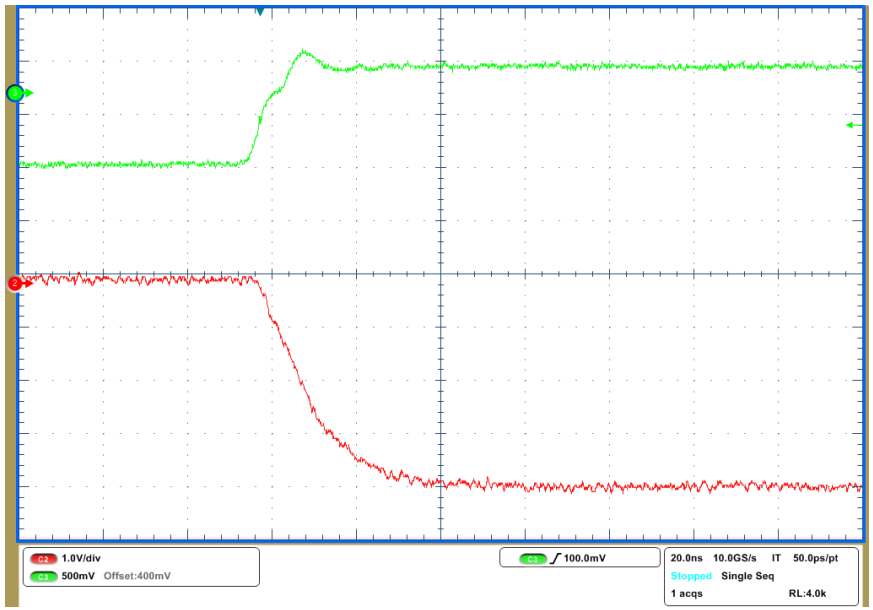
No compensation capacitor



Socket for 22pF or 220pF

Optional compensation

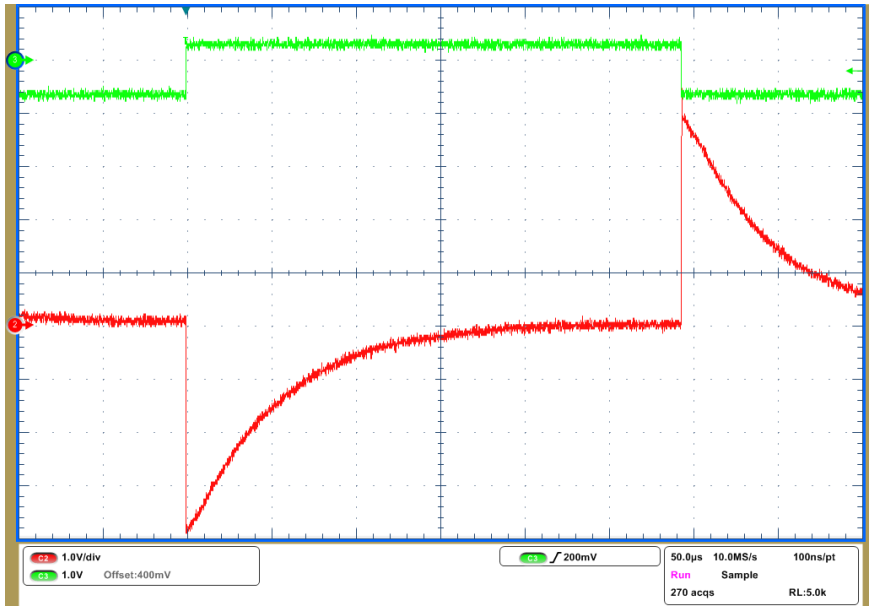
RAL108 2.2pF feedback



Input: 15ns 1V step on 10pF

Output: 20ns 4V step

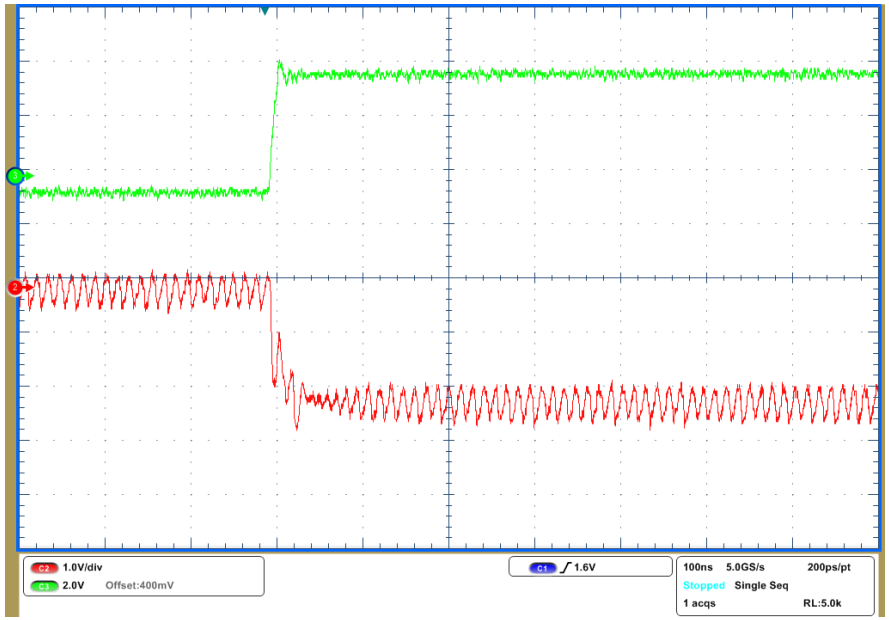
20ns/div



50 µs/div, 50 µs fall-time,

No termination resistor - full dynamic range for both polarities

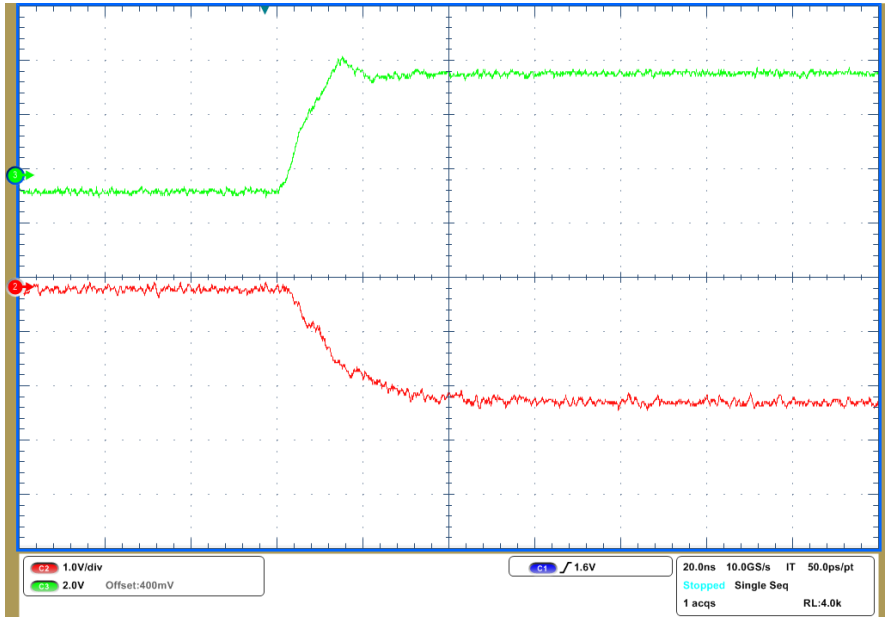
RAL108 22pF feedback



Input: 15ns 4.4V step on 10pF

Output: 2.1V step with oscillation

100ns/div

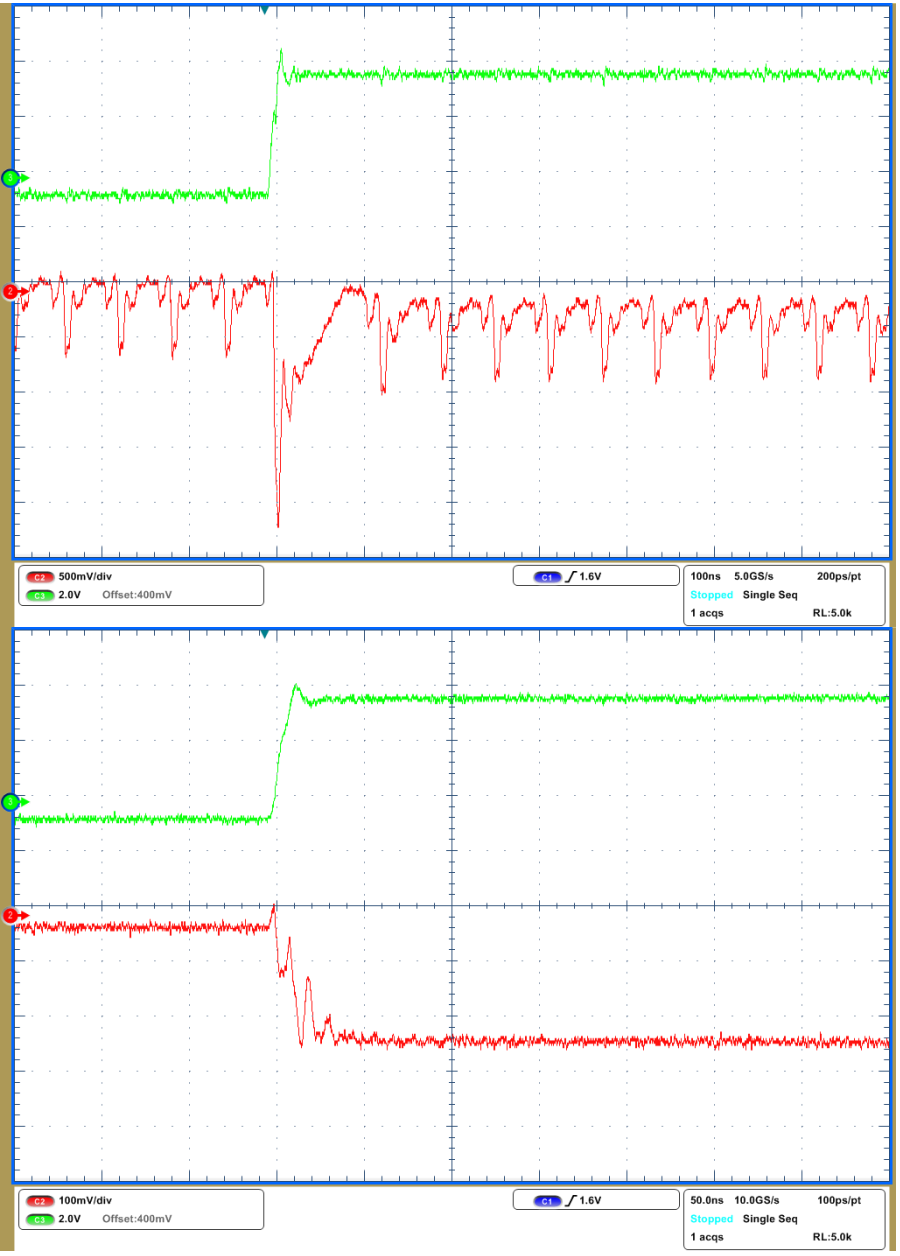


Result with 4.7pF compensation

20 ns/div

~30ns 2.1V step

RAL108 220pF feedback



Input: 15ns 4.4V step on 10pF

Output: Variable step with oscillation

100ns/div

Result with 22pF compensation

50 ns/div

~30ns 0.21V step with resonance

Resonance could be damped by larger compensation, or resistance is series with Cf

RAL108 detector tests

Aim :

To verify that the large detector charges can be read out quickly, without loss of signal

RAL108 capability:

Operation with 220pF feedback, ~1nC charge

Adjustment of compensation for best stability, rise-time

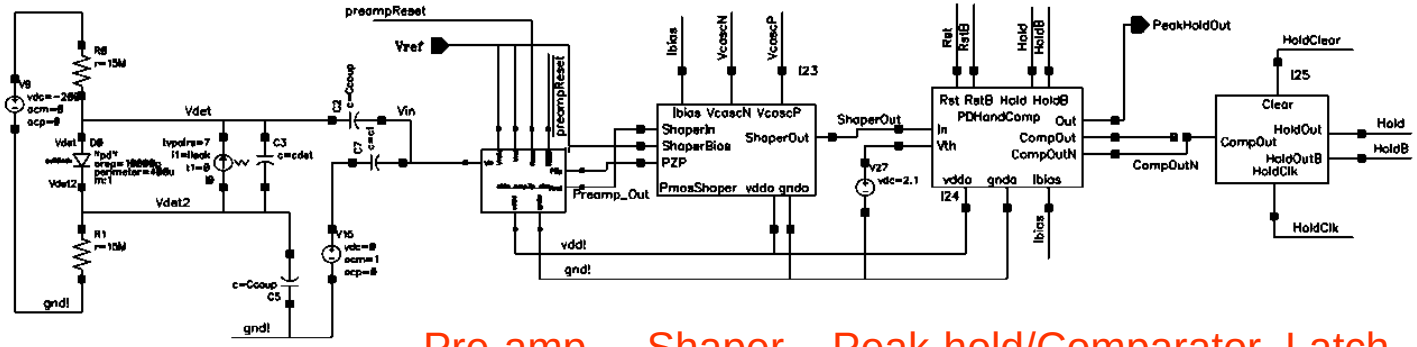
Shaper pole-zero can be matched to pre-amp

Next steps:

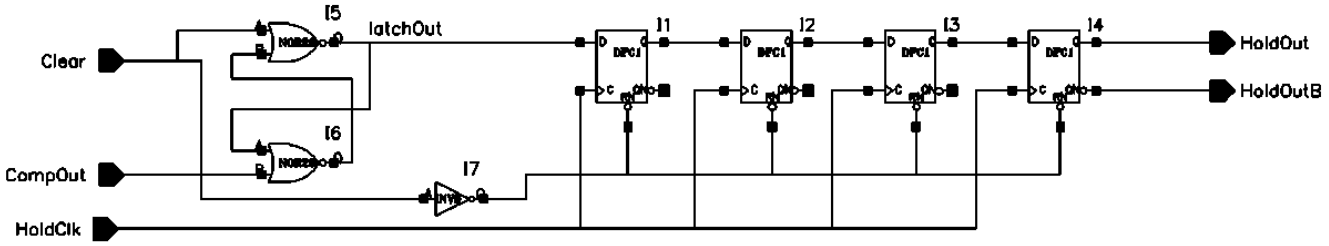
RAL108 batch with large Cf

Detector tests with IR laser or test beam

Analogue channel, with peak-hold gating

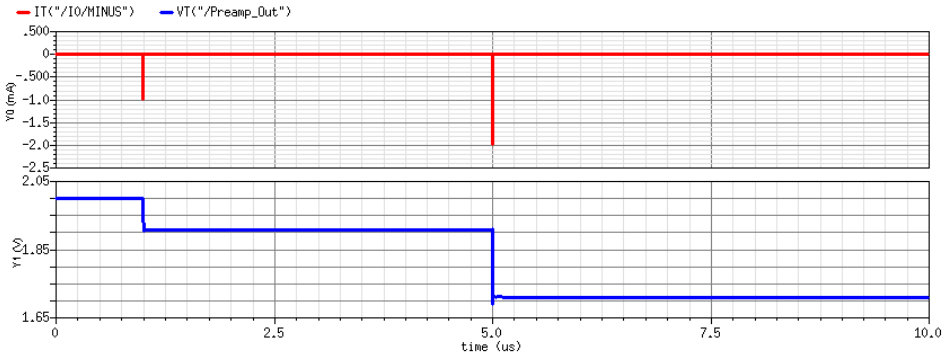


Pre-amp Shaper Peak-hold/Comparator Latch



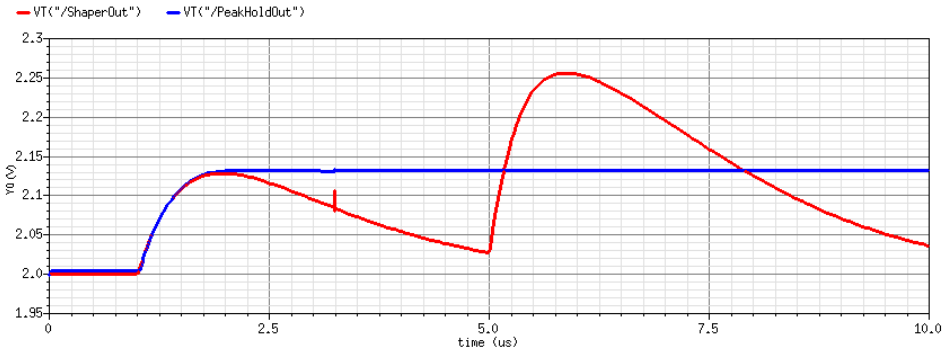
Hold latch - 4 clock cycle delay from Compout to Holdout

Peak-hold gating



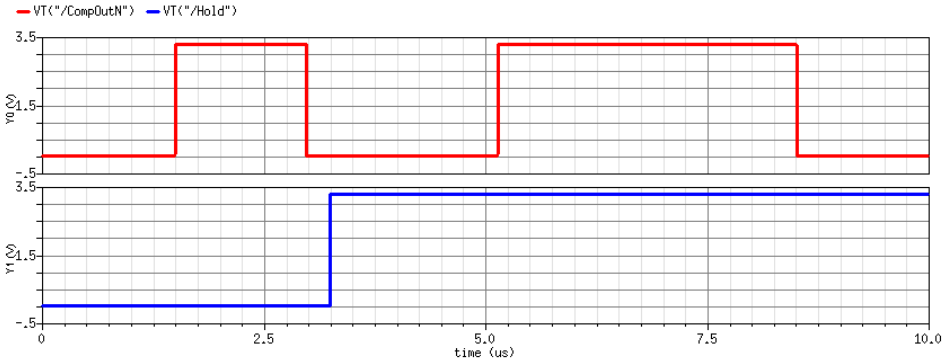
Detector current (1pC, 2pC)

Pre-amp output (Cf=10pF)



Shaper output (1μs peak)

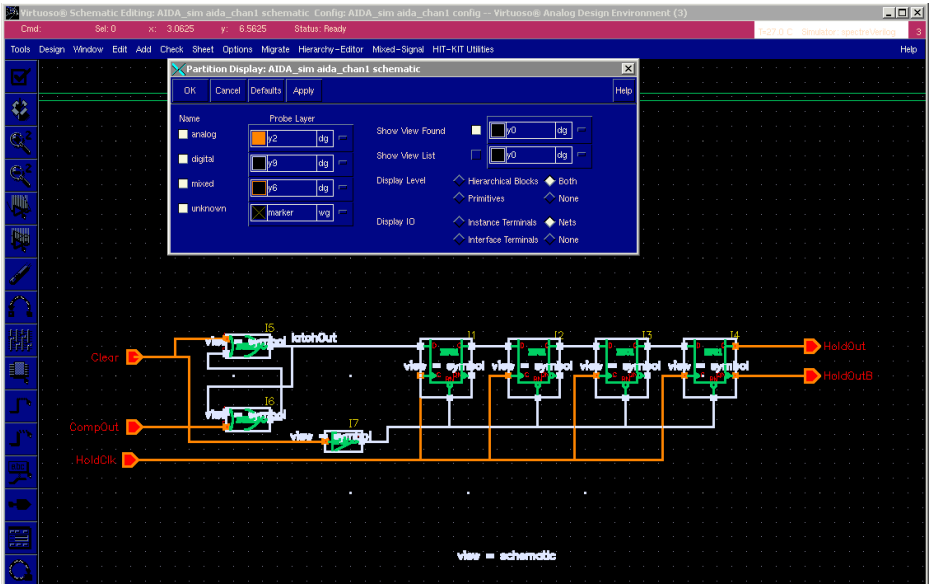
Peak-hold output

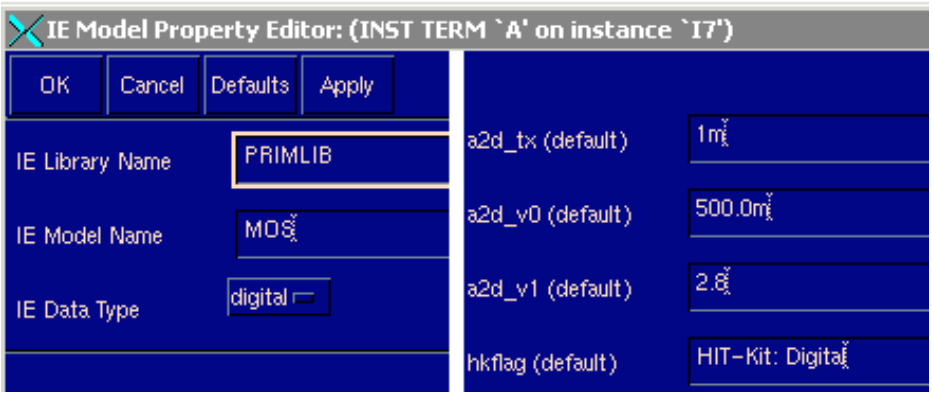


Comparator output

Peak-hold gate

Mixed-signal analysis





Benefits:

High-speed Verilog simulation for digital blocks

Accurate (but slow) simulations for analogue

Automatic generation of interface elements

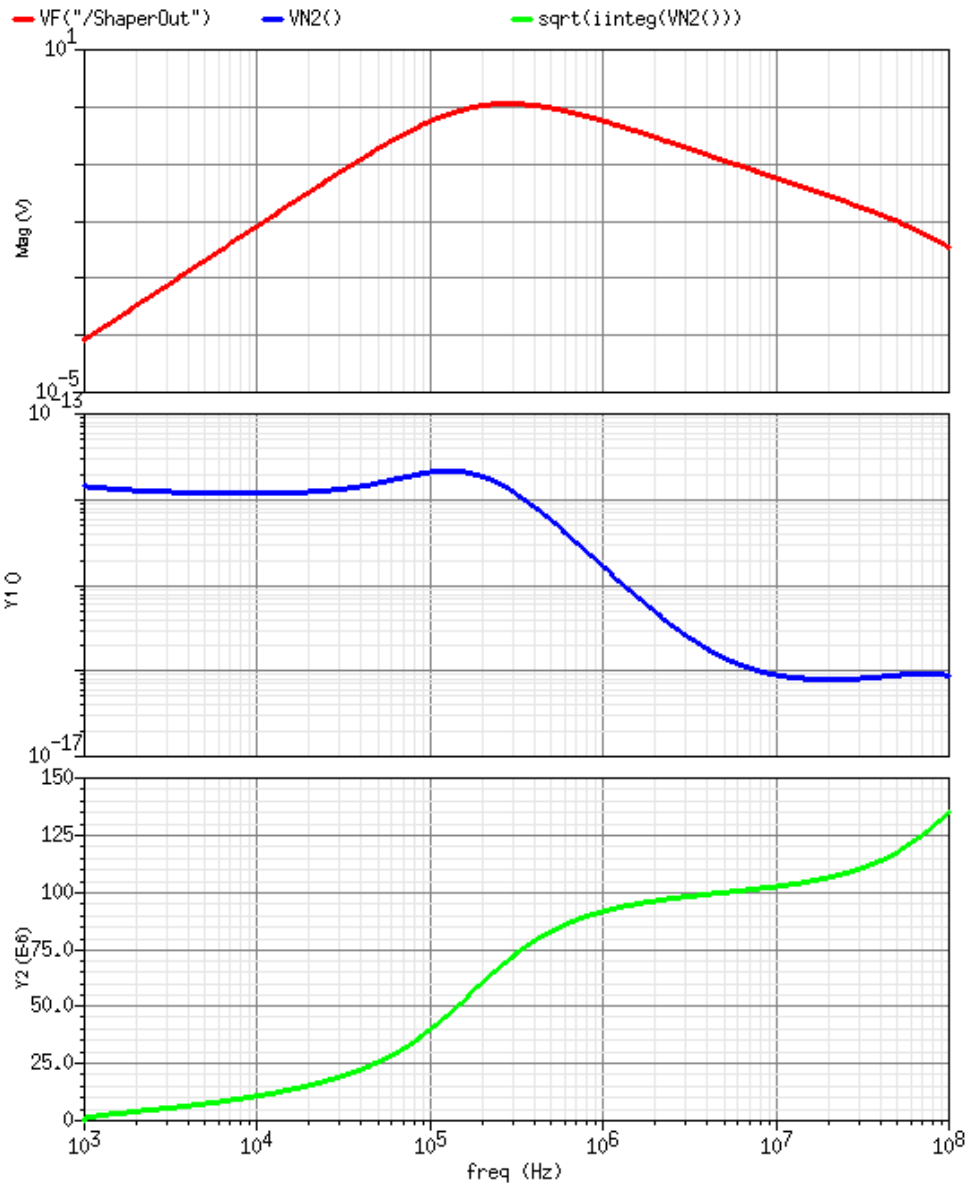
Problems:

Start-up of digital circuits - outputs of gates and latches can be undefined at t=0

Timing accuracy determined by functional model (text file).

Capacitance loading effects not automatically included

Frequency domain noise



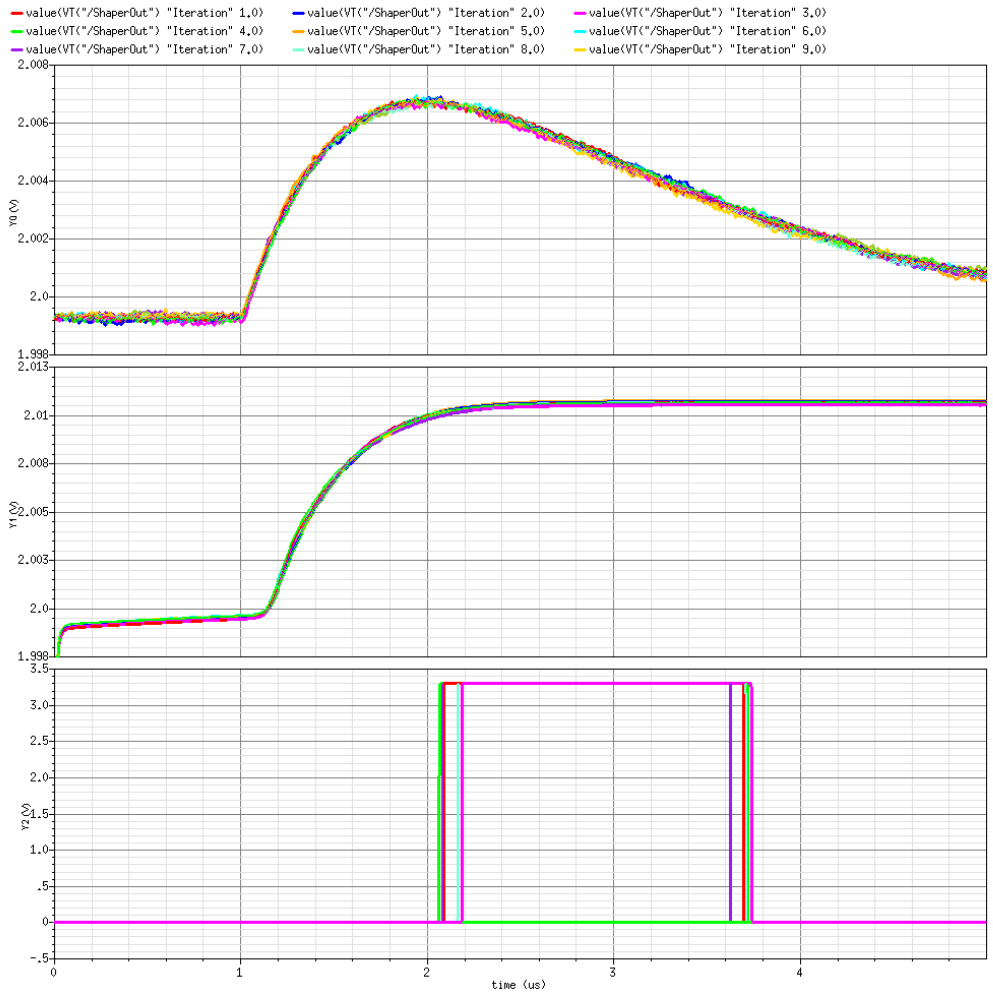
Analysis based on small-signal AC model : noise sources multiplied by AC transfer function to output.

Applicable only when circuits have small signal response

Noise at output is the sum of all specified noise sources.

Integrated noise gives an indication of critical frequency range.

Transient noise

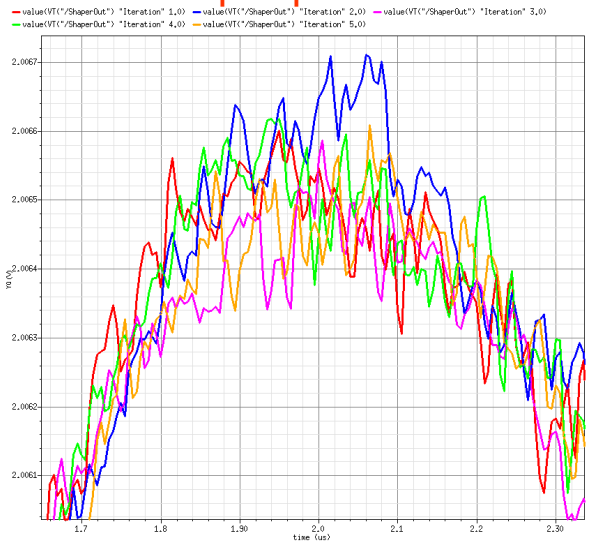


Shaper

Peak-hold

Comparator

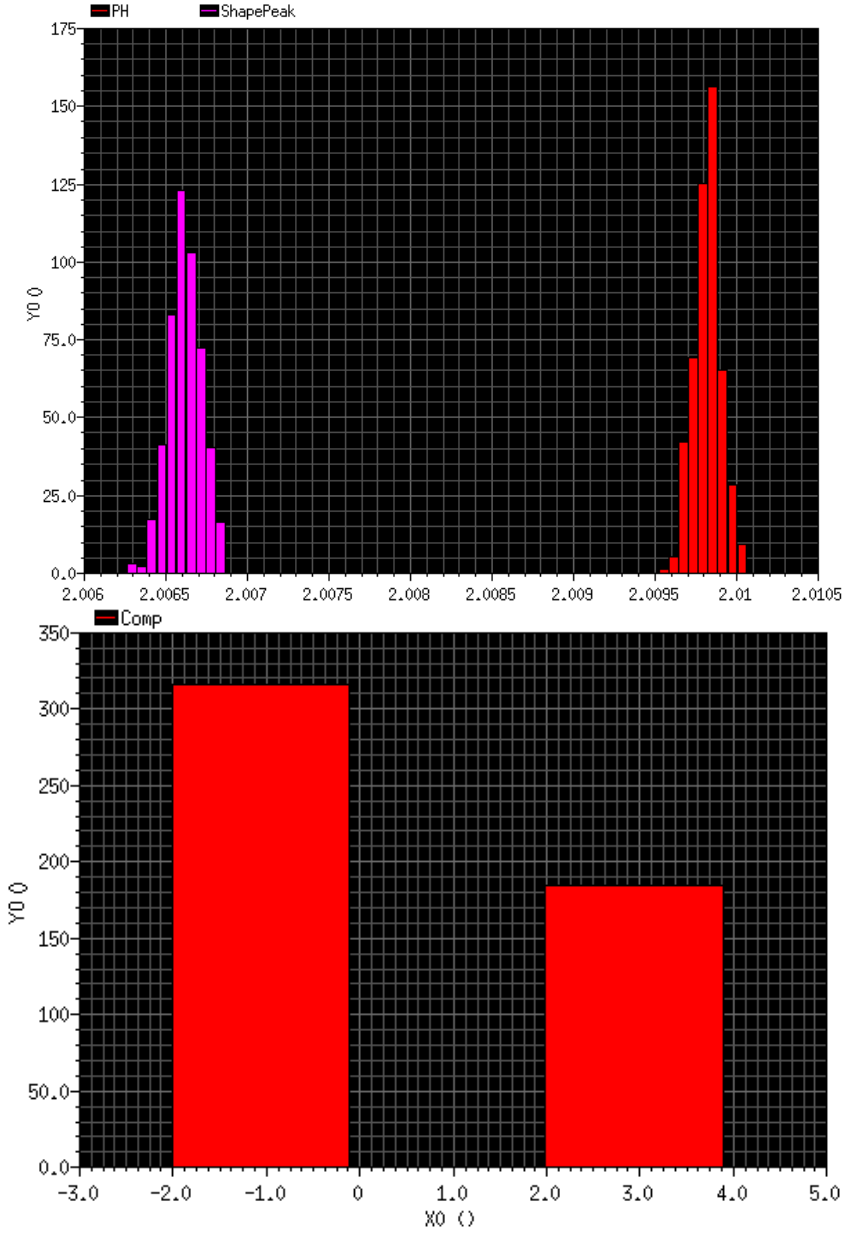
Shaper peak



10 transient noise simulations (different noise seeds)

Possible to evaluate equivalent noise of peak-hold and comparator

Transient noise histogram



Multiple transient run (500 iterations with random seeds)

Waveform parameters available for histogram

Left: shaper output at peaking time

Right : peak hold output, centred on comparator threshold

Comparator output (logic 1/0)

Future work

Simulation of pre-amp/shaper/link reset

Integration of single channel and top-level control circuit

Definition of digital interface, with example waveforms

Investigation of time-stamp issues

Physical layout, initially of front-end

Design completion in December 2007 still realistic