First SPES School on Experimental Techniques with Radioactive Beams

INFN LNS Catania – November 2011

Experimental Challenges
Lecture 3: Future Systems

Tom Davinson

School of Physics & Astronomy

Outline

Application Specific Integrated Circuits (ASICs)

- AIDA
- MUST II
- HINP16C/32C

New experimental techniques

- HELIOS

Case for ASICs

- Future Nuclear Physics Applications
  - detector areas 100-1000s cm^2
  - strip pitches ~0.5mm
  - 1000s channels of instrumentation required
- VLSI IC technology (CMOS)
  - low noise
  - high density
  - low power
  - low (per channel) cost … *in principle*
- Widely used
  - Particle Physics
  - Space
  - X-ray imaging
- Principal applications
  - Minimally ionising particles (MIPs), X-rays and low energy γ-rays
  - Emphasis on position information (e.g. ~10μm)
  - Excellent S/N ratios
    - high efficiency detection
    - low rate ‘false’ hits … important for *large* systems

ASICs: Reality Check

The Bad News (and there's quite a bit)…

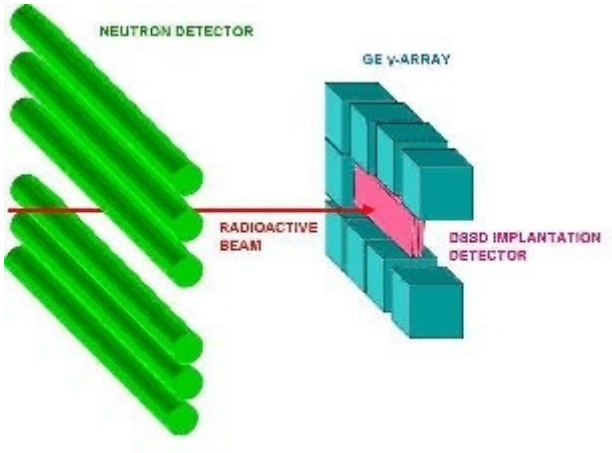
- CMOS design environment
  - passives temperature & voltage dependent
  - area constrains component values
  - parasitic effects
  - poor control of absolute component values
- Modelling
  - empirical data required
  - time consuming
- Entry costs
  - MPW – shared NRE costs, higher production costs
  - dedicated – high NRE costs, lower production costs
- Risk
- CMOS production process lifetime
- Limited dynamic range ~2,000:1 (cf. RAL108 ~100,000:1)
- ASIC channel pitch constrains detector strip pitch

The reality is that there are significant design and engineering limitations … compromise will be necessary.

AIDA: introduction

Advanced Implantation Detector Array (AIDA)

UK collaboration: *University of Edinburgh, University of Liverpool, STFC Daresbury Laboratory & STFC Rutherford Appleton Laboratory*



- SuperFRS/FAIR
- Exotic nuclei ~ 50 – 200MeV/u
- Implant – decay correlations
- Multi-GeV implantation events
- Subsequent low-energy decays
- Tag events for gamma and neutron detector arrays

Detector: multi-plane Si DSSD array
wafer thickness 1mm
8cm x 8cm (128x128 strips) *or* 24cm x 8cm (384x128 strips)

Instrumentation: ASIC
low noise (<12keV FWHM), low threshold (0.25% FSR)
20GeV FSR *plus* (20MeV FSR *or* 1GeV FSR)
fast overload recovery (~μs)
spectroscopy performance
time-stamping

ASIC Design Requirements

Selectable gain	20	1000	20000	MeV FSR
Low noise	12	600	50000	keV FWHM

energy measurement of implantation and decay events

Selectable threshold < 0.25 – 10% FSR

observe and measure low energy β, β detection efficiency

Integral non-linearity < 0.1% and differential non-linearity < 2% for > 95% FSR

spectrum analysis, calibration, threshold determination

Autonomous overload detection & recovery ~ μs

observe and measure fast implantation – decay correlations

Nominal signal processing time < 10μs

observe and measure fast decay – decay correlations

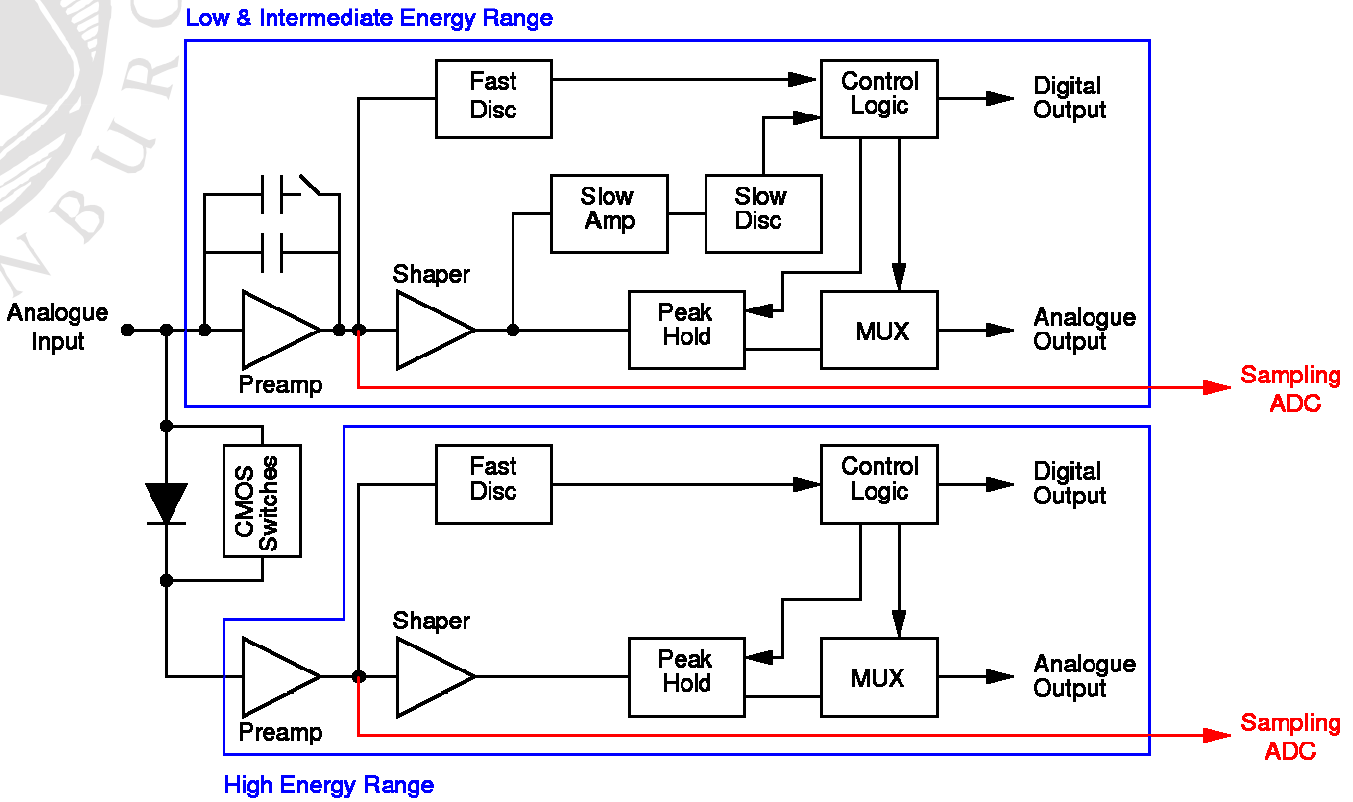
Receive (transmit) timestamp data

correlate events with data from other detector systems

Timing trigger for coincidences with other detector systems

DAQ rate management, neutron ToF

Schematic of ASIC Functionality



Note – ASIC will also evaluate use of digital signal processing

Potential advantages

- decay – decay correlations to ~ 200ns
- pulse shape analysis
- ballistic deficit correction

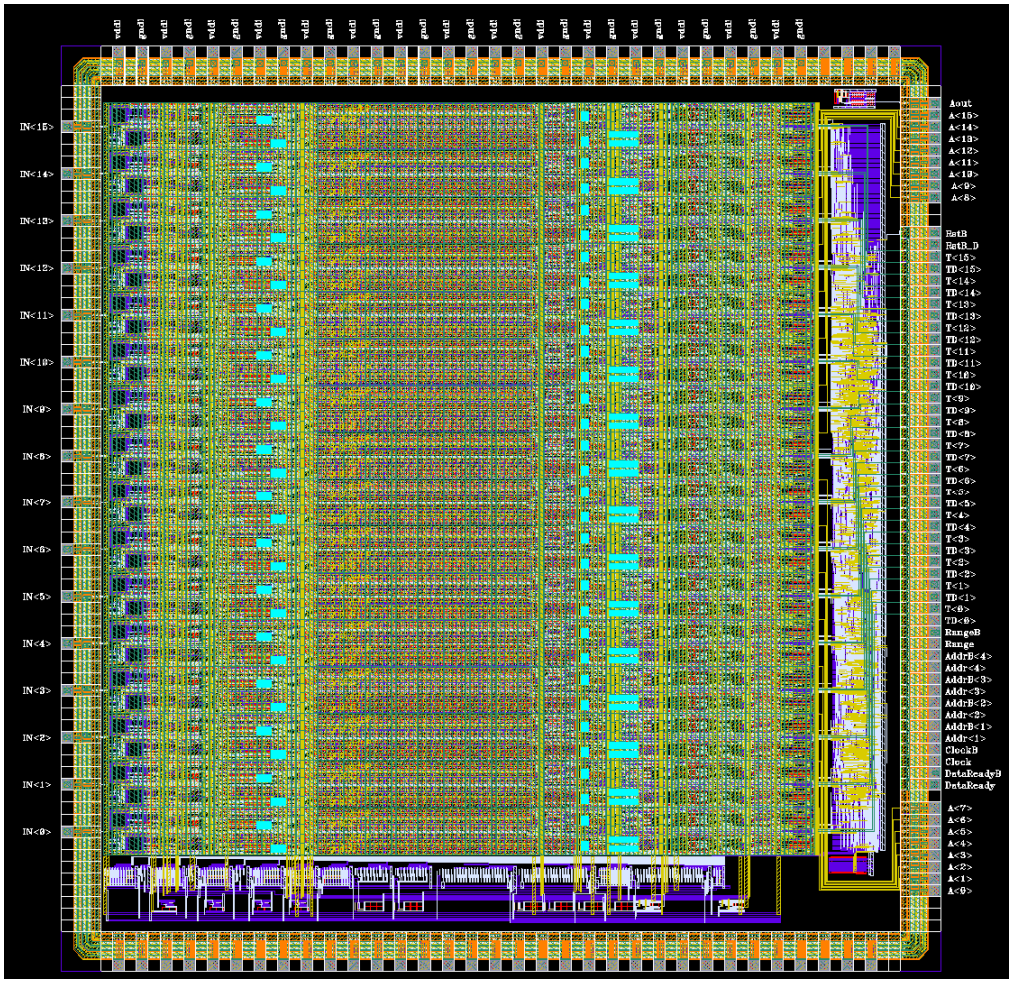
AIDA ASIC: Top level design

- Analogue inputs left edge
- Control/outputs right edge
- Power/bias top and bottom
- 16 channels per ASIC

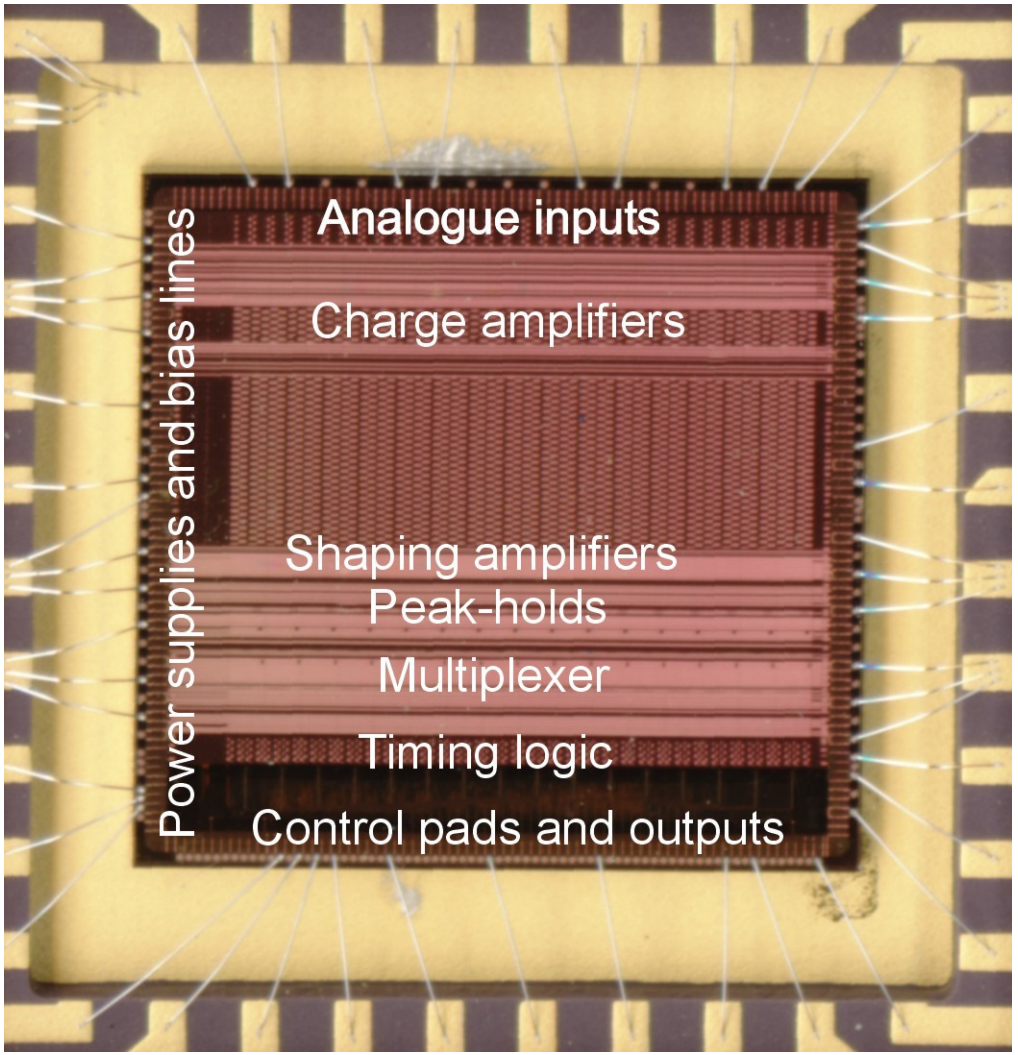
- Prototypes delivered May 2009
  MPW run
  100 dies delivered

- Functional tests at STFC RAL OK

courtesy STFC RAL

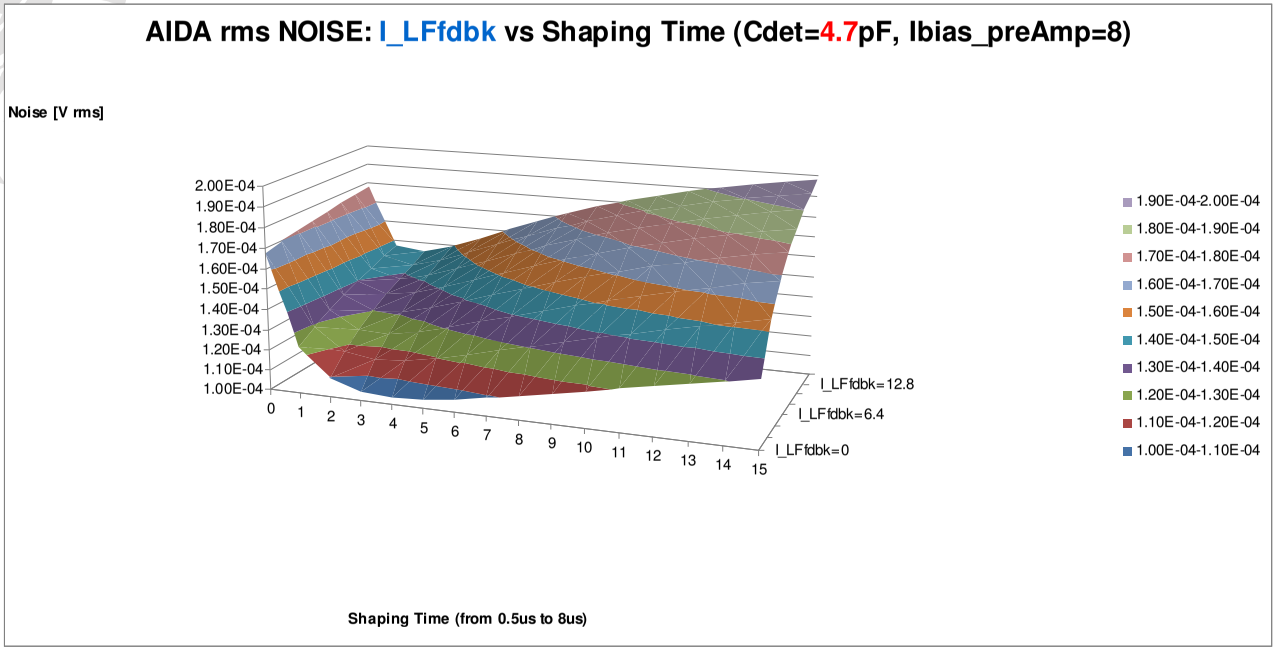


AIDA ASIC



courtesy STFC RAL

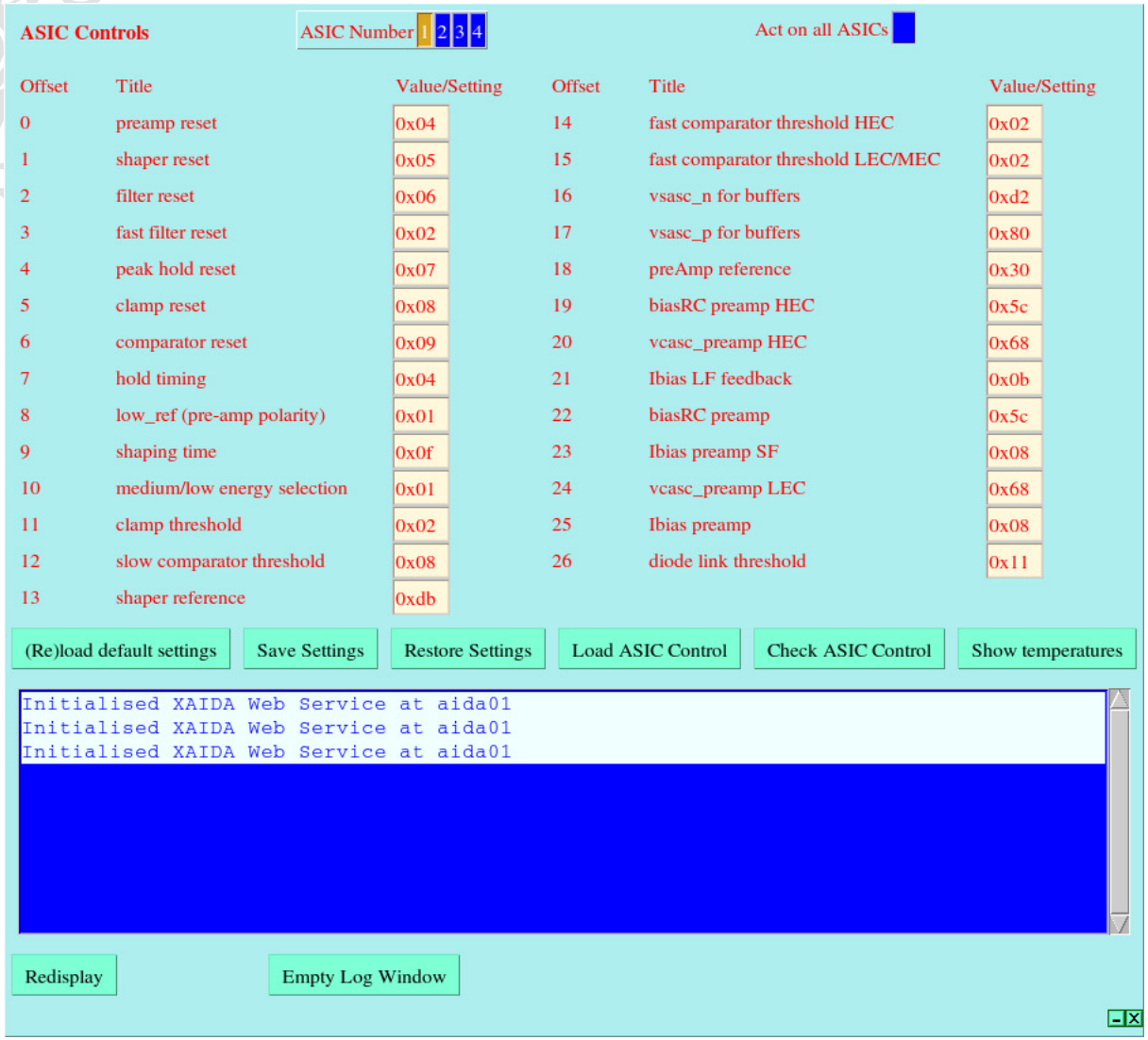
AIDA ASIC simulation: example



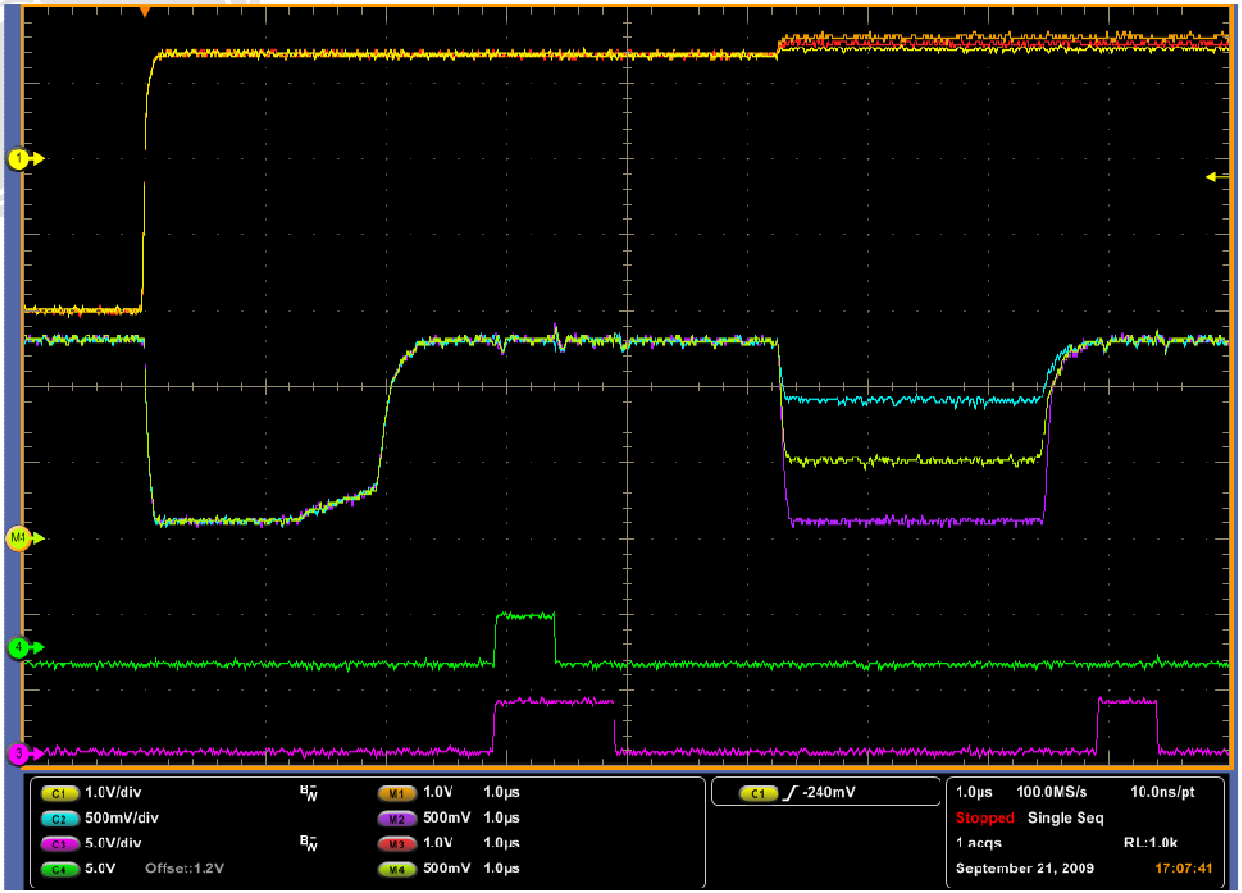
Optimum ASIC control parameters identified by simulation

courtesy STFC RAL

ASIC Controls



High Energy (HEC) + Medium Energy (MEC)



Input signals (voltage step capacitive-coupled)

Preamp buffered output (Low-Medium Energy Channel)

"Range" signal
High = high-energy channel active

"Data Ready" signal

Fixed high-energy (HEC) event (610pC/13.9GeV) followed by three MEC events (15pC, 30pC, 45pC): the ASIC recovers autonomously from the overload of the L-ME channel and the second event is read correctly.

High Energy (HEC) + Medium Energy (MEC)

Input signals (voltage step capacitive-coupled)

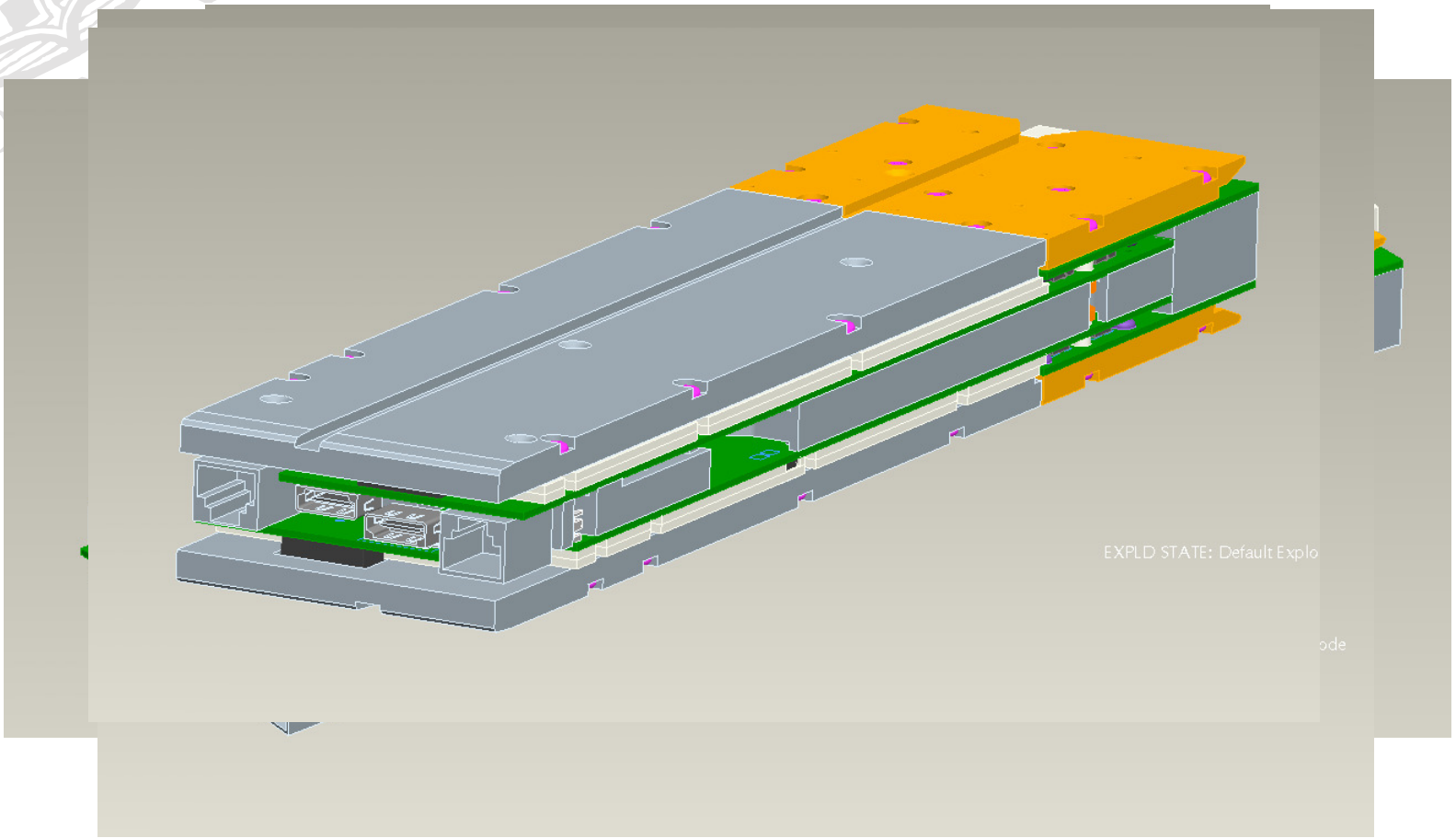
Analog output (peak-hold multiplexed output)

"Range" signal
High = high-energy channel active

"Data Ready" signal

First value (constant) given by the high-energy channel (HEC), second by the medium energy channel (MEC)

FEE Assembly Sequence

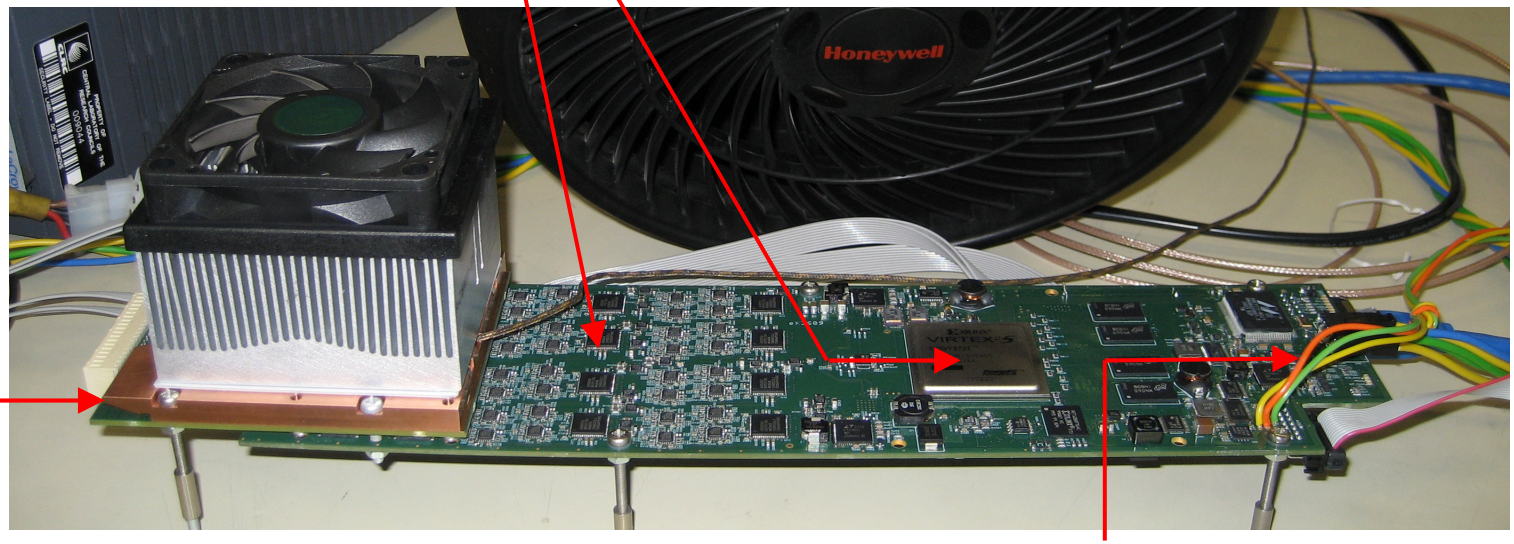


AIDA hardware

- Systems integrated production hardware available
  - bench & in-beam tests in progress

Mezzanine:
4x 16 channel ASICs
Cu cover
EMI/RFI/light screen
cooling

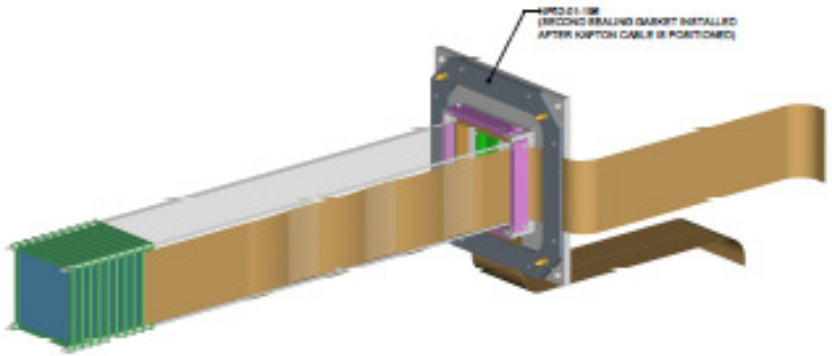
FEE:
4x 16-bit ADC MUX readout (*not visible*)
8x octal 50MSPS 14-bit ADCs
Xilinx Virtex 5 FPGA
550MHz PowerPC 440 CPU core – Linux OS



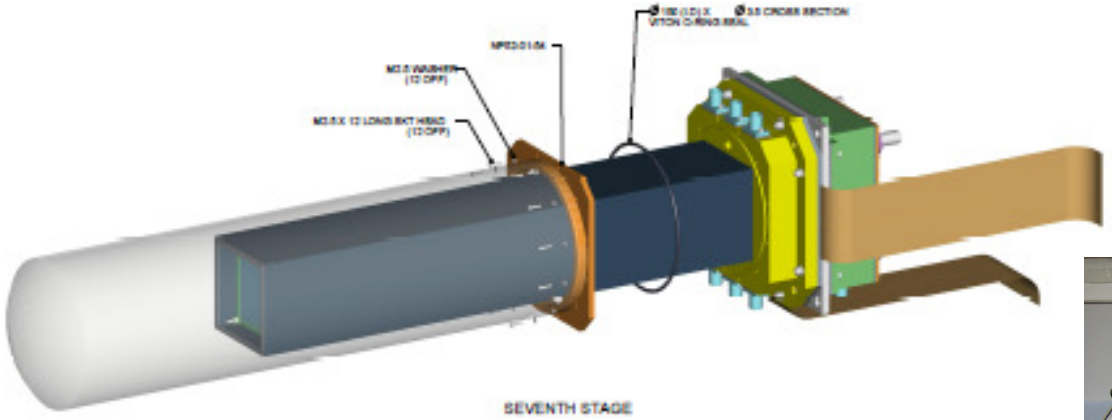
FEE width: 8cm
Prototype – air cooling
Production – recirculating coolant

Gbit ethernet, clock, JTAG ports
Power

Prototype AIDA Enclosure



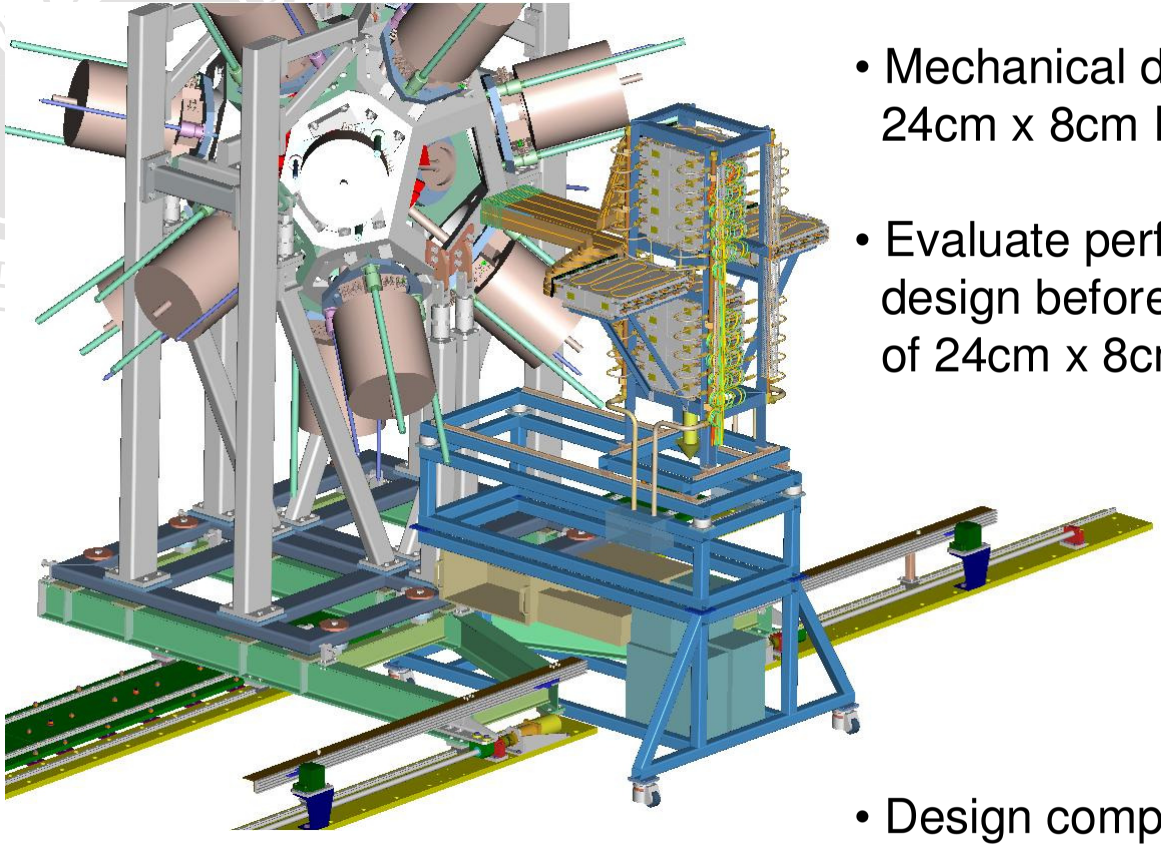
SECOND STAGE



SEVENTH STAGE

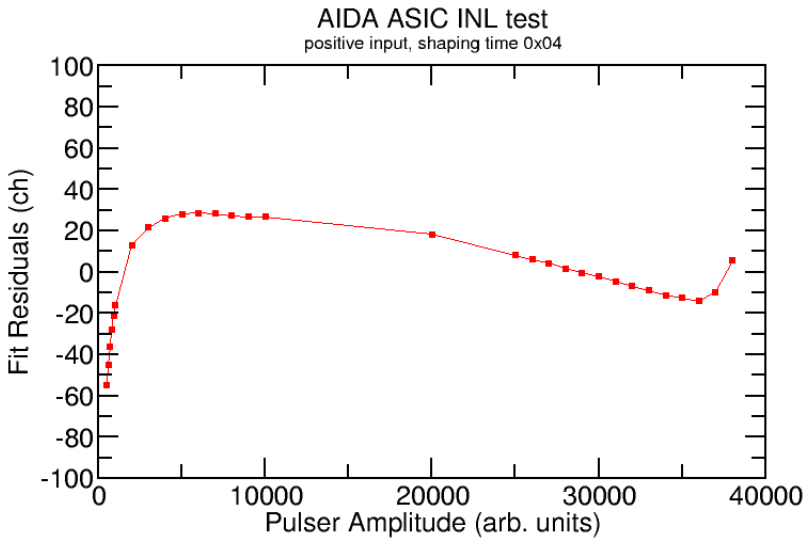
- Design drawings (PDF) available
  http://www.eng.dl.ac.uk/secure/np-work/AIDA/

AIDA Mechanical



- Mechanical design for 8cm x 8cm and 24cm x 8cm DSSSDs is complete
- Evaluate performance of 8cm x 8cm design before proceeding to manufacture of 24cm x 8cm design
- Design compatible with BELEN, TAS, MONSTER , RISING, FATIMA etc.

Bench Tests of *Prototype* Hardware

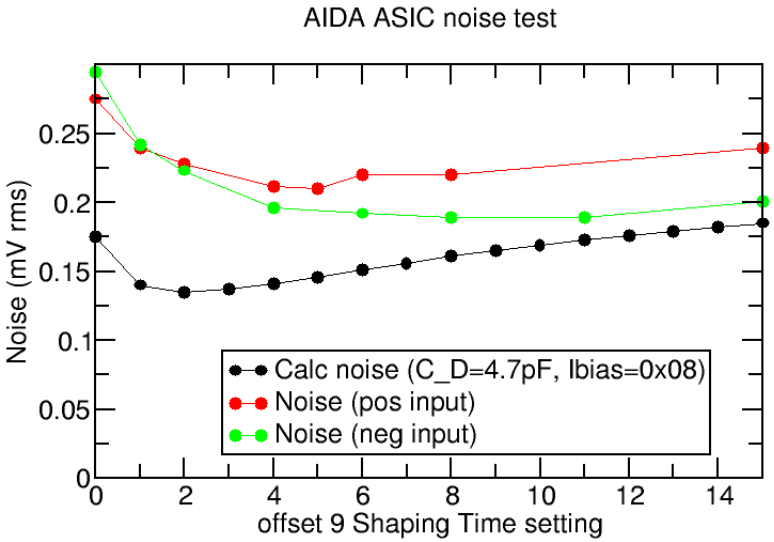


Tests with pulser demonstrating integral non-linearity and noise performance of 20MeV range (LEC)

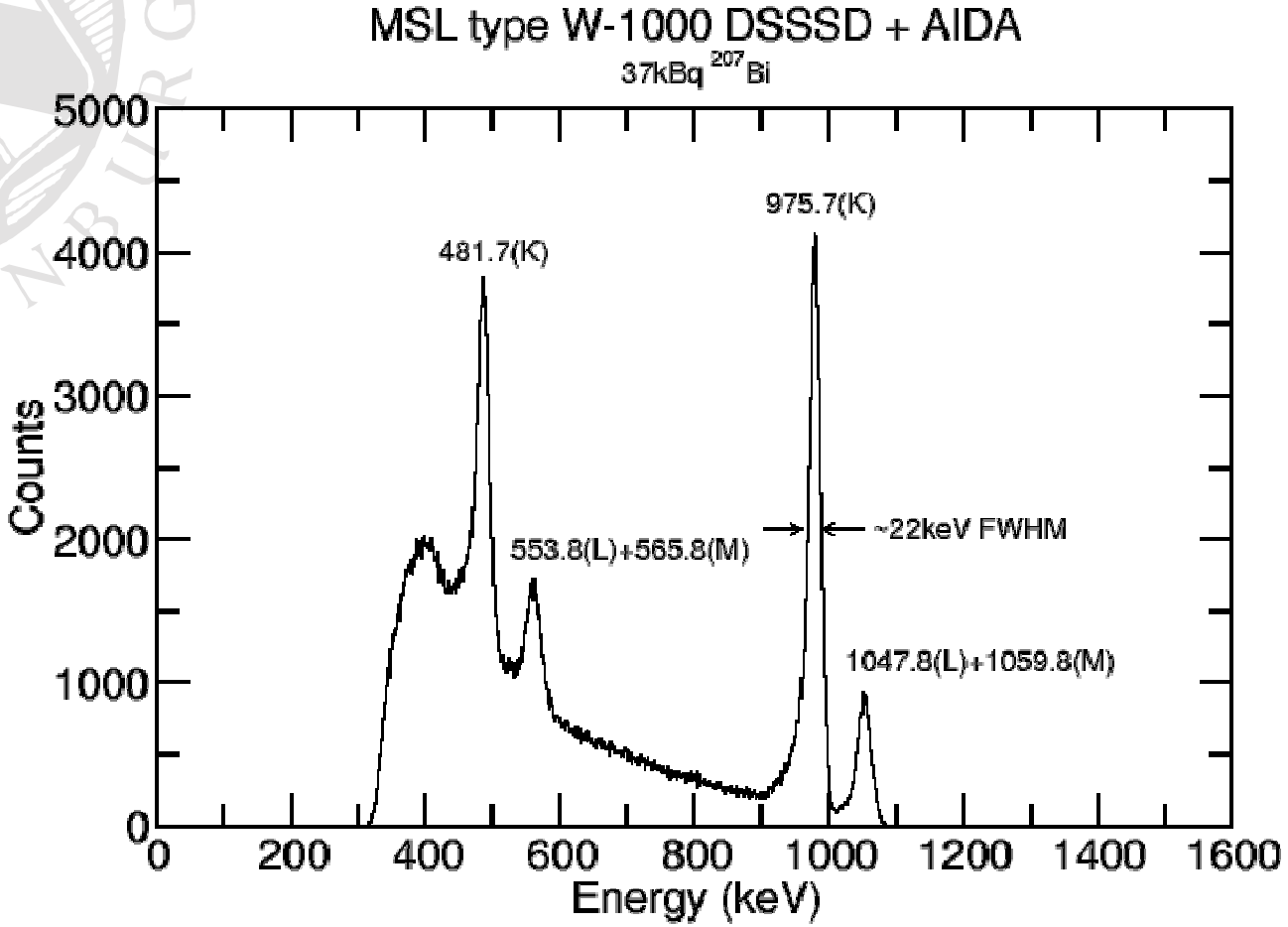
INL < 0.1% (> 95% FSR)

zero input load (C_D=I_L=0)

0.15mV rms ~ 2.5keV rms Si

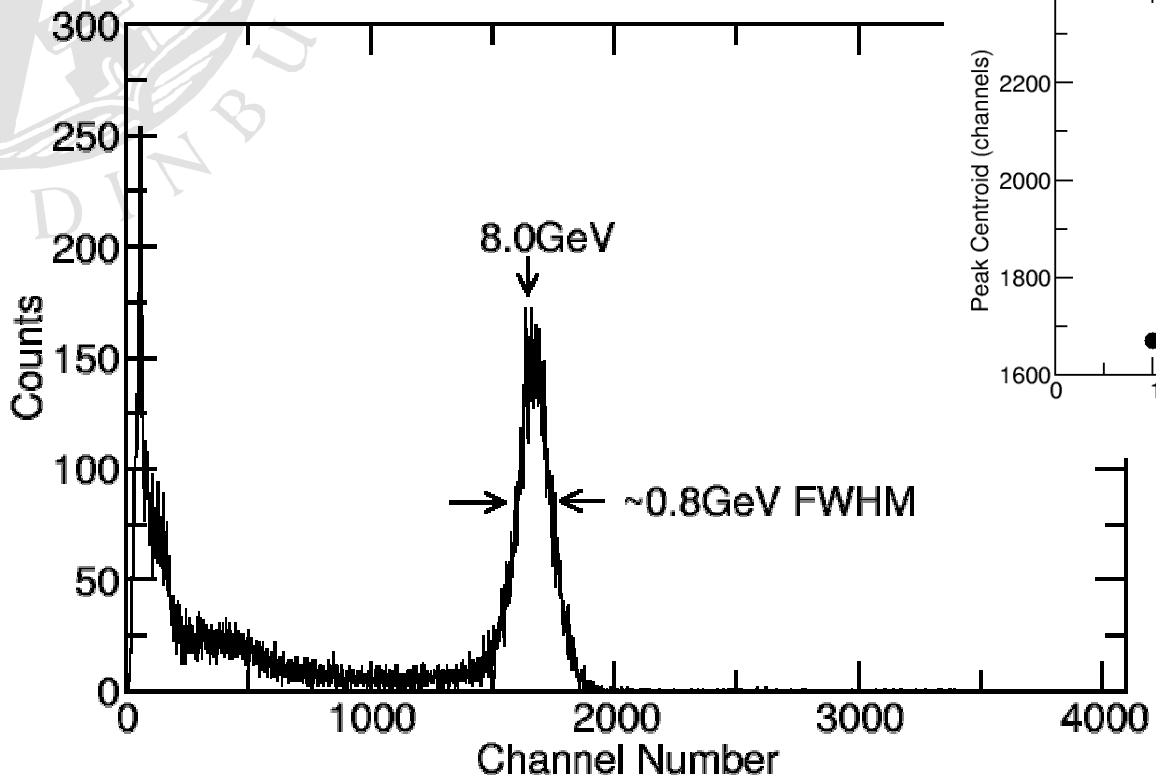


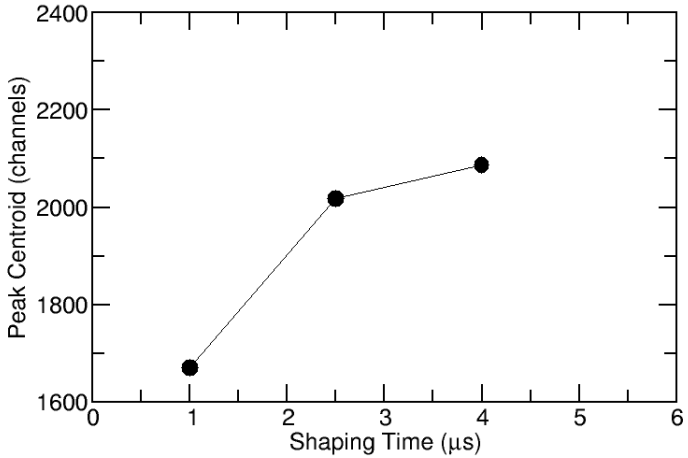
Tests with AIDA *Production* Hardware



- Realistic input loading C_D ~ 60pF, I_L ~ 60nA
- Expectation ~12keV FWHM

High Energy Implantation Events





- SIS 250MeV/u ^{209}Bi + degrader 2mm Al + ~2m air
- Significant ballistic deficit effects
- Confirms Bardelli model and previous TAMU observations
- Implies preamp risetime for high energy heavy-ions >500ns
  (cf. intrinsic preamp risetime ~90ns)

AIDA: status

- DSSSD with sub-contractor (MSL)
  - *12+ 8cm x 8cm production detectors delivery November 2011*
- Production hardware (ASIC, FEE Mezzanine PCB, FEE PCB) has been delivered by sub-contractors
- ASIC + FEE Mezzanine module assembly
  - *12 complete*
  - *65+ queued*
- FEE PCB QA acceptance tests
  - *50 complete*
  - *20 queued*
  - *8 with faults requiring further testing*
- Mechanical design and infrastructure (HV, PSUs, cooling etc.)
  - *detector HV, FEE PSUs, cooling & FEE crates delivered*
  - *support assembly University of Liverpool workshop*

AIDA: outlook

- AIDA production hardware was available for commissioning on schedule in 2011/Q3

- Performance of 20GeV & 1GeV ranges meets specification
  - *need to optimise DSSSD-FEE coupling for 20MeV range*
  - *progress very encouraging*

- Basic data merge with MBS successfully demonstrated during AIDA+LYCCA test May 2011
  - *further work required*

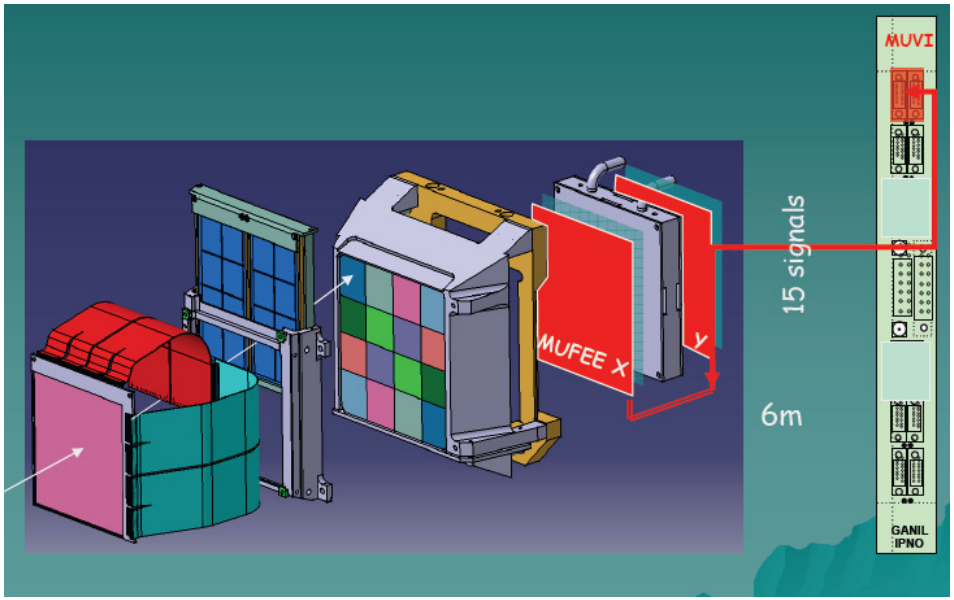
- Continuing FEE development work in progress
  - *DSP (e.g. digital CFD, MWD)*
  - *timestamp distribution hardware*

- DAQ software development work in progress
  - *migrating interface from Tcl/Tk to XML/SOAP (web-based)*
  - *control and management of multiple FEE modules*
  - *timestamp-ordered data merge*

Translation – AIDA is ready for early science experiments

MUST II

- Nuclear physics application
- High-energy light & heavy ion detection
- Composite telescope (PID)
  Si DSSD ΔE - Si(Li) E_1 - CsI(Tl) E_2
- Energy & time spectroscopy
- Vacuum operation
- ToF requirements … BiCMOS technology

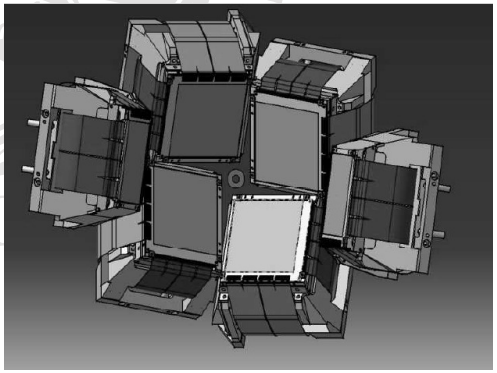


- Channels 16 (Fast & Slow)
  - Full Bipolar
  - Slow Control – I2C
  - Energy
    - 1µs/3µs RC-CR
    - 11,22,50, 100, 200,500,1000 MeV
    - 8 keV resoln. for 50 MeV
    - T/H
  - Time
    - Disc Leading Edge
    - TAC (300 or 600 nsec)
    - Common stop
    - 100 psec jitter
- Chip 36mm²
  - 16K transistors & 35mW/Ch
- Serial output 2 MHz

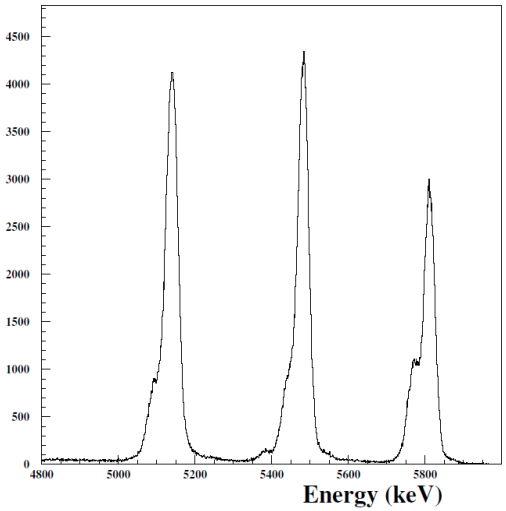
http://ipnweb.in2p3.fr/~sep/projets/exp/must2/must2.html

MUST II contd

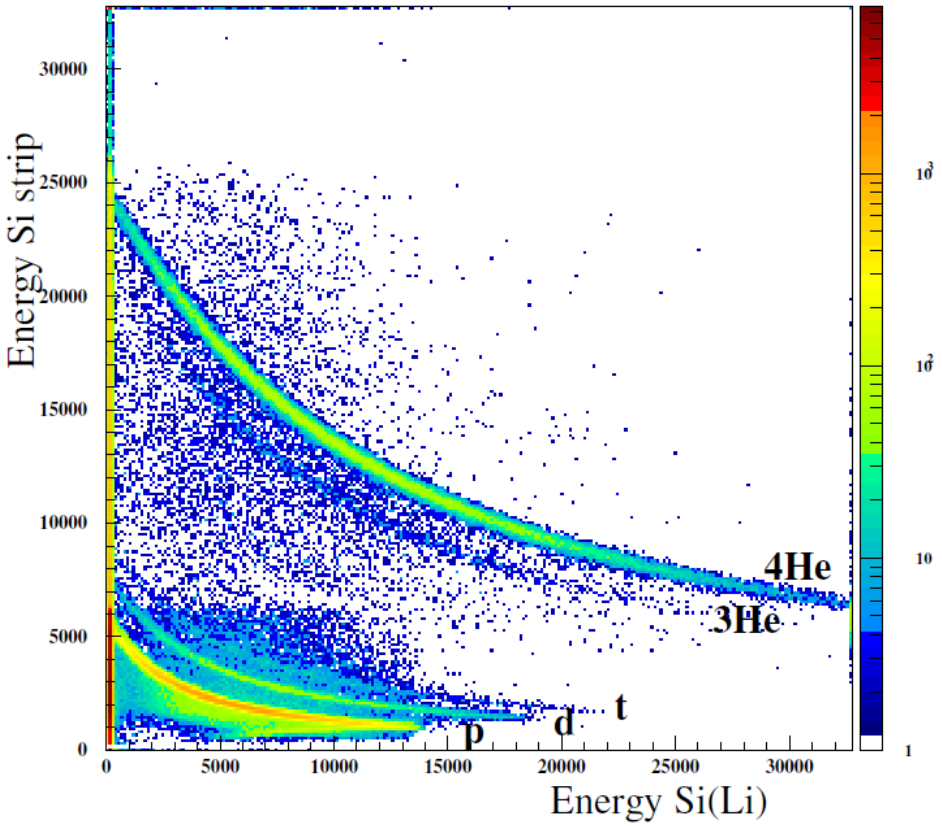
Six telescope array



35keV FWHM (128 ch)



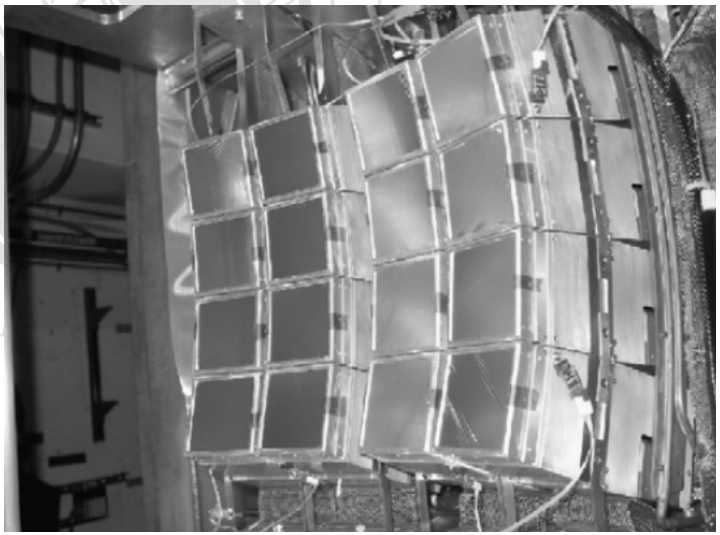
10MeV/u 58Ni + CDH target
DSSSD + Si(Li) *only*



ΔE 1keV/ch, E 2keV/ch

E.Pollacco *et al.*, EPJ A25 (2005) 287

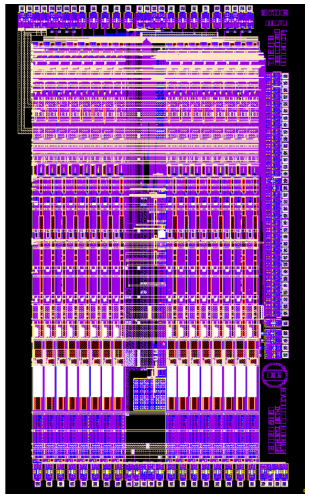
HiRa



Measured performance

Parameters	Value (measured)
Energy branch	
Resolution at 75 pF	38 keV
Linear range in LOW gain mode	500 MeV
Linear range in HIGH gain mode	100 MeV
CSA gain in LOW gain mode	3 mV/MeV (0.08 mV/fC)
CSA gain in HIGH gain mode	15 mV/Mev (0.4 mV/fC)
Timing branch	
Walk through CFD	<1 ns over a range of 40 dB
Jitter	1 ns

- 20x 65μm DSSSD $\Delta E1$ + 1500μm DSSSD $\Delta E2$
  + 4cm CsI(Tl) E particle telescopes
  area 6.25cm x 6.25cm
- ~2000 channels
- high energy (~65MeV/u) transfer reactions



HINPC16 (Heavy Ion Nuclear Physics 16 channels) ASIC

G.L.Engel *et al.,* NIM A573 (2007) 418
M.S.Wallace *et al.,* NIM A583 (2007) 302

The Bottom Line

Project timeline

- dominated by ‘design’, simulation and test phases

‘if you don’t test it, it won’t work’

Project costs

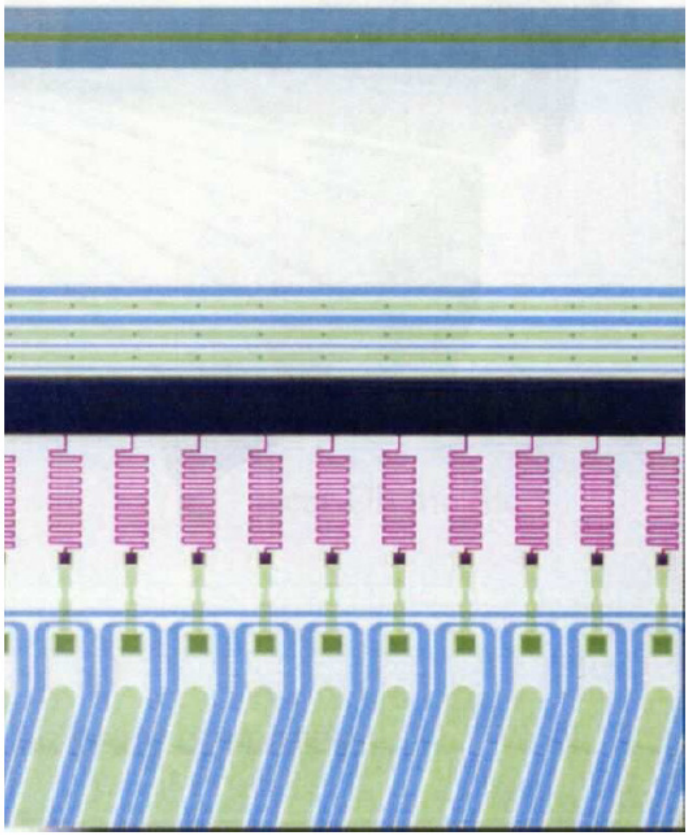
- dominated by manpower costs
- ASIC cost is a fraction of *system/hardware* cost

rule of thumb … 2–3x ASIC cost

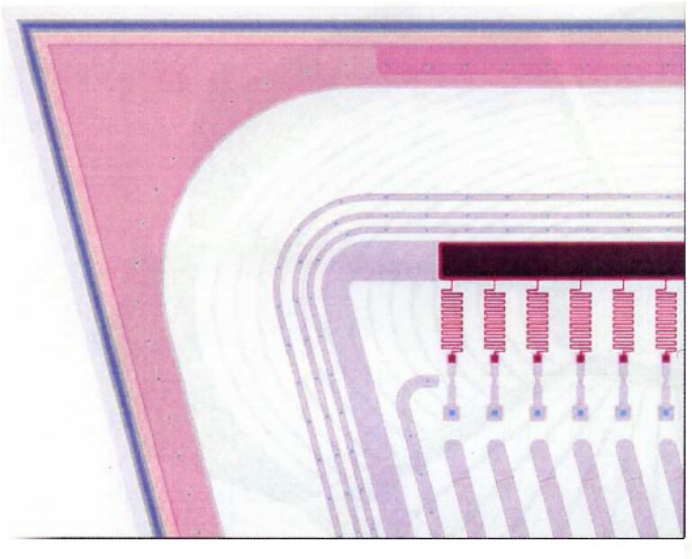
… and did I mention detectors?

ASIC Compatible Silicon Strip Detectors

- Integrated coupling capacitors
  ~100pF/100V
- Integrated poly-Si bias resistors
  ~1-50MΩ
- Strip pitch
  ASIC compatible

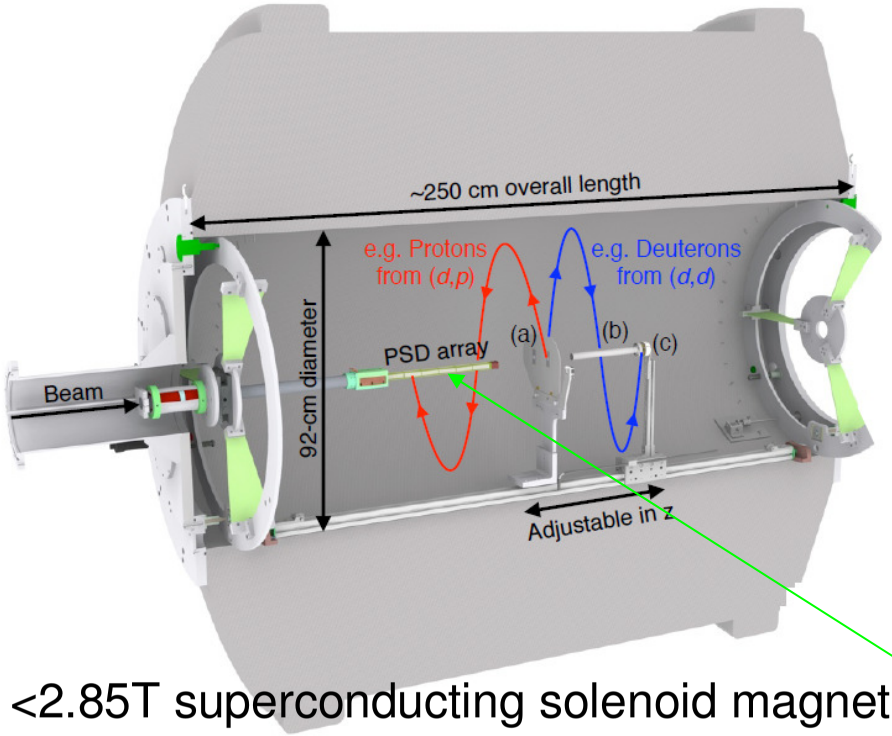


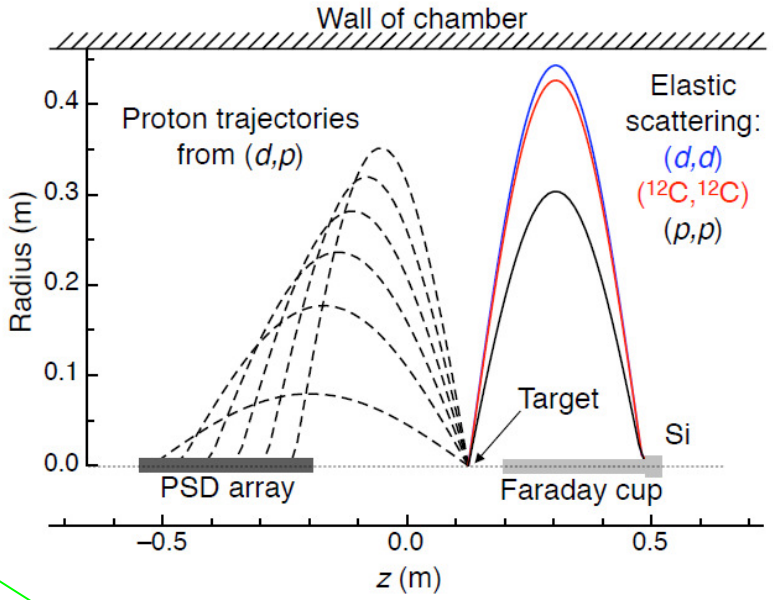
from MSL type HHH(DS)



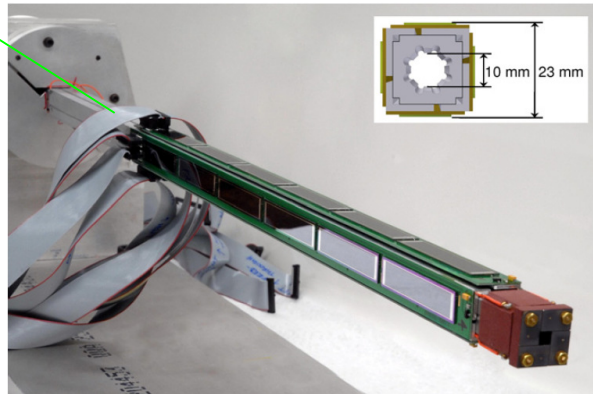
- Design complexity
  more photomasks
  higher NRE costs ~$40-60k
- Production complexity
  more processing steps
  lower yields
  higher costs ~$10-15k
- Larger area (6” wafers)
  restricted range of thicknesses

HELIOS





- <2.85T superconducting solenoid magnet
- Detector $\Delta\Omega_{CM}$ ~ 0.5sr
- Further developments
  - upstream PSD array
  - cryogenic gas cell
  - downstream Bragg detector



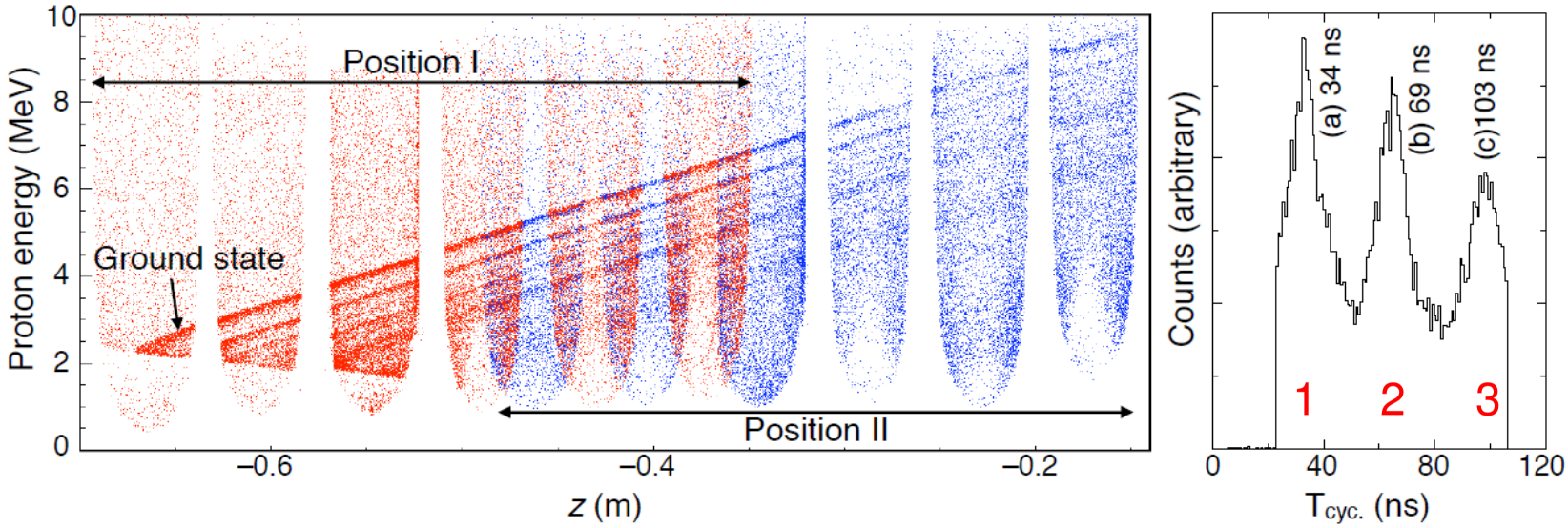
4x 6x ~50mm x 9mm PSD

B.P.Kay *et al.*, J. Phys. 312 (2011) 092034

J.C.Lighthall *et al.*, NIM A622 (2010) 97

http://www.phy.anl.gov/atlas/helios/index.html

HELIOS

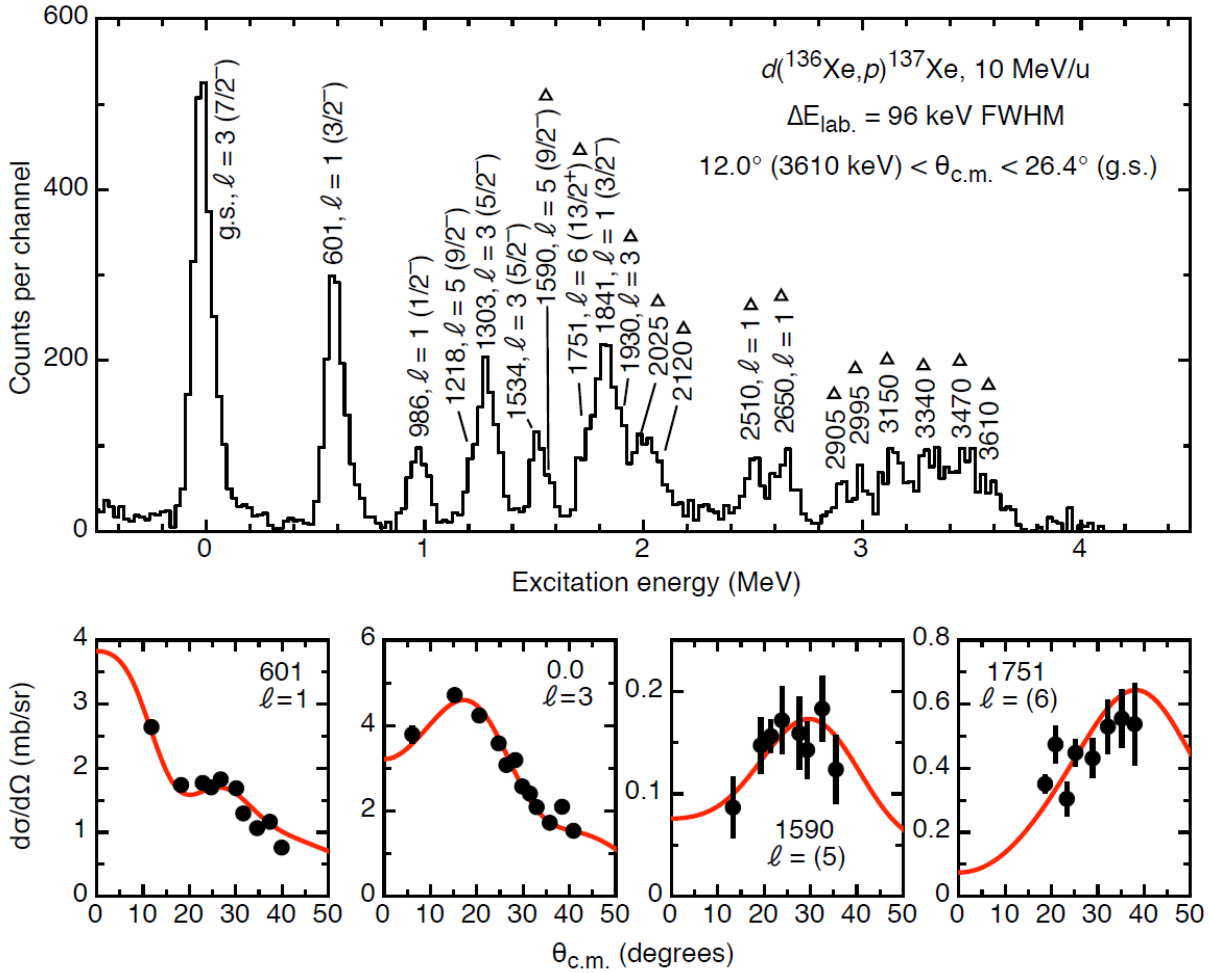


Measured quantities: $T_{flight} = T_{cyc}$, position z, E_{lab}
Derived quantities: m/q, E_{CM}, θ_{CM}

Effectively removes kinematic angular resolution effects and avoids kinematic compression (measure z not θ)
Target thickness remains an issue as with more conventional detector systems

B.P.Kay *et al.*, J. Phys. 312 (2011) 092034

HELIOS



~10^7/s ^{136}Xe + ~150µg/cm^2 $(CD_2)_n$

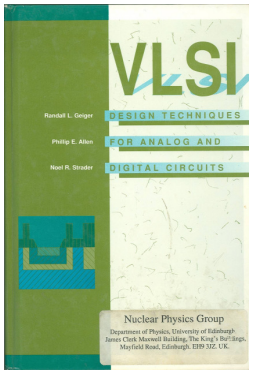
B.P.Kay *et al.*, J. Phys. 312 (2011) 092034

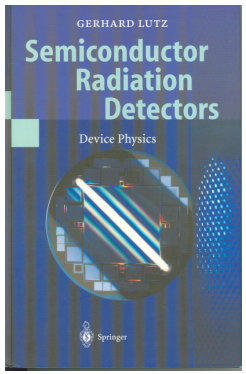
ASIC Summary

- Silicon strip detectors
  - pervasive technology
- ASICs
  - wide range of applications
  - sophisticated design
  - high performance
  - accessible and affordable technology
- Critically dependent on
  - engineering expertise
  - systems integration

Further Reading

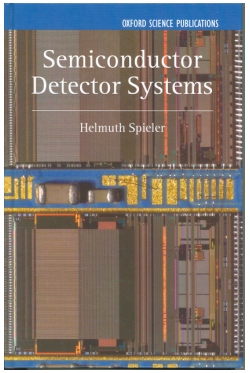
VLSI Design Techniques for Analog and Digital Circuits,
R.L.Geiger, P.E.Allen and N.R.Strader, McGraw-Hill, 1999





Semiconductor Radiation Detectors,
Gerhard Lutz, Springer Verlag, 1999

Semiconductor Detector Systems,
Helmuth Spieler, Oxford, 2005
http://www-physics.lbl.gov/~spieler/



AIDA Acknowledgements

My thanks to:

STFC DL
P. Coleman-Smith, M. Kogimtzis, I. Lazarus, S. Letts, P. Morrall, V. Pucknell, J. Simpson & J. Strachan

STFC RAL
D. Braga, M. Prydderch *&* S. Thomas

University of Liverpool
T. Grahn, P. Nolan, R. Page, S. Ritta-Antila *&* D. Seddon

University of Edinburgh
Z. Liu, G. Lotay & P. Woods

University of Brighton
O. Roberts

GSI
F. Amek, L. Cortes, J. Gerl, E. Merchan, S. Pietri *et al.*